AMD's processor lines belonging to the Intermediate Families (Families 11h (Griffin) and 12h (Llano))

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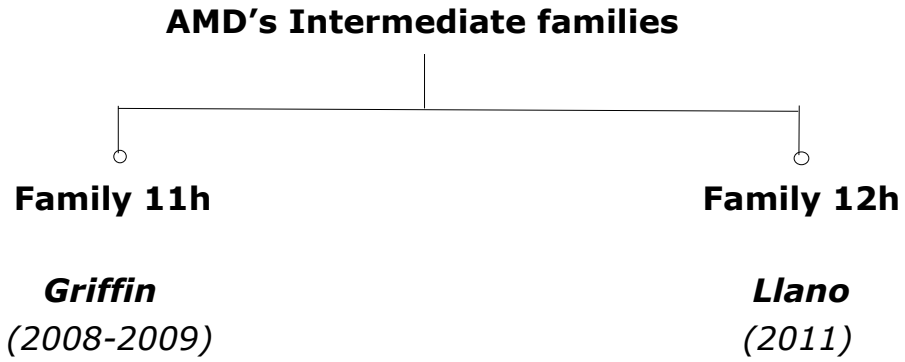
(Ver. 1.1)

AMD's processor lines belonging to the Intermediate Families (Families 11h (Griffin) and 12h (Llano))

- 1. Overview of AMD's Intermediate families
- 2. The Family 11h (Griffin) Family
- 3. The Family 12h (Llano) Family
- 4. References

1. Overview of AMD’s Intermediate Families

1.1. Overview of AMD's Intermediate families



1.1 Overview of AMD's Intermendiate families (2)

Brand names of AMD's Intermediate families

	Launched in	2008-2009	2011
		Family 11h (**Griffin**)	**Family 12h** (**Llano**)
Servers	**4P servers**		
	2P servers		
	1P servers		
	(85-140 W)		
Desktops	**High perf.** (~95-125 W)		
	Mainstream (~65-100 W)		Llano A8/A6/A4/E2 Sempron X2
	Entry level (40-60 W)		
Notebooks	**High perf.** (~30-60 W)	Turion X2 Ultra (ZM-xx) Turion X2 (RM-xx)	Llano A8 M
	Mainstream/Entry (~20-30 W)	Athlon X2 (QL-xx) Sempron (SI-xx)	Llano A6/A4/E2 M
	Ultra portable (~10-15 W)	Turion Neo X2 (L6xx) Turion X2 (RM-xx) Athlon Neo X2 (L3xx) Sempron (200U/210U)	
Tablet (~5 W)			
Embedded (~10 – 20 W)		Turion Neo X2 (L6xx) Athlon Neo X2 (L3xx) Sempron (200U/210U)	

2.3.2 Mobile APU lines of the Brazos platform (20)

Main features of Intermediate, Cat and Zen-based mainstream mobile lines

Base arch./ stepping	Intro	High perf. mobile family name	Series	Techn.	Core count (up to)	L2 (up to)	L3	Memory (up to)	TDP [W]	Sock et
Family 11h (K11) (Griffin)	6/2008	Lion (no APU) (not SoC)	Turion X2 Ultra	65 nm	2	2x512 KB/ 2*1 MB[2]	-	DDR2-800	31-35	S1g2
Family 12h (K12) (Llano)	6/2011	Llano (APU) (not SoC)	Fusion A8 M	32 nm	4	4x1 MB	-	DDR3-1600		FM1
Family14h (00h-0Fh) (Bobcat)	1/2011	Zacate (APU) (not SoC)	Fusion E	40 nm	2	2x512 KB	-	DDR3L-1333		FT1 (BGA)
Family 16h (10H-1fH) (Jaguar)	5/2013	Kabini APU (SoC)	A Series	28 nm	4 cores with a shared L2 cache	2 MB shared	-	DDR3L-1866		FT3
Family 16h (30H-3fH) (Puma+)	4/2014	Beemai APU (SoC)	A4 Series	28 nm		2 MB shared	-	DDR3L-1866		FT3b
Family 16h (30H-3fH) (Puma+)	5/2015	Carrizo-L APU (SoC)	A8/A6/ A4 Series	28 nm		2 MB shared	-	DDR3L-1866		FP4
Family 17h (00H-0fH) (Zen)	10/2017	Raven Ridge APU (SoC)	Ryzen 7/5/3	14 nm	4-core CCX with private L2 caches and shared L3	½ MB /core	1 MB/ core	DDR4-2400		AM4

APU: Accelerated Processing Unit (CPU +GPU) CCX: Core CompleX

[2]: 2*512 KB for Turion X2, 2*1 MB for Turion X2 Ultra

UMI: Universal Media Interface

2. The 11h Griffin Family

- 2.1 Overview of the 11h Griffin Family
- 2.2 Main enhancements of the 11h Griffin Family
- 2.3 The 11h Griffin mobile lines

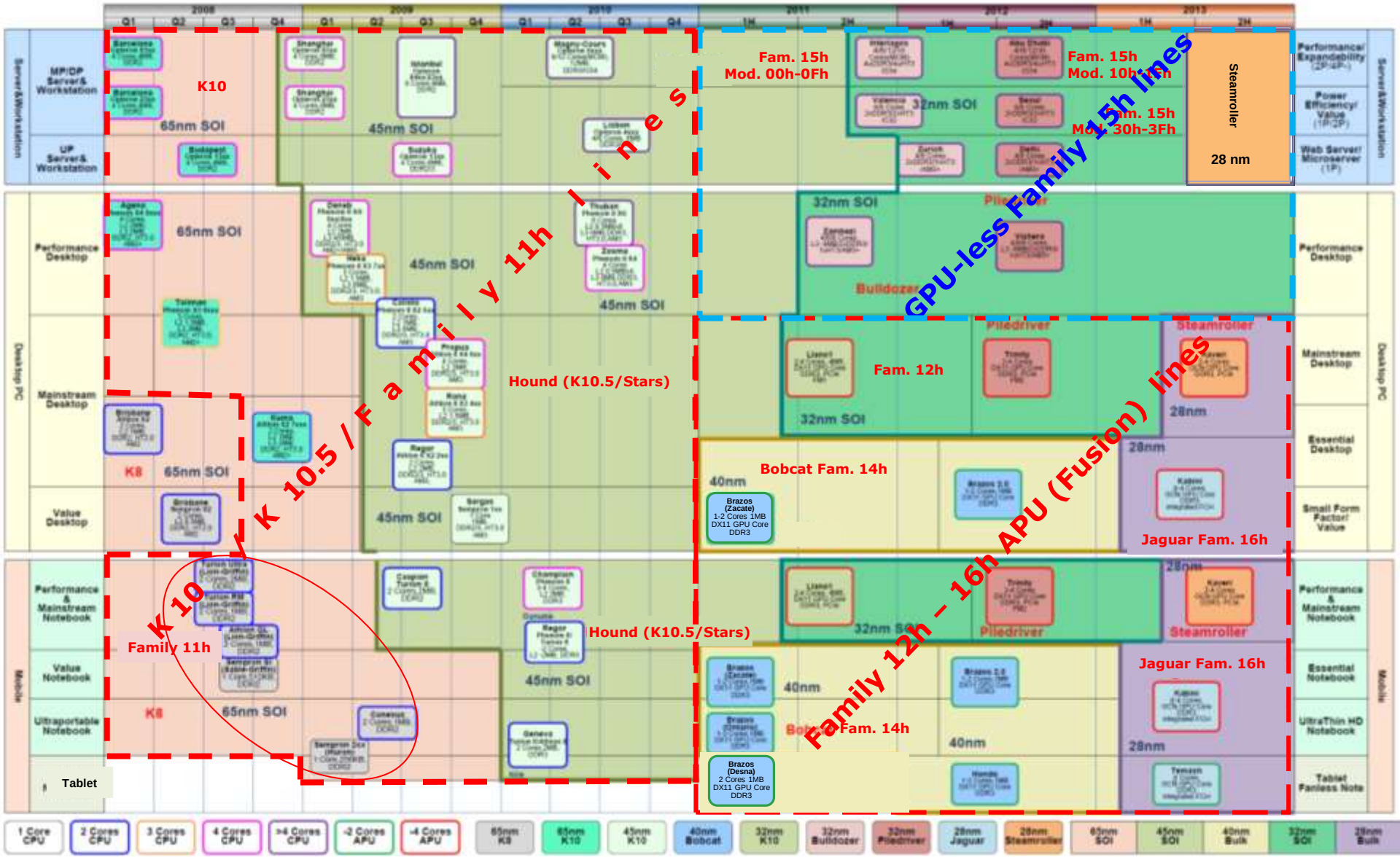
2.1 Overview of the 11h Griffin Family

2.1 Oveview of the 11h Griffin family

- Introduced: in 6/2008, it preceded the K10.5 Shanghai-based mobiles
- Processor family designed solely for mobiles
- Derived from the 65 nm K8 Brisbane-based Turion 64 X2 (Tyler die) [4]
- Design emphasis on power saving
- Until now it is AMD's only design with per processor power planes, i.e. with fully independent per processor P-state control
- AMD's first processor family supporting HyperTransport 3.0
- 2C, 65 nm technology
- 160 mm^2, 225.6 mtrs

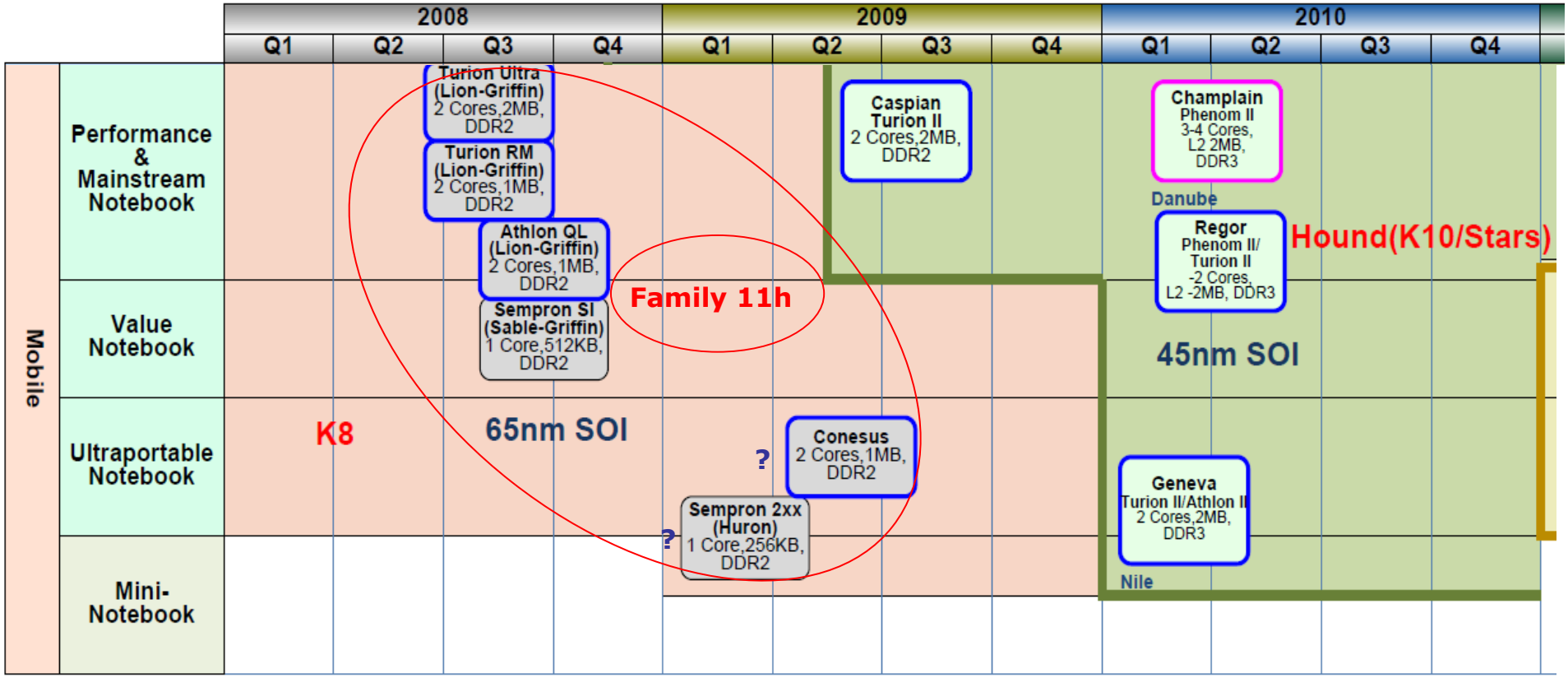
10.1 Overview of the 11h Griffin Family (2)

AMD's 11h Griffin-based mobile lines – Overview-1 [2]



2.1 Overview of the 11h Griffin Family (3)

AMD's 11h Griffin-based mobile lines – Overview-2 [2]

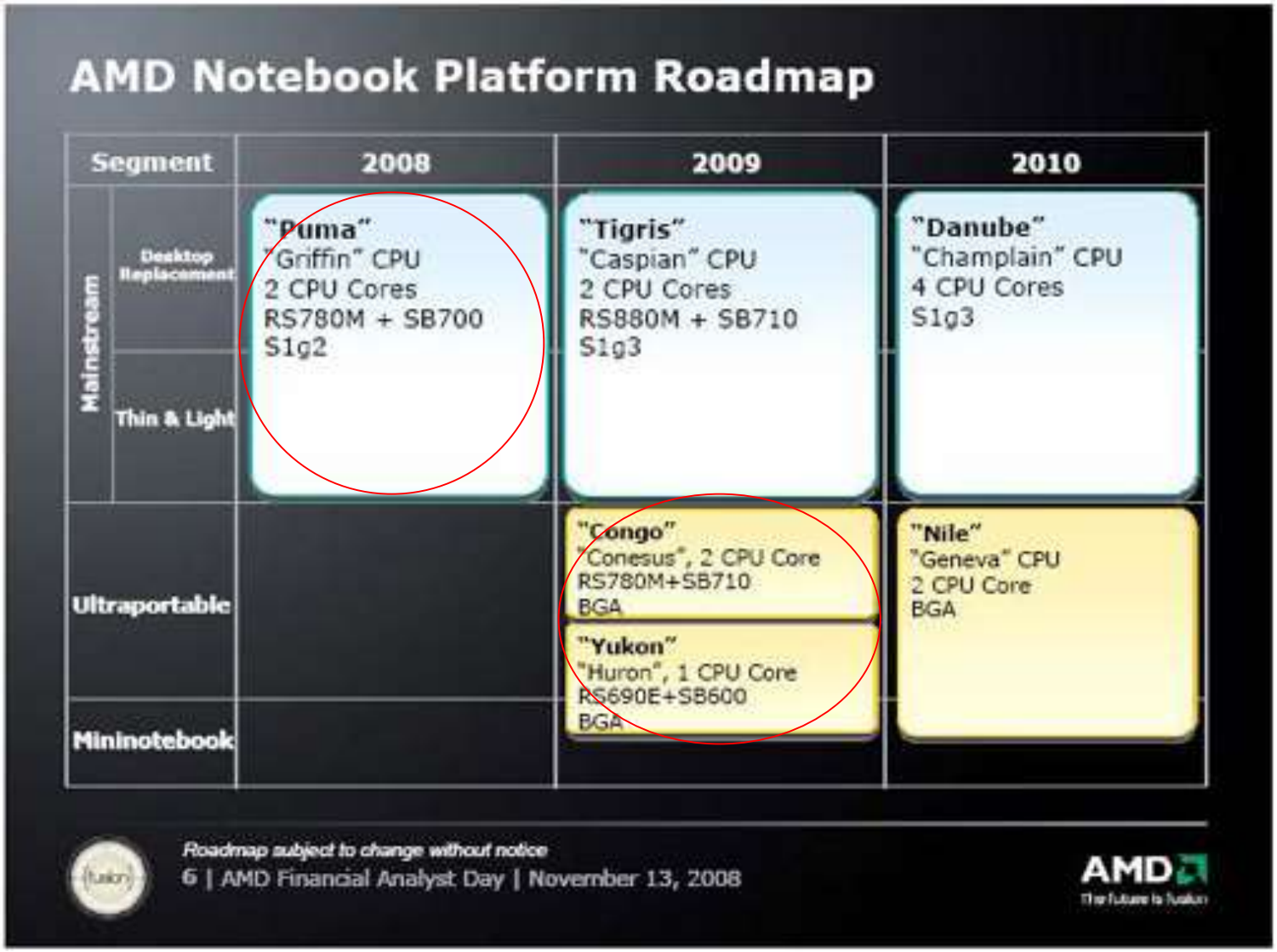


2.1 Overview of the 11h Griffin Family (4)

Brand names of Family 11h (Griffin)-based mobile lines

	Launched in	2008-2009	2011
		Family 11h (Griffin)	**Family 12h (Llano)**
Servers	**4P servers**		
	2P servers		
	1P servers		
	(85-140 W)		
Desktops	**High perf.** (~95-125 W)		
	Mainstream (~65-100 W)		Llano A8/A6/A4/E2 Sempron X2
	Entry level (40-60 W)		
Notebooks	**High perf.** (~30-60 W)	Turion X2 Ultra (ZM-xx) Turion X2 (RM-xx)	Llano A8 M
	Mainstream/Entry (~20-30 W)	Athlon X2 (QL-xx) Sempron (SI-xx)	Llano A6/A4/E2 M
	Ultra portable (~10-15 W)	Turion Neo X2 (L6xx) Turion X2 (RM-xx) Athlon Neo X2 (L3xx) Sempron (200U/210U)	
Tablet (~5 W)			
Embedded (~10 – 20 W)		Turion Neo X2 (L6xx) Athlon Neo X2 (L3xx) Sempron (200U/210U)	

Use of the 11h Griffin-based mobile lines in AMD's mobile platforms [5]



2.1 Overview of the 11h Griffin Family (6)

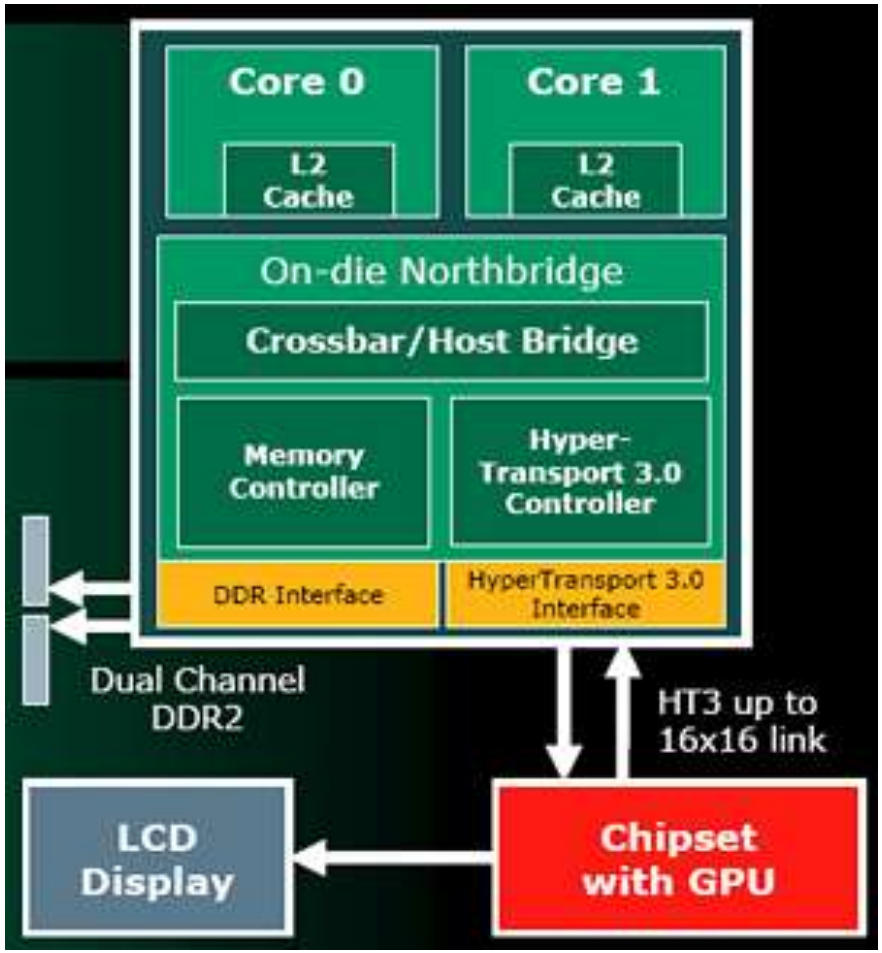
Main features of AMD's 11h Griffin-based high performance Turion Ultra mobile line

Base arch./ stepping		Intro	High perf. mobile family	Series	Techn.	Core count (up to)	L2 (up to)	L3	Memory (up to)	HT/ dir. (up to)	Sock et
K8	C0, CG	9/2003	Claw-hammer	Mobile Athlon 64	130 nm	1	512 KB	-	DDR-400	HT 1.0: 3.2 GB/s	754
	E5	3/2005	Lancaster	Turion 64	90 nm	1	1 MB	-	DDR-400	HT 1.0: 3.2 GB/s	754
	F2	5/2006	Trinidad	Turion 64 X2	90 nm	2	2*½ MB	-	DDR2-667	HT 1.0: 3.2 GB/s	S1
K10.5	DA-C2	9/2009	Caspian	Turion II	45 nm	2	2*½ MB/ 2*1 MB[1]	-	DDR2-800	HT 3.0: 7.2 GB/s	S1g3
	DA-C3	5/2010	Champlain	Turion X4	45 nm	4	4*½ MB	-	DDR3-1066	HT 3.0: 7.2 GB/s	S1g4
Fam. 11 (Griffin)	B1	6/2008	Lion	Turion X2 Ultra	65 nm	2	2x½ MB/ 2*1 MB[2]	-	DDR2-800	HT 3.0: 10.4 GB/s	S1g2
Fam. 12 (Llano)	B0	6/2011	Llano APU	Fusion A8	32 nm	4	4x1 MB	-	DDR3-1600	-	FM1
Family 15h Mod. 10h-1Fh (Piledriver)		5/2012	Trinity APU	A10-A4 M	32 nm	2 CM (4C)	2 MB/CM	-	DDR3-1600	PCIe 2.0x16 UMI	FS1r2
Family 15h Mod. 20h-2Fh (Piledriver)		2/2013	Richland APU	A10-A4 M	32 nm	2 CM (4C)	2 MB/CM	-	DDR3-1866	PCIe 2.0x16 ???UMI	FS1r2
Family 16h (Jaguar)		H1/2013	Kabini APU (SOC)	A/E Series	28 nm	2 CM (4C)	2 MB shared	-	DDR3-1866	PCIe ???	BGA

[1]: 2*512 KB for Turion II, 2*1 MB for Turion II Ultra
[2]: 2*512 KB for Turion X2, 2*1 MB for Turion X2 Ultra

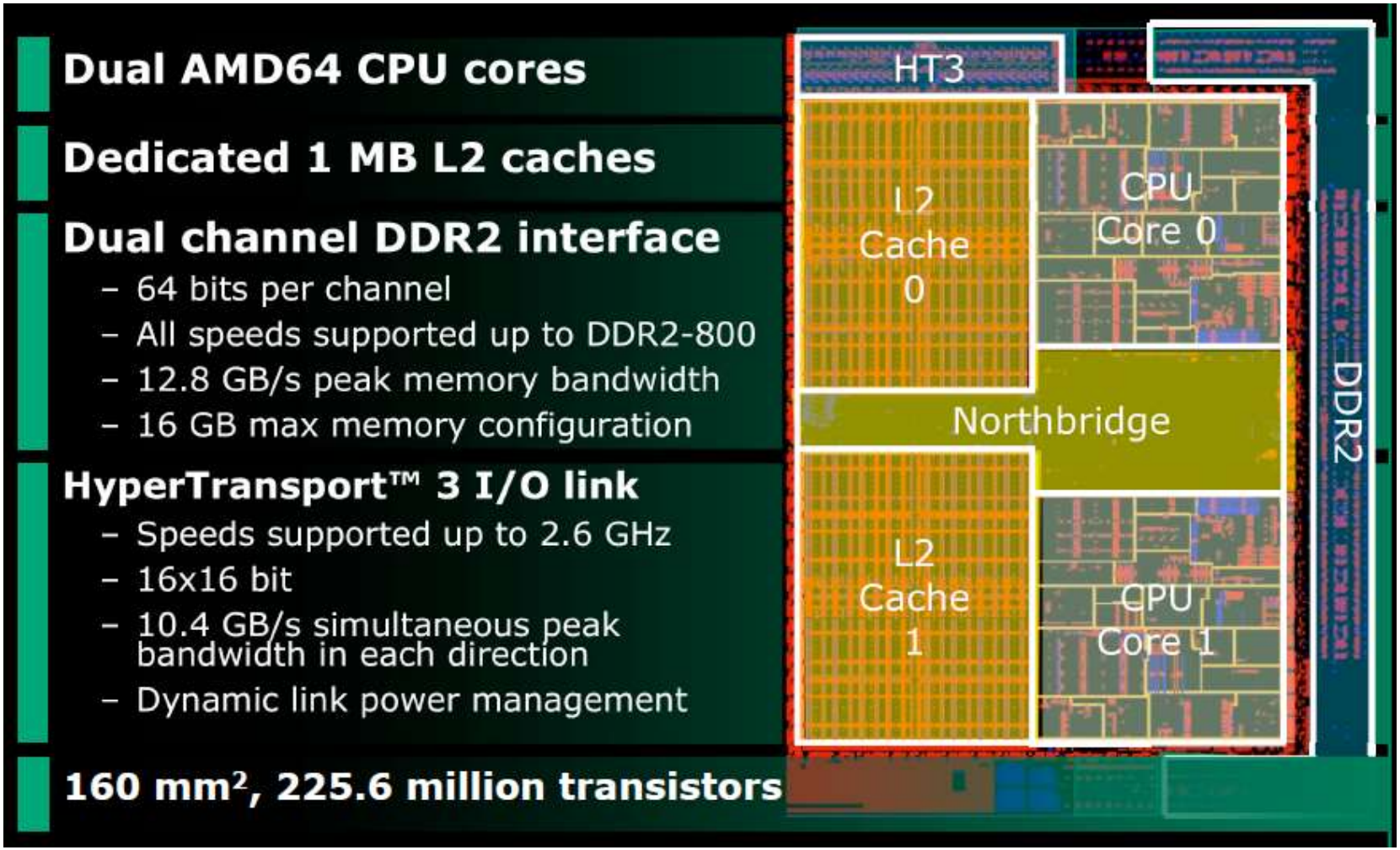
UMI: Universal Media Interface

Block diagram of Griffin [29]



2.2 Main enhancements of the 11h Griffin Family

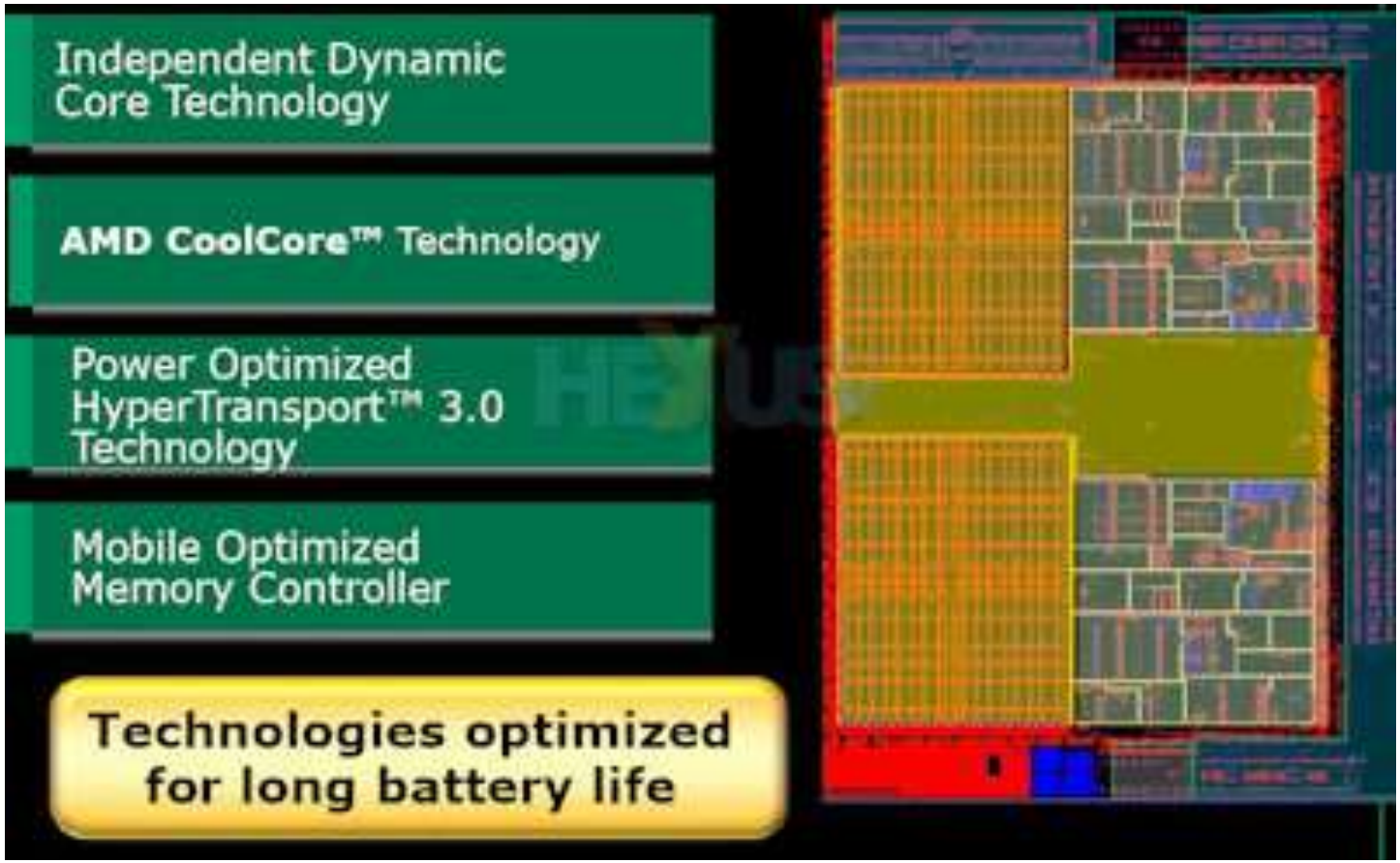
2.2 Main enhancements of the 11h Griffin Family [3]



2.2 Main enhancements of the 11h Griffin Family (2)

Main power saving techniques used in Griffin [6]

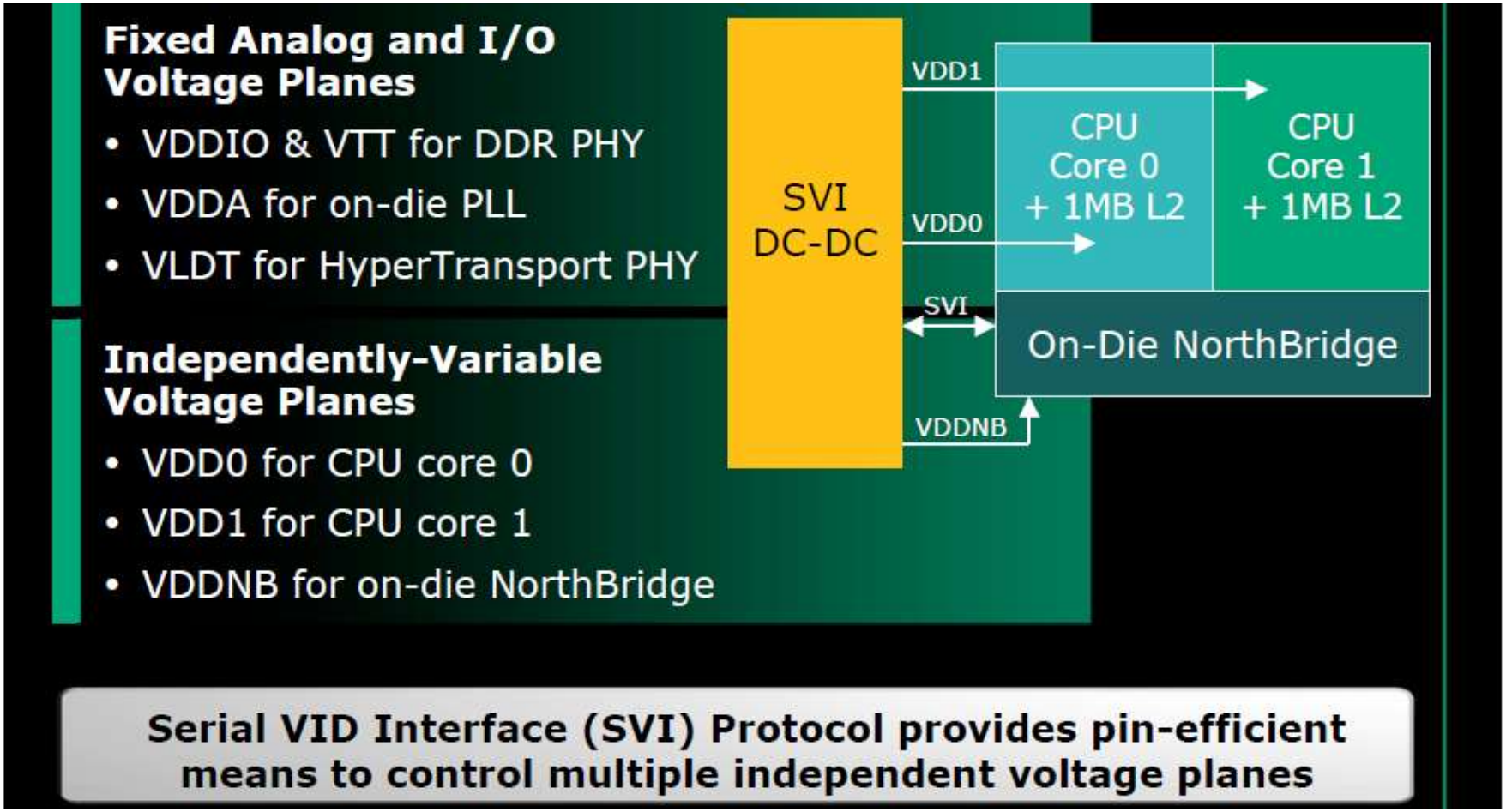
Cool'n'Quiet 2.0 (as introduced into then K10 Barcelona-based desktops (Phenom line) with a few enhancements intended for mobile use



2.2 Main enhancements of the 11h Griffin Family (3)

a) Independent Dynamic Core Technology

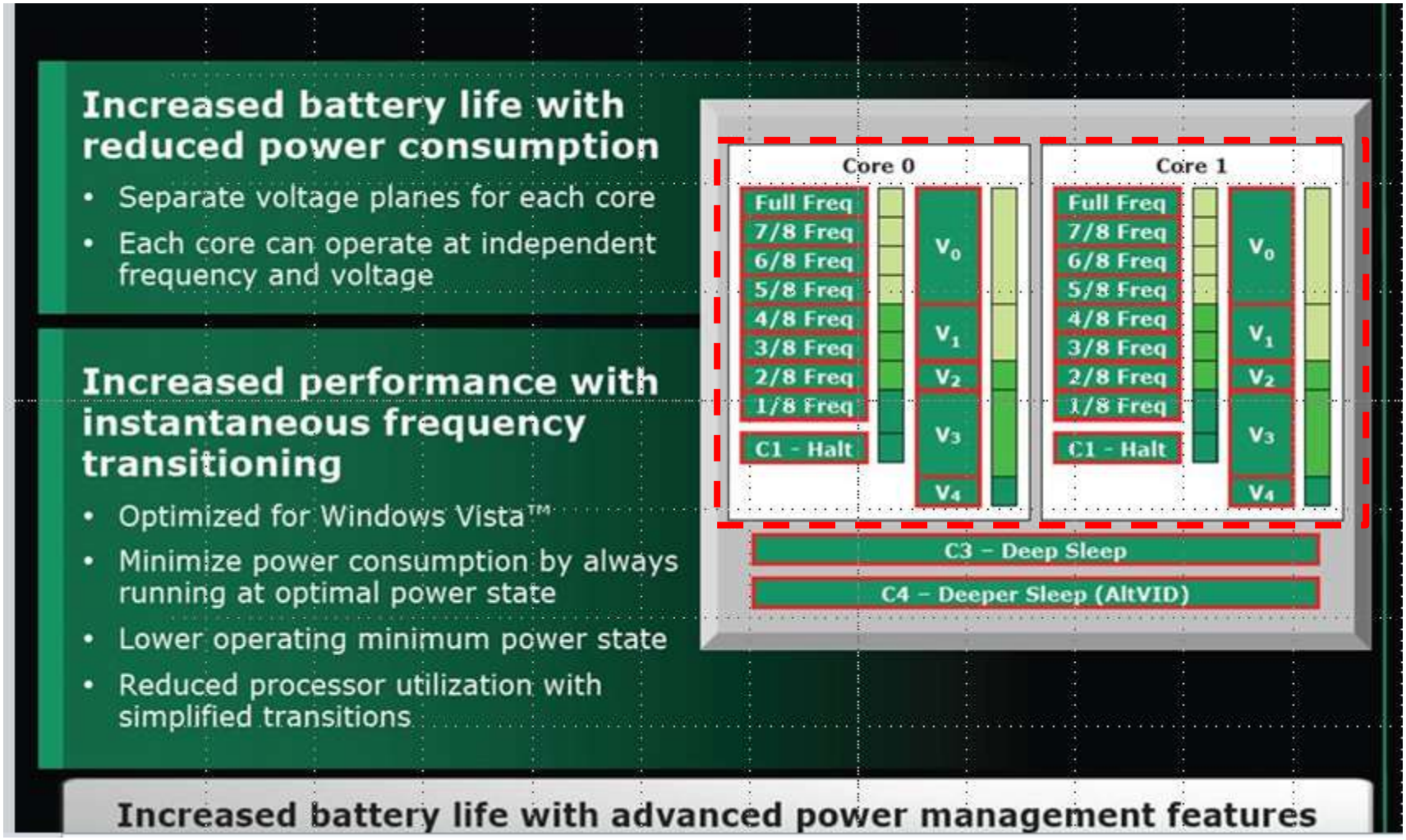
It means both separate voltage planes and clock domains [3]



2.2 Main enhancements of the 11h Griffin Family (4)

Number of available frequency and voltage levels [28]

There are up to 8 frequeny levels and 4 voltage levels available for each core.



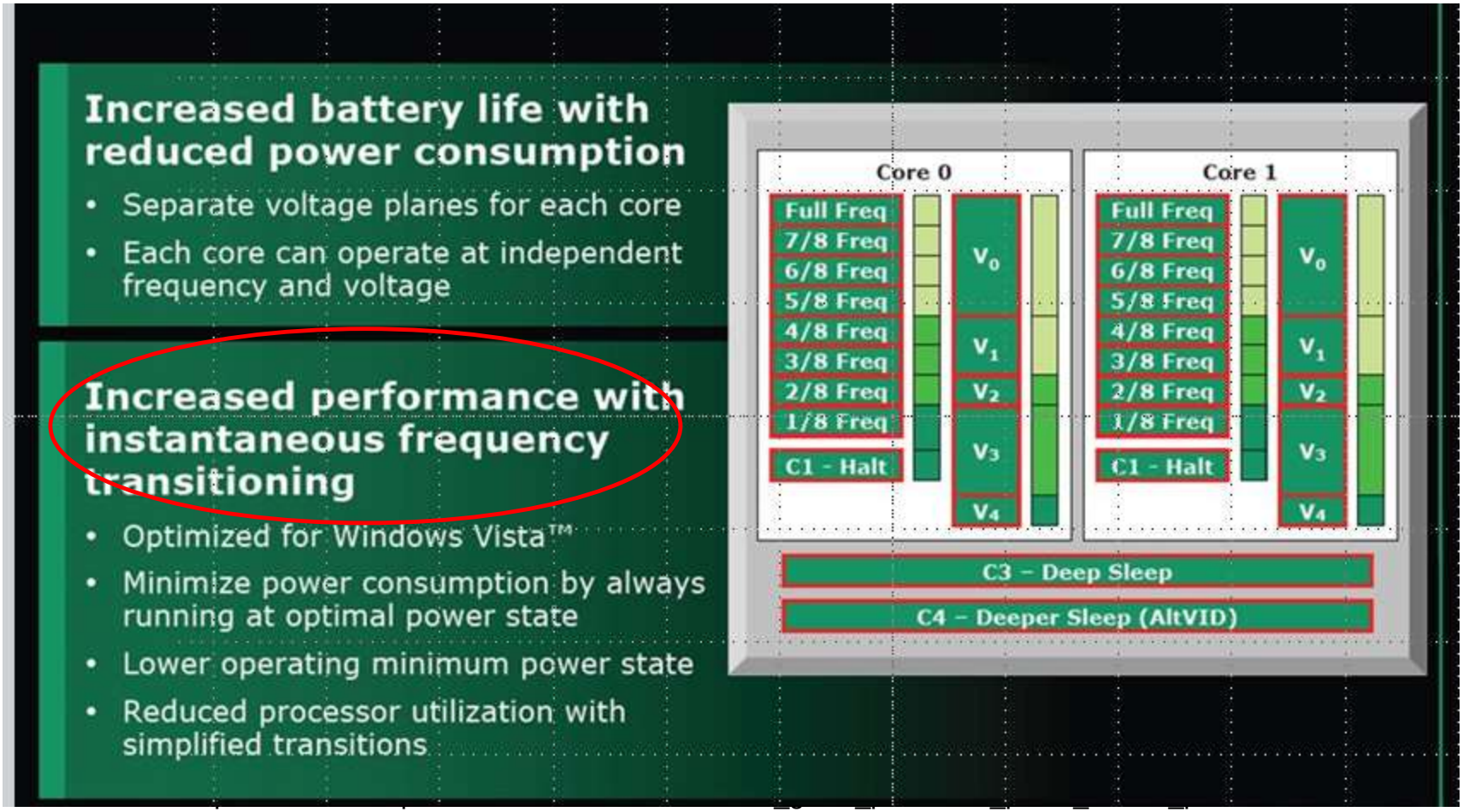
2.2 Main enhancements of the 11h Griffin Family (5)

Instantaneous frequency transitions [28]

Achieved with a single shared high-speed PLL and programmable dividers for each core.

The PLL frequency is fixed at the part's maximum frequency.

The dividers divide the maximum frequency by n/2, where n is any integer of a given set [30].



2.2 Main enhancements of the 11h Griffin Family (6)

Percentage power savings resulting from iindependent core voltage and frequency planes [30]

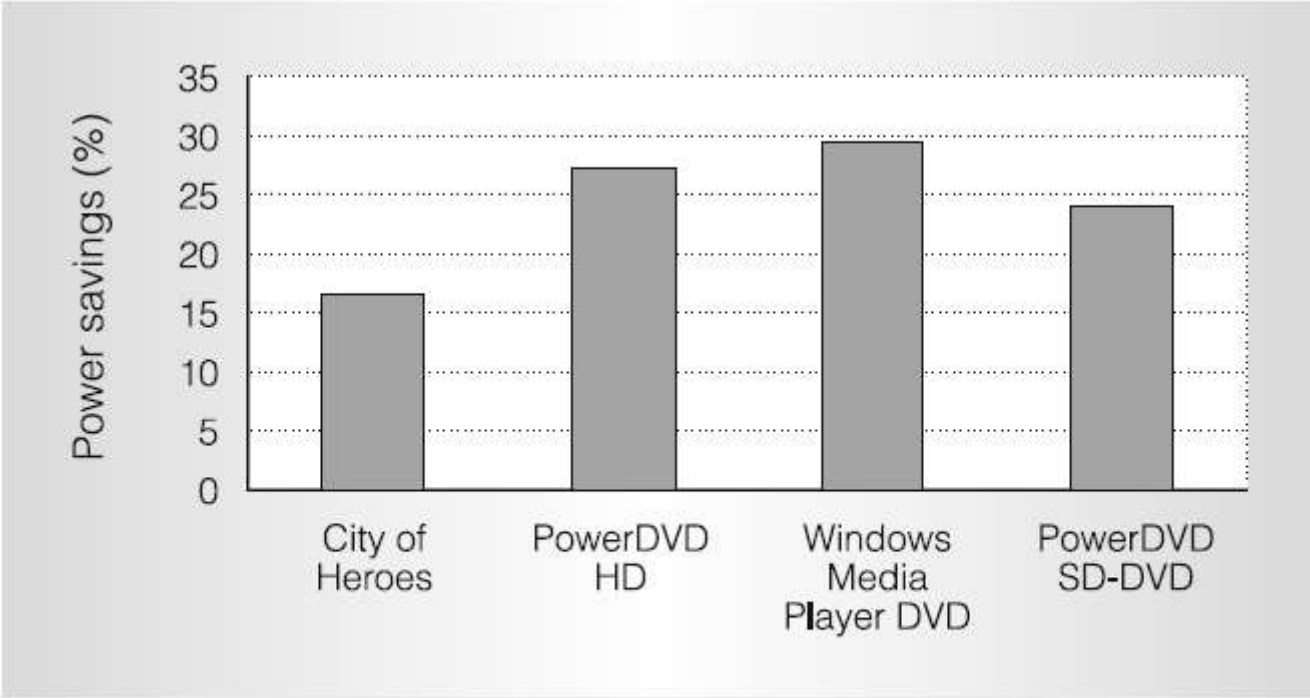


Figure 4. Griffin's percentage power savings resulting from independent CPU voltage and frequency planes.

2.2 Main enhancements of the 11h Griffin Family (7)

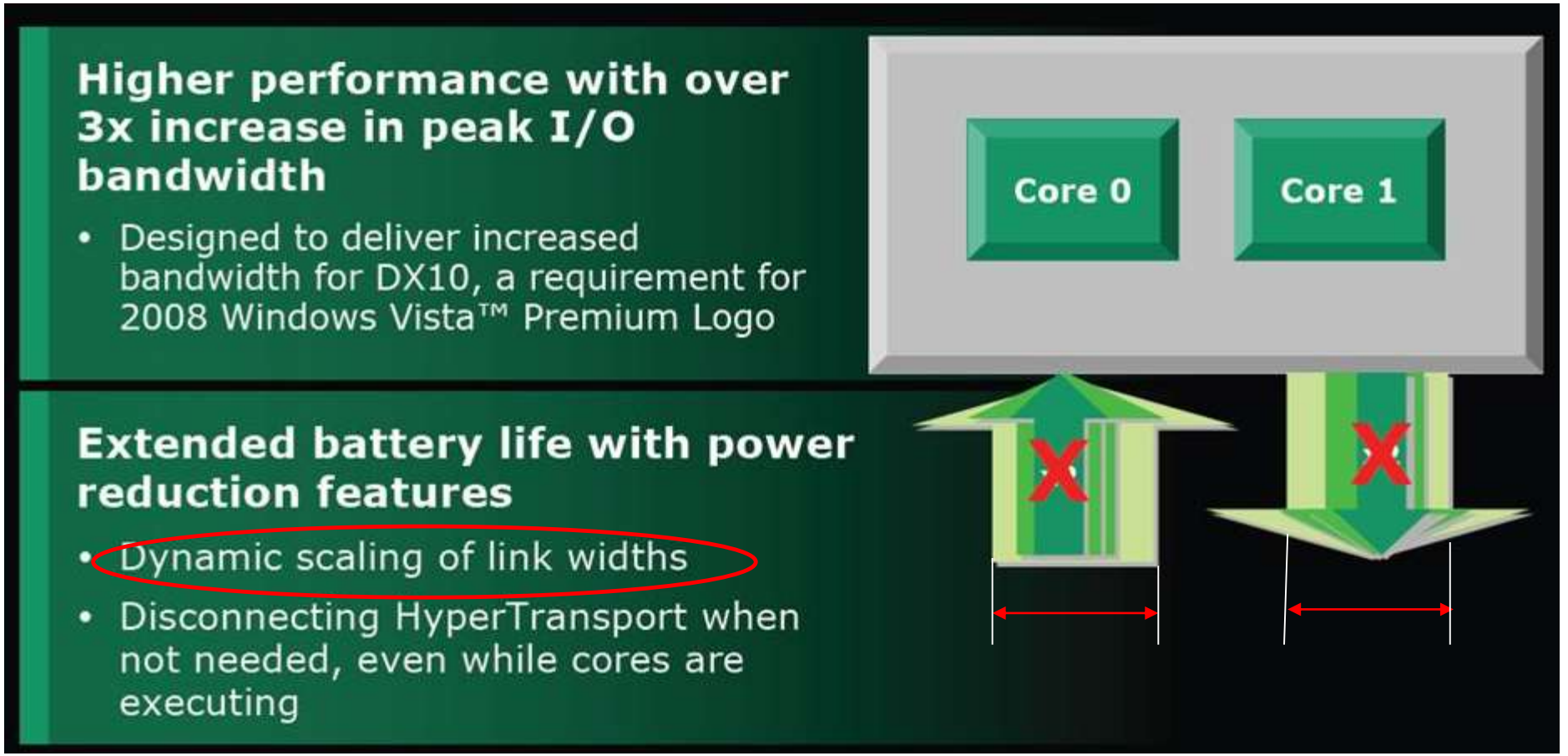
b) CoolCore Technology

- Introduced already in K10 Barcelona-based processors (2007).
- It turns off blocks of logic (e.g. execution units) if not in use in order to save power.

2.2 Main enhancements of the 11h Griffin Family (8)

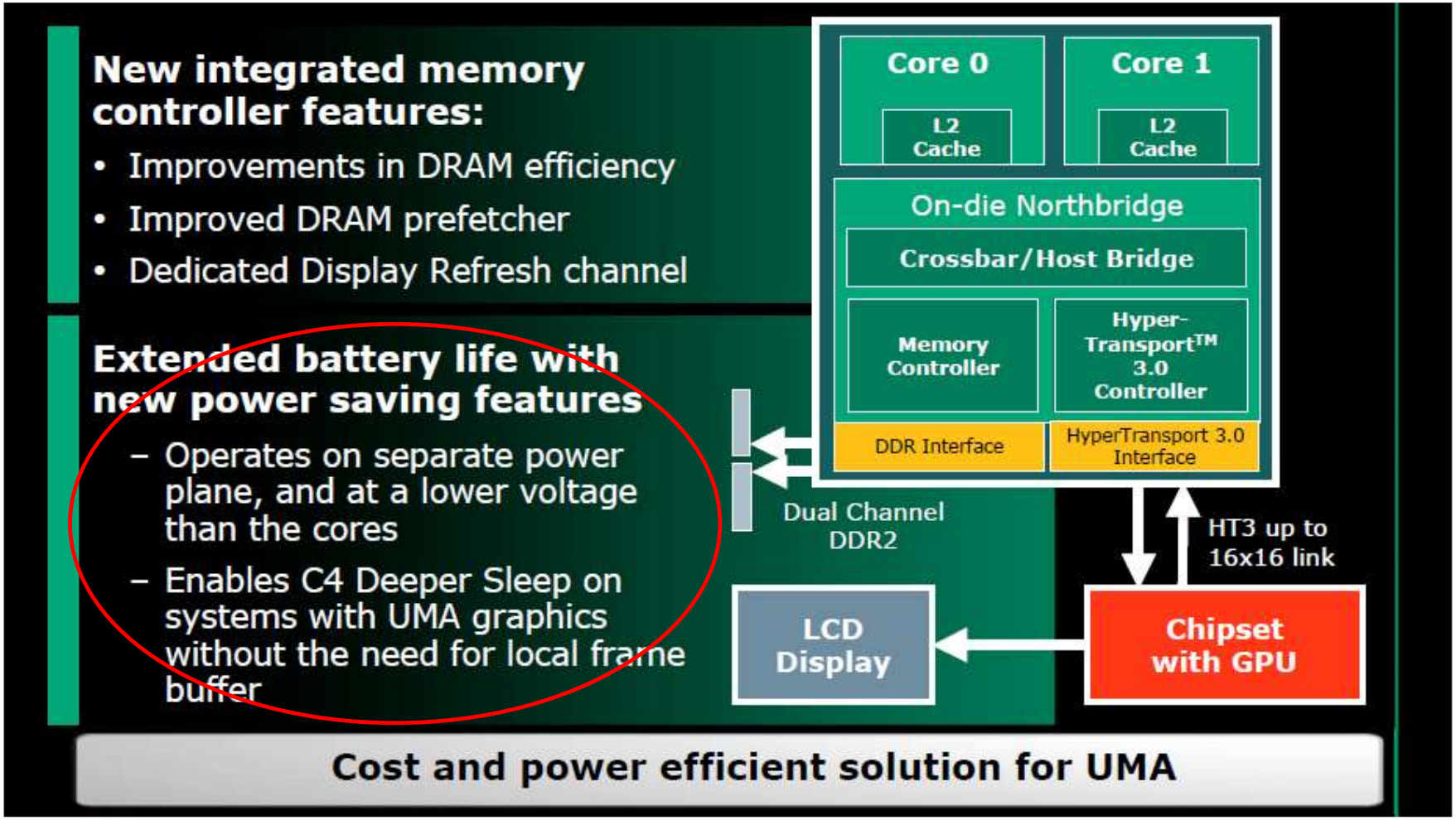
c) Power optimized HT 3.0 [28]

Dynamic scaling of HT link width down to 0-bit ("disconnected") in both directions from and to the chipset.



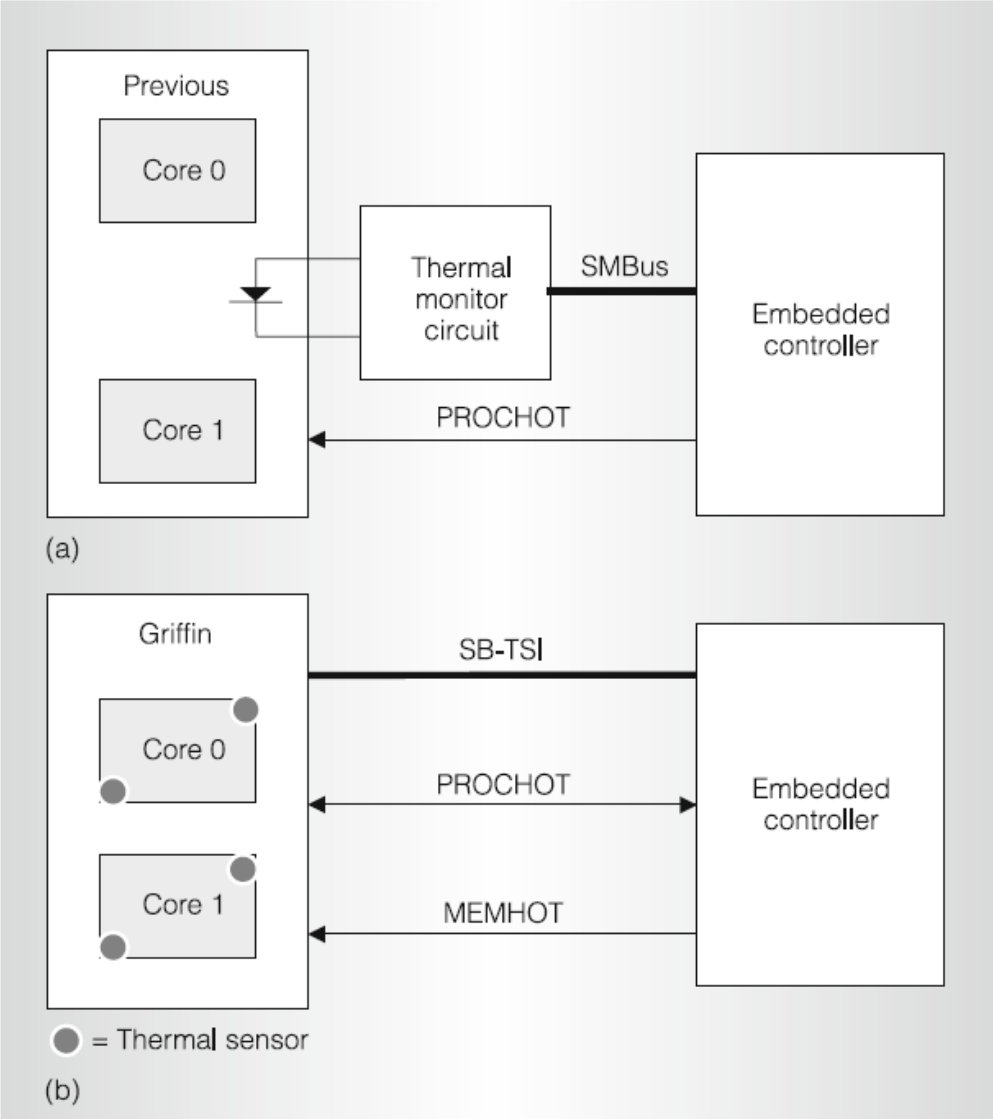
2.2 Main enhancements of the 11h Griffin Family (9)

d) Mobile optimized Memory Controller [28]



2.2 Main enhancements of the 11h Griffin Family (10)

e) Multi-point on-die thermal sensors on the Griffin die [30]



Single on-die thermal diode

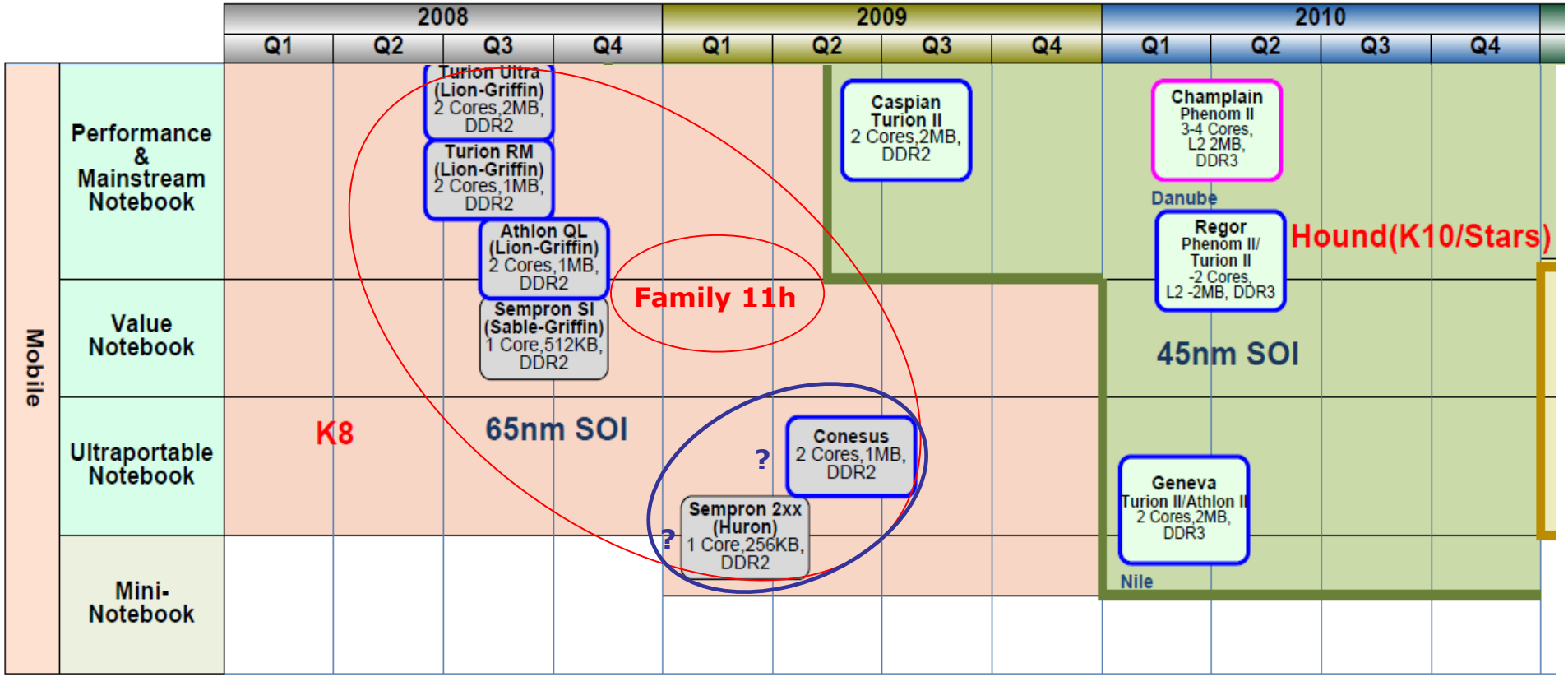
PROCHOT: Processor overtemperature condition

SB-TSI: SideBand Thermal Sensor Interface bus (provides a subset of the SMBus functionality)

Multiple on-die thermal sensors

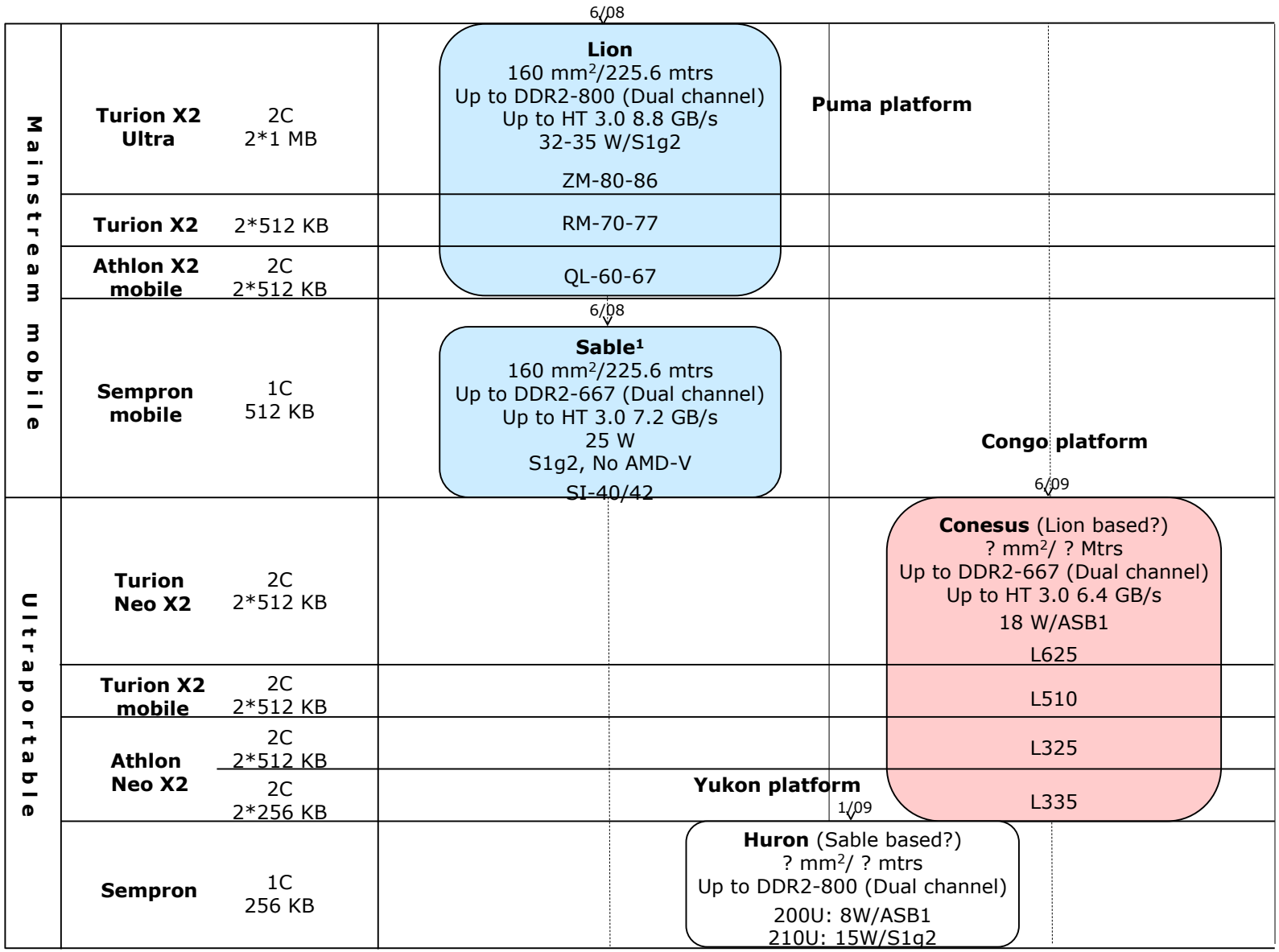
2.3 The 11h Griffin mobile lines

2.3 The 11h Griffin mobile lines



2.3 The 11h Griffin mobile lines (2)

AMD's Family 11h mobile lines – Overview-2



[1] One core disabled

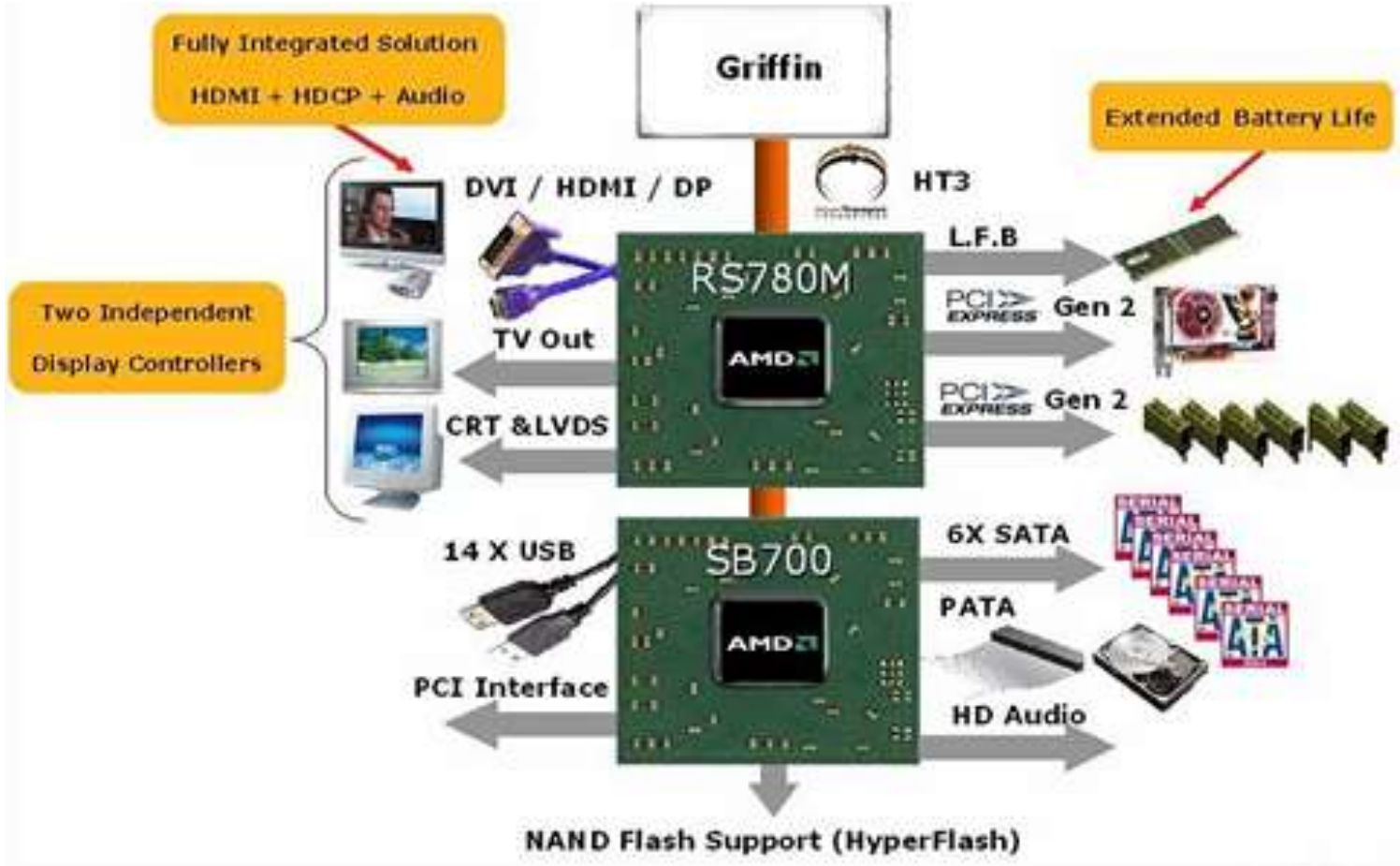
2.3 The 11h Griffin mobile lines (3)

Example: Main features of the Lyon-based Turion X2 Ultra ZM-8x line [1]

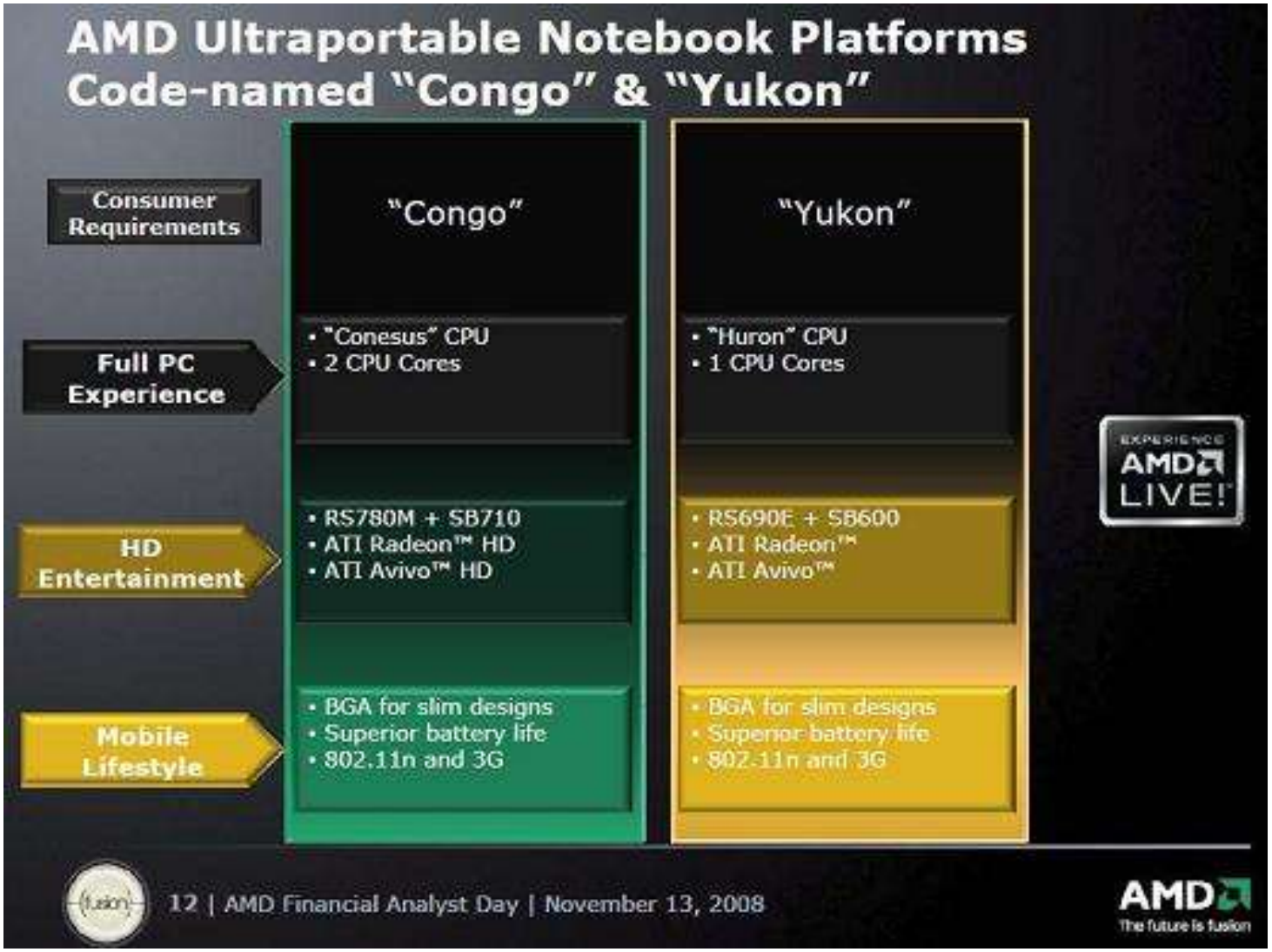
Model Number	Frequency	L2-Cache	HT	Multiplier[1]	Voltage	TDP	Socket	Release date
Turion X2 Ultra ZM-80[2]	2100 MHz	2 × 1 MB	1800 MHz	10.5x	0.75V-1.2V	32 W	Socket S1G2	June 4, 2008
Turion X2 Ultra ZM-82[2]	2200 MHz	2 × 1 MB	1800 MHz	11x	0.75V-1.2V	35 W	Socket S1G2	June 4, 2008
Turion X2 Ultra ZM-84[2]	2300 MHz	2 × 1 MB	1800 MHz	11.5x	0.75V-1.2V	35 W	Socket S1G2	Q3 2008
Turion X2 Ultra ZM-85[2]	2300 MHz	2 × 1 MB	2200 MHz	11.5x	0.75V-1.2V	35 W	Socket S1G2	Q3 2008
Turion X2 Ultra ZM-86[2]	2400 MHz	2 × 1 MB	1800 MHz	12x	0.75V-1.2V	35 W	Socket S1G2	June 4, 2008
Turion X2 Ultra ZM-87[2]	2400 MHz	2 × 1 MB	2200 MHz	12x	0.75V-1.2V	35 W	Socket S1G2	Q3 2008
Turion X2 Ultra ZM-88[2]	2500 MHz	2 × 1 MB	1800 MHz	12.5x	0.75V-1.2V	35 W	Socket S1G2	Q3 2008

2.3 The 11h Griffin mobile lines (4)

The Puma platform [29]



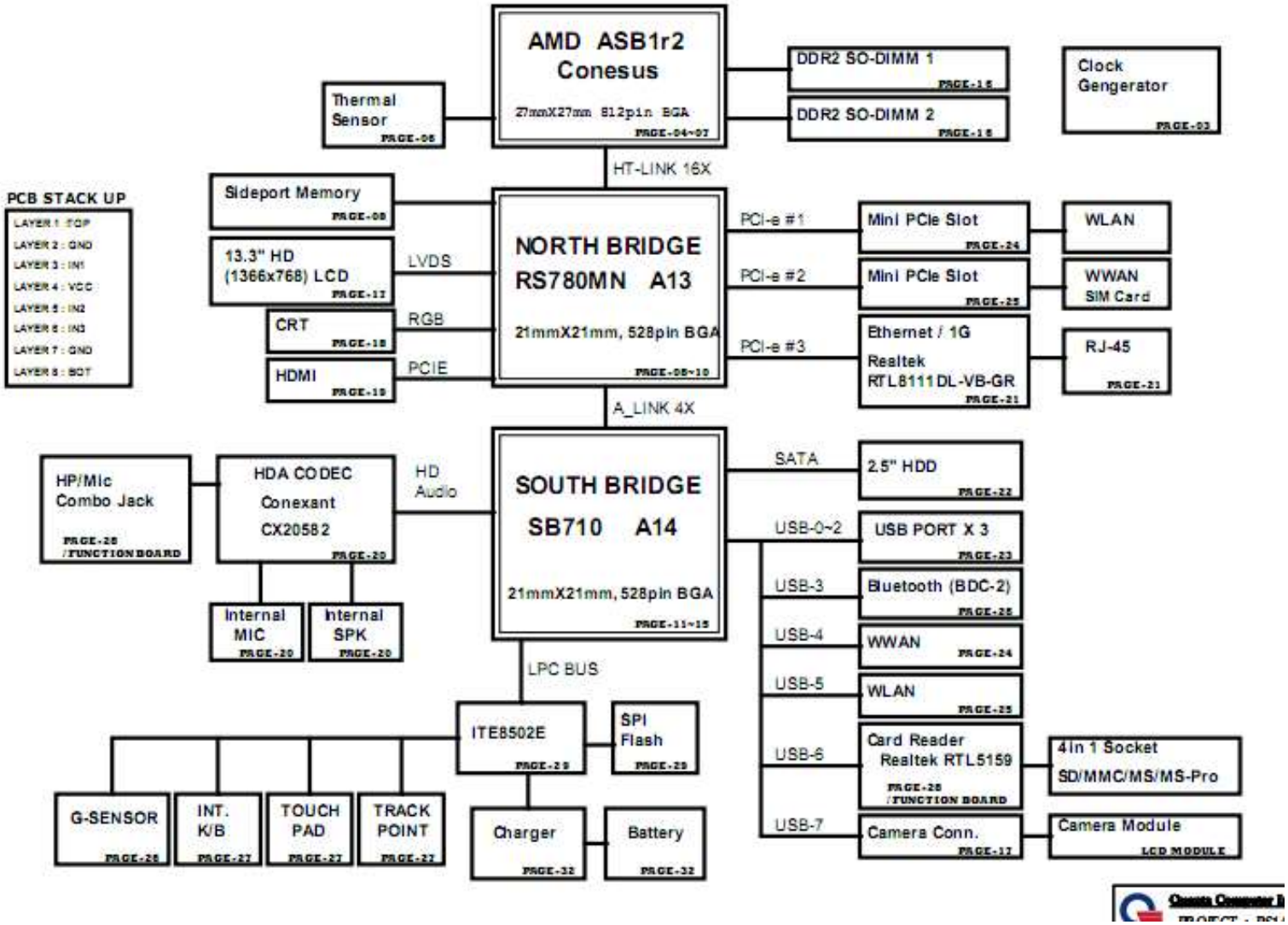
Overview of the Congo and Yukon platforms [31]



2.3 The 11h Griffin mobile lines (6)

Example for the Conesus-based Congo platform

Block diagram of the Lenovo ThinkPad Edge 0221-RY6 notebook [32]



2.3 The 11h Griffin mobile lines (7)

Remark

There are no detailed specifications available for the Huron and Conesus processors as far to decide whether they are Griffin-based or not.
Nevertheless, it can be assumed that the ultra portable notebooks aimed

- Conesus (2C, 2x512 KB, 18 W) and
- Huron (1C, 256 KB, 8-15 W)

processors are lower clocked downsized versions of the value notebook aimed

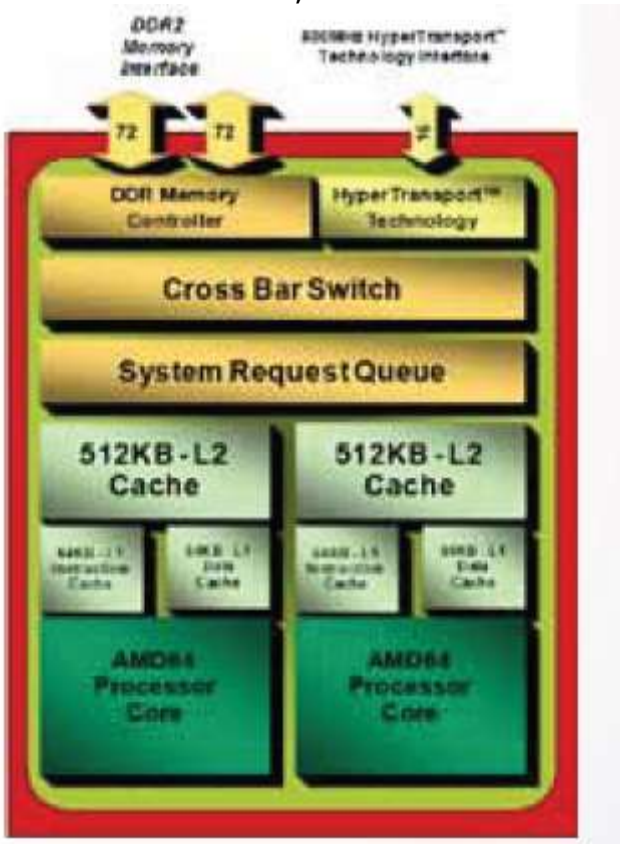
- Lion (Athlon X2 mobile QL 6x (2C, 2x512 KB, 35 W) and
- Sable (1C, 512 KB, 25 W)

processors.

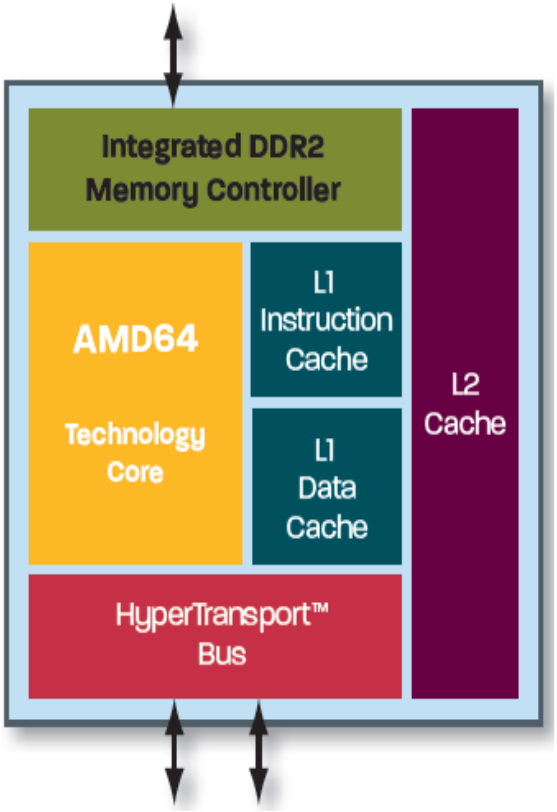
2.3 The 11h Griffin mobile lines (8)

Block diagrams of the Conesus and Huron dies

Conesus [8]
2C, 2x512 KB
DDR2-667 Dual channel
HT 3-0 up to 6.4 GB/s
18 W, ASB1



Huron [7]
1C, 256 KB
DDR2-800 Single Channel
HT 3.0 up to 6.4 GB/s
8/15W, ASB1/S1g2



3. The 12h Llano Family

- 3.1 Introduction to the 12h Llano Family
- 3.2 The microarchitecture of the Family 12h Llano lines
- 3.3 Microarchitecture enhancements aiming at increasing performance
- 3.4 Microarchitecture enhancements aiming at reducing power consumption
- 3.5 Family 12h (Llano)-based Fusion desktop lines
- 3.6 AMD's Family 12h (Llano)-based Fusion mobile lines

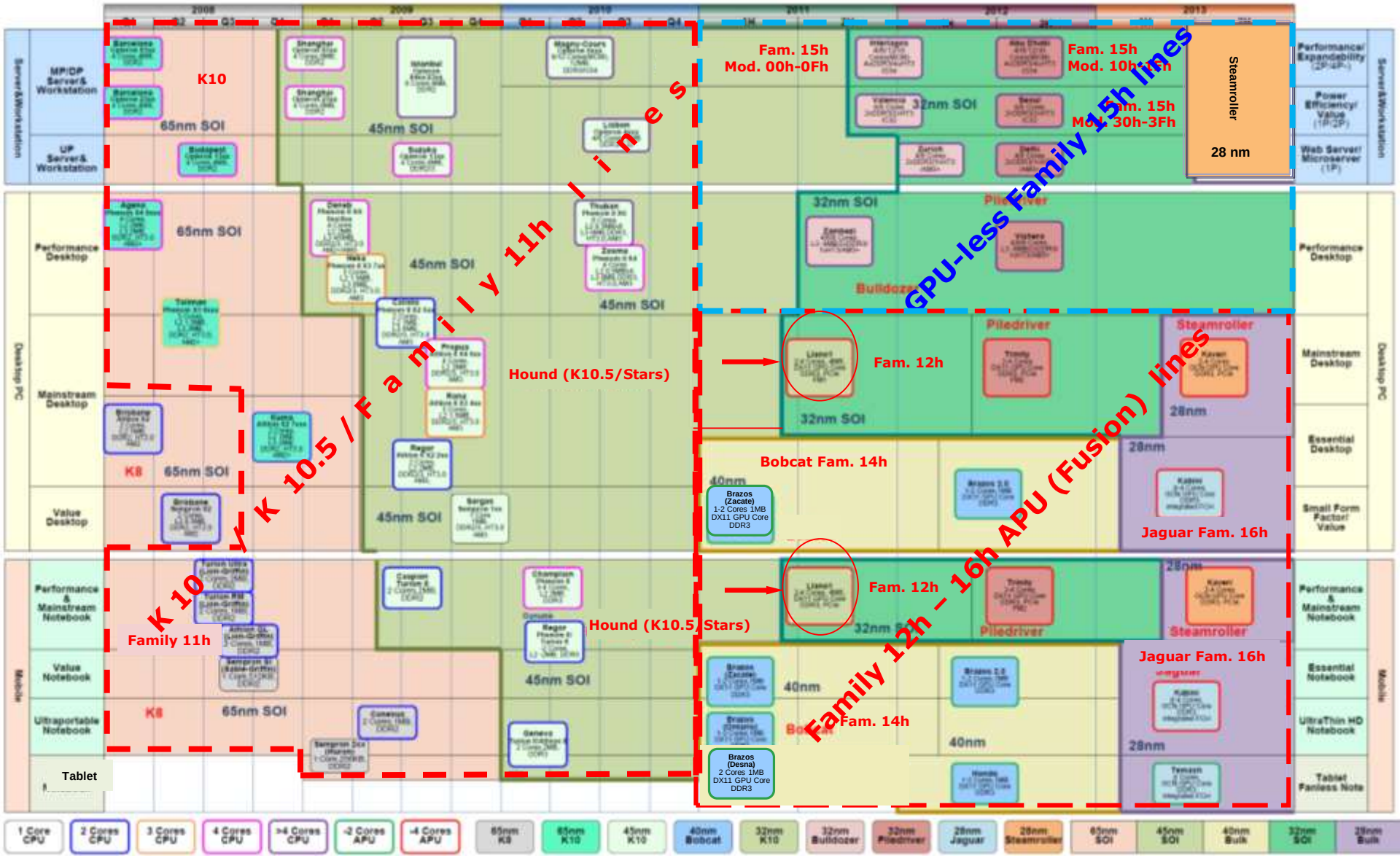
3.1 Introduction to the 12h Llano Family

3.1 Introduction to the 12h Llano Family [4]

- Introduced: 6/2011.
- This processor family belongs to the Fusion APU (Accelerated Processing Unit) series.
  The Fusion APU series include two to four x86 CPUs and a GPU to accelerate vision computing (graphics and media).
- Family 12h Llano processors do not include an L3 cache, but typically a GPU.
- Family 12h Llano covers desktop and mobile lines, as shown later.
- Processors of the Llano lines have up to 4 CPU cores and a GPU.
  Nevertheless, AMD sells Llano based desktop lines as well with disabled GPUs.
  These lines are branded as Athlon II X4/X2 or Sempron lines.
- 32 nm technology, 228 mm^2, 1450 mtrs.

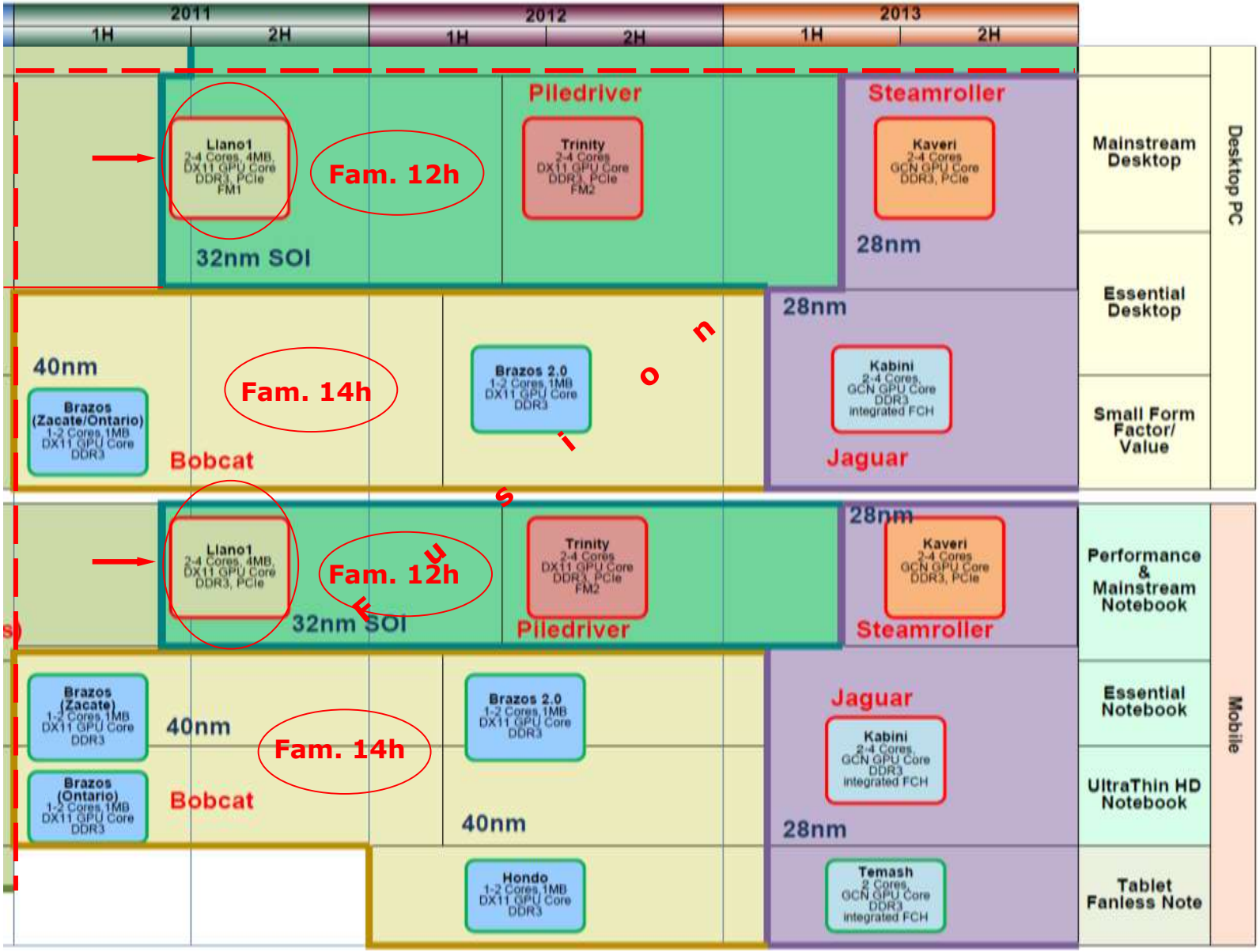
3.1 Introduction to the 12h Llano Family (2)

Overview of AMD's K10 - Family 16h based processor lines [2]



3.1 Introduction to the 12h Llano Family (3)

AMD's Family 12h Llano-based desktop and mobile lines – Overview-2 [2]



3.1 Introduction to the 12h Llano Family (4)

Brand names of Family 12h (Llano)-based desktop and notebook lines

	Launched in	2008-2009	2011
		Family 11h (**Griffin**)	**Family 12h** (**Llano**)
Servers	**4P servers**		
	2P servers		
	1P servers		
	(85-140 W)		
Desktops	**High perf.** (~95-125 W)		
	Mainstream (~65-100 W)		Llano A8/A6/A4/E2 Sempron X2
	Entry level (40-60 W)		
Notebooks	**High perf.** (~30-60 W)	Turion X2 Ultra (ZM-xx) Turion X2 (RM-xx)	Llano A8 M
	Mainstream/Entry (~20-30 W)	Athlon X2 (QL-xx) Sempron (SI-xx)	Llano A6/A4/E2 M
	Ultra portable (~10-15 W)	Turion Neo X2 (L6xx) Turion X2 (RM-xx) Athlon Neo X2 (L3xx) Sempron (200U/210U)	
Tablet (~5 W)			
Embedded (~10 – 20 W)		Turion Neo X2 (L6xx) Athlon Neo X2 (L3xx) Sempron (200U/210U)	

3.1 Introduction to the 12h Llano Family (5)

K12 (Llano)-based processor lines – Overview-3 [11]

Llano line

Desktop/mobile Fusion APU models

- *Lynx desktop platform (65/100 W)*

  Fusion A/E2 series *(6/2011-12/2011)*
  2/4 C, 512 KB/1 MB per C, GPU, 65/100 W

  Turbo Core on select desktop models

- *Sabine mobile platform (35-45 W)*

  Fusion A/E2 M/MX series *(6/2011-12/2011)*
  2/3/4 C, 512 KB/1 MB L2 per C, GPU, 35/45 W

  Turbo Core on all mobile models

GPU-less desktop models

Lynx desktop platform (65/100 W)

- ***Athlon II X4 6xx****, (8/2011- 2/2012)*
  4C, 1 MB/C, 65/100 W
- ***Athlon II X2 221****, (8/2011)*
  2C, 512 KB/C, 65 W
- ***Sempron 198****, /8/2011)*
  2C, 512 KB/C, 65 W

GPU disabled, no Turbo Core

Socket FM1

3.1 Introduction to the 12h Llano Family (6)

The Vision branding [4]

Desktop and mobile lines based on Fusion APUs are categorized into four Vision brands according to their MM and graphics capabilities (E2, A4, A6 and A8 series) as follows:

- E2 series
  Skip-free HD-playback (1080p High-Definition smooth playback)
- A4 series
  Easy photo editing
- A6 series
  Fast video editing
- A8 series
  Ultra-realistic 3D gaming

3.1 Introduction to the 12h Llano Family (7)

Example: AMD's Llano-based A-series mobile lines [9]

35W Model	x86 Cores	L2 Total	Radeon™ Cores	Base Frequency	Boost Frequency
A8	4	4 MB	400	1.5 GHz	2.4 GHz
A6	4	4 MB	320	1.4 GHz	2.3 GHz
A4	2	2 MB	260	1.9 GHz	2.5 GHz

3.1 Introduction to the 12h Llano Family (8)

Remark [10]

In fact, AMD introduced the Vision branding already in 2009 to characterize the visual capabilities of their mainstream laptops, by differentiating between

- Vision Basic
- Vision Premium
- Vision Ultimate and
- Vision Black

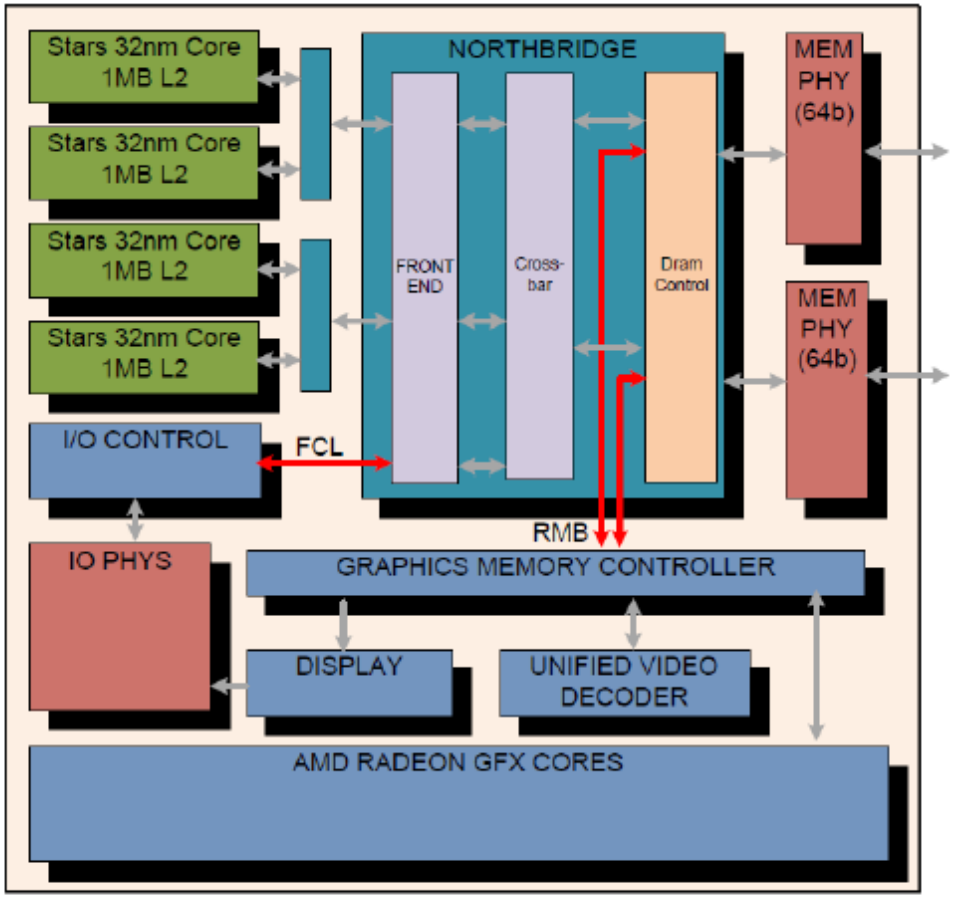
branding.

To avoid consumer confusion AMD redefined their Vision branding in 6/2011, along with the introduction of the Llano based desktops and laptops, as stated above.

3.2 The microarchitecture of the Family 12h Llano lines

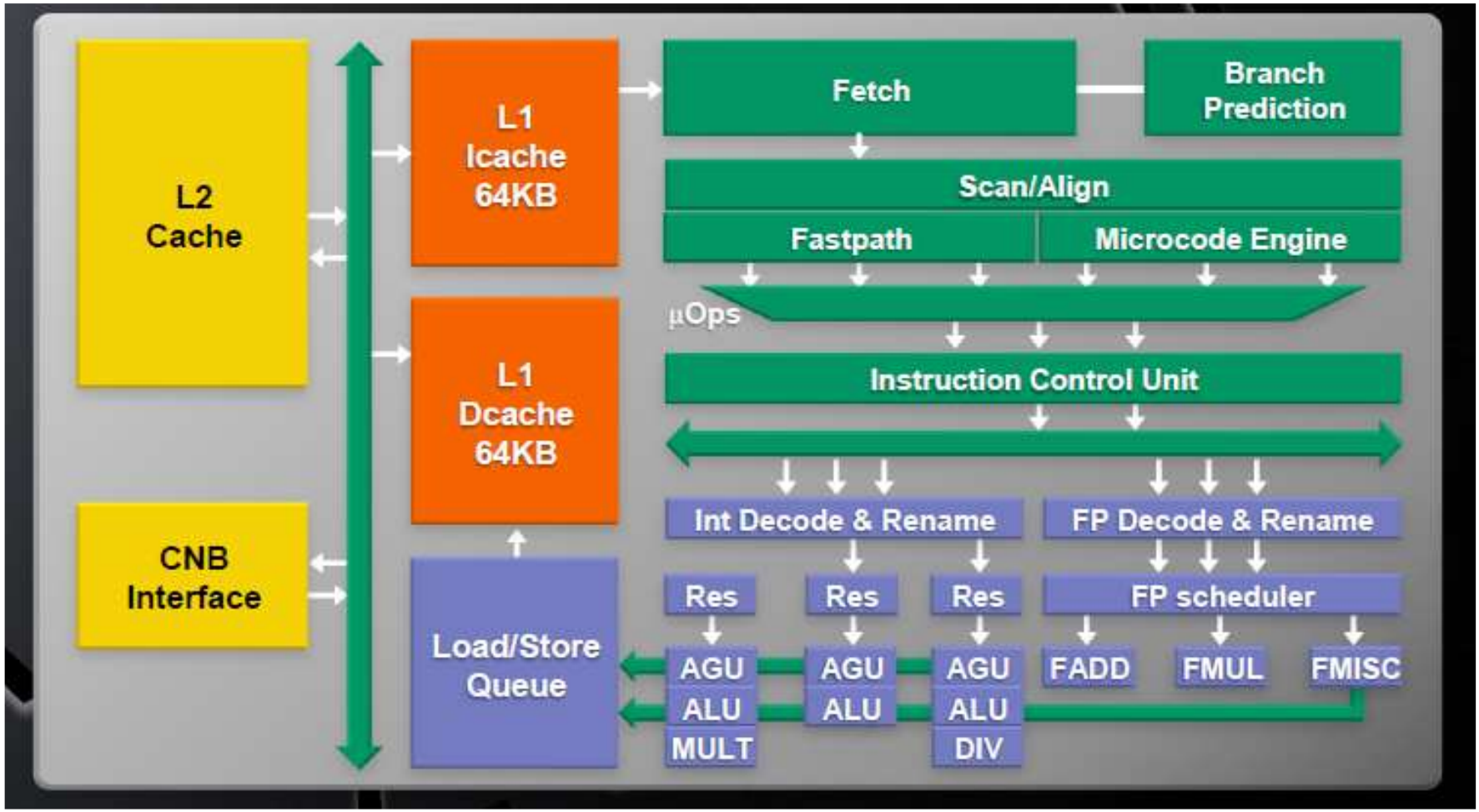
3.2 The microarchitecture of the Family 12h Llano lines [12]

- Up to 4 Stars-32nm x86 Cores
  - 1MB L2 cache/core
- Integrated Northbridge
- 2 Chan of DDR3-1866 memory
- 24 Lanes of PCIe® Gen2
  - x4 UMI (Unified Media Interface)
  - x4 GPP (General Purpose Ports)
  - x16 Graphics expansion or display
- 2 x4 Lanes dedicated display
- 2 Head Display Controller
- UVD (Unified Video Decoder)
- 400 AMD Radeon™ Compute Units
- GMC (Graphics Memory Controller)
- FCL (Fusion Control Link)
- RMB (AMD Radeon™ Memory Bus)
- 227mm^2, 32nm SOI
- 1.45BN transistors



3.2 The microarchitecture of the Family 12h Llano lines (2)

The microarchitecture of Llano's CPU cores [9]

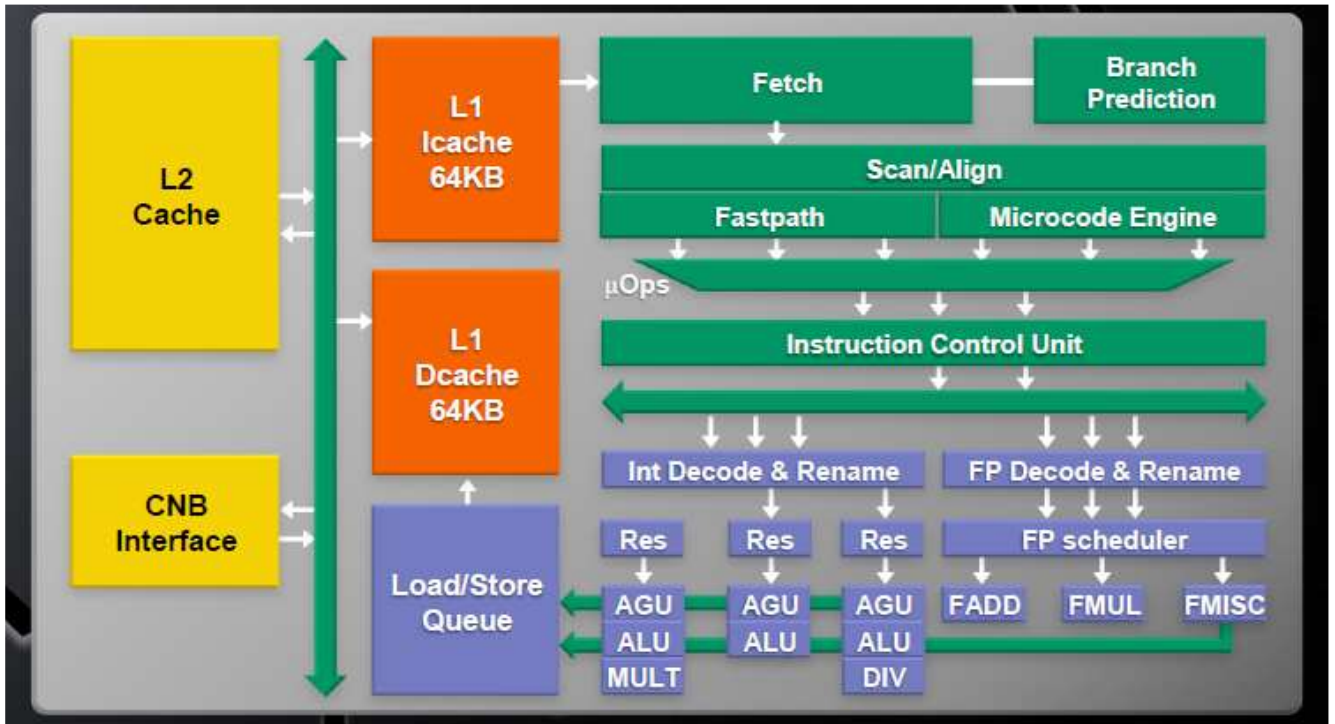


3.2 The microarchitecture of the Family 12h Llano lines (3)

The block diagram of the GPU [12]

3.2 The microarchitecture of the Family 12h Llano lines (4)

Core numbers in different Llano-based A-series mobile lines [9]

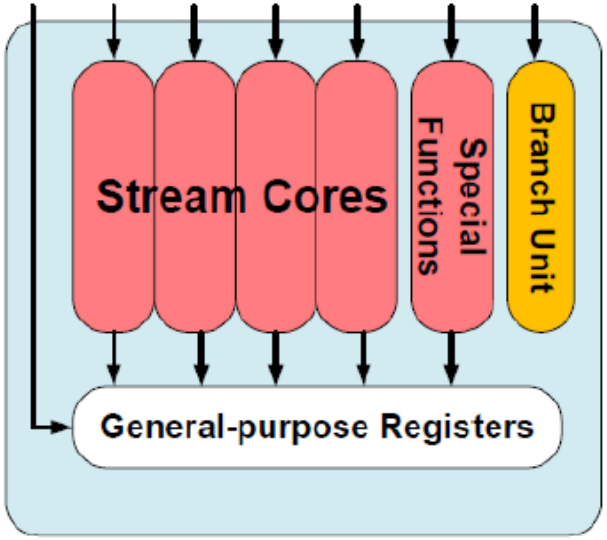


35W Model	x86 Cores	L2 Total	Radeon™ Cores	Base Frequency	Boost Frequency
A8	4	4 MB	400	1.5 GHz	2.4 GHz
A6	4	4 MB	320	1.4 GHz	2.3 GHz
A4	2	2 MB	260	1.9 GHz	2.5 GHz

3.2 The microarchitecture of the Family 12h Llano lines (5)

The AMD Radeon VLIW-5 core [12]

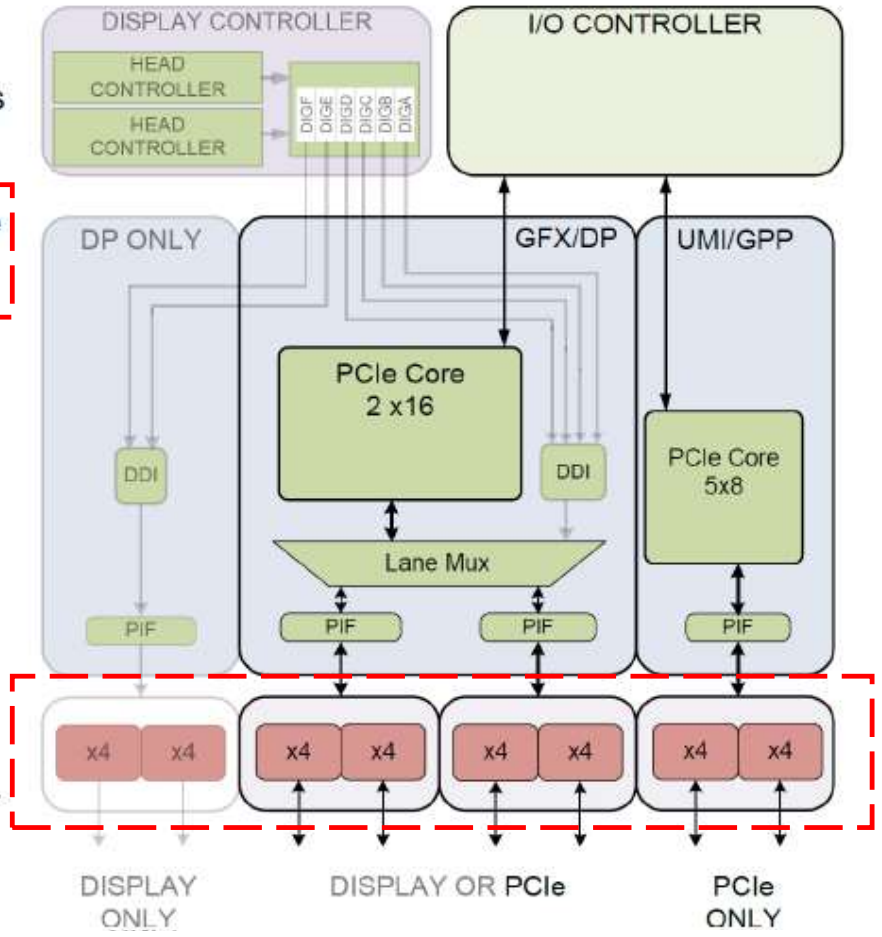
- Includes
  - 4 Stream Cores
  - 1 Special Functions Stream Core
  - Branch Unit
  - General Purpose Registers
- 4 Stream Cores are capable of
  - 4 32-bit FP MULADD per clock
  - 4 24-bit Int MUL or ADD per clock
  - 2 64-bit FP MUL or ADD per clock
  - 1 64-bit FP MULADD per clock
- Additional special function core
  - 1 32b-FP MULADD per clock



3.2 The microarchitecture of the Family 12h Llano lines (6)

I/O and display capabilities of the Llano processor [12]

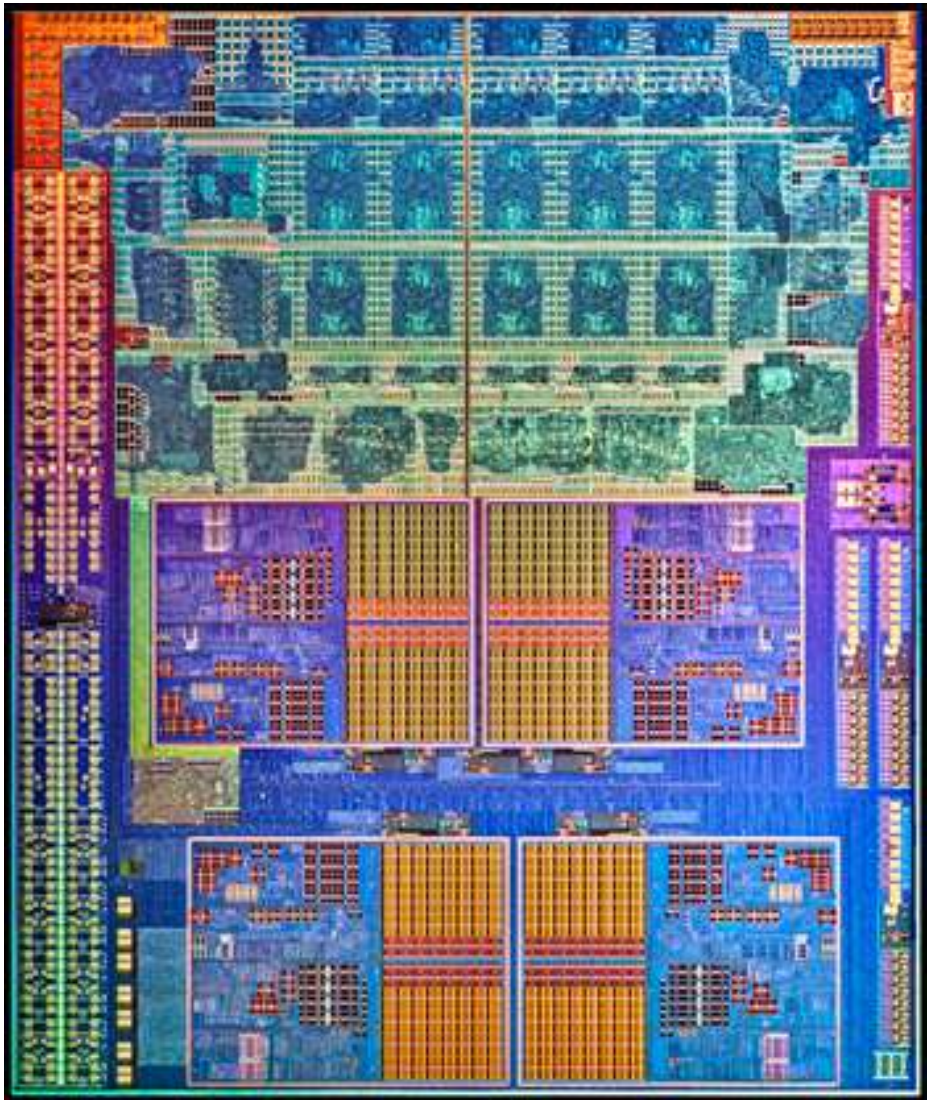
- Same PHY design used for display and PCIe®
- Display controller can drive 2 unique display streams to up to 6 display ports
- Two PCIe Controllers support up to 24 lanes of PCIe
  - Up to Gen2 bit rates (5Gbps or 500MBps)
  - 5 x 8 Controller (5 devices and 8 Lanes)
    - x4 for UMI, 4 lanes for GPP
  - 2 x 16 Controller (2 devices and 16 Lanes)
    - x16 for GFX expansion -or-
    - Up to 4 x4 DP links
- PHY lanes can be bifurcated into multiple engines/links
- Each 'engine' has independent link-frequency & link-width control
- Highly configurable lane allocation to support varied platform topologies



GPP: General Purpose Port
UMI: Unified Media Interface
(Connection to Fusion Control Hub)

3.2 The microarchitecture of the Family 12h Llano lines (7)

Llano's microphotograph [13]

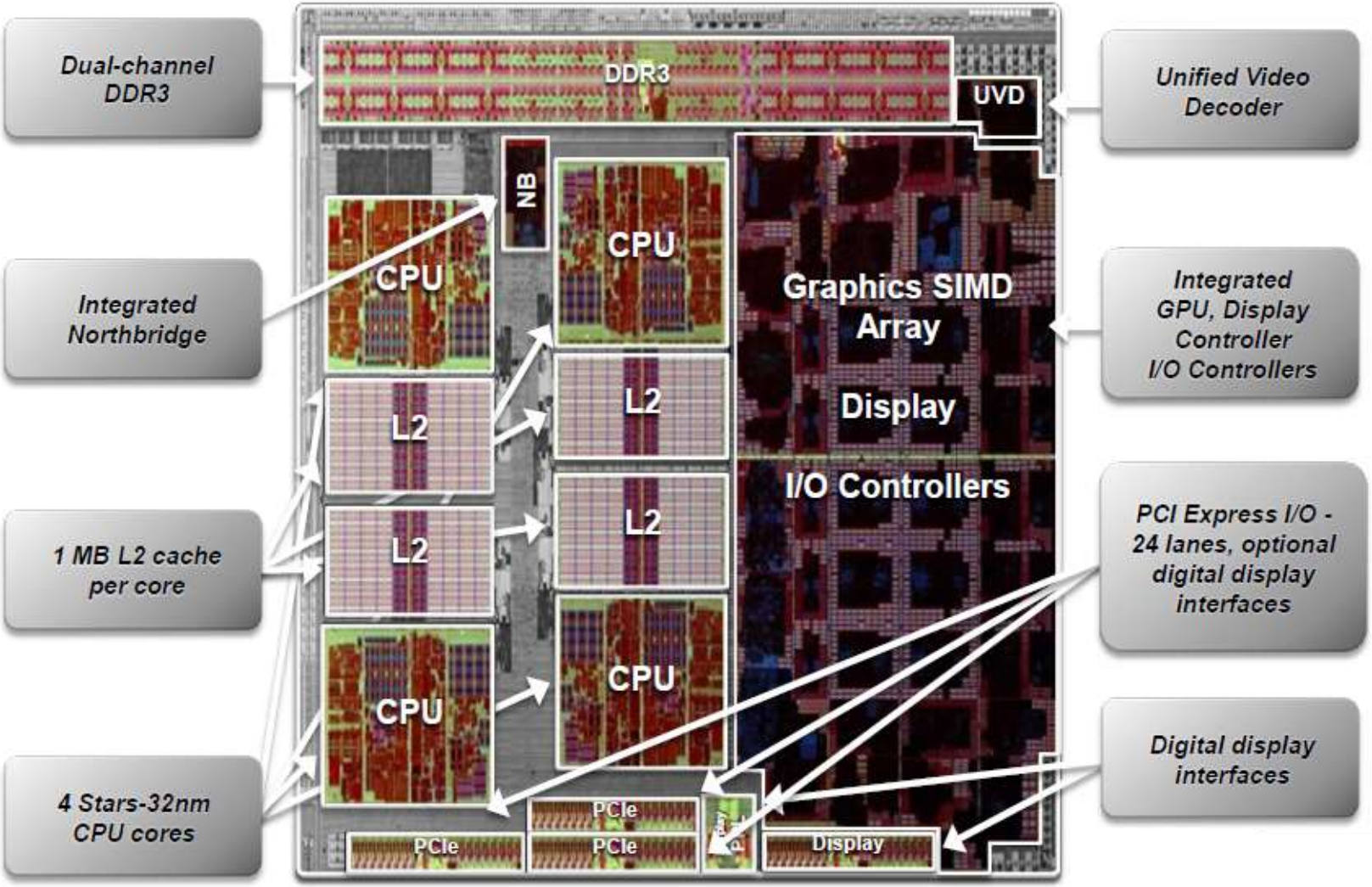


Llano

- 32 nm technology,
- 228 mm2, 1450 mtrs.

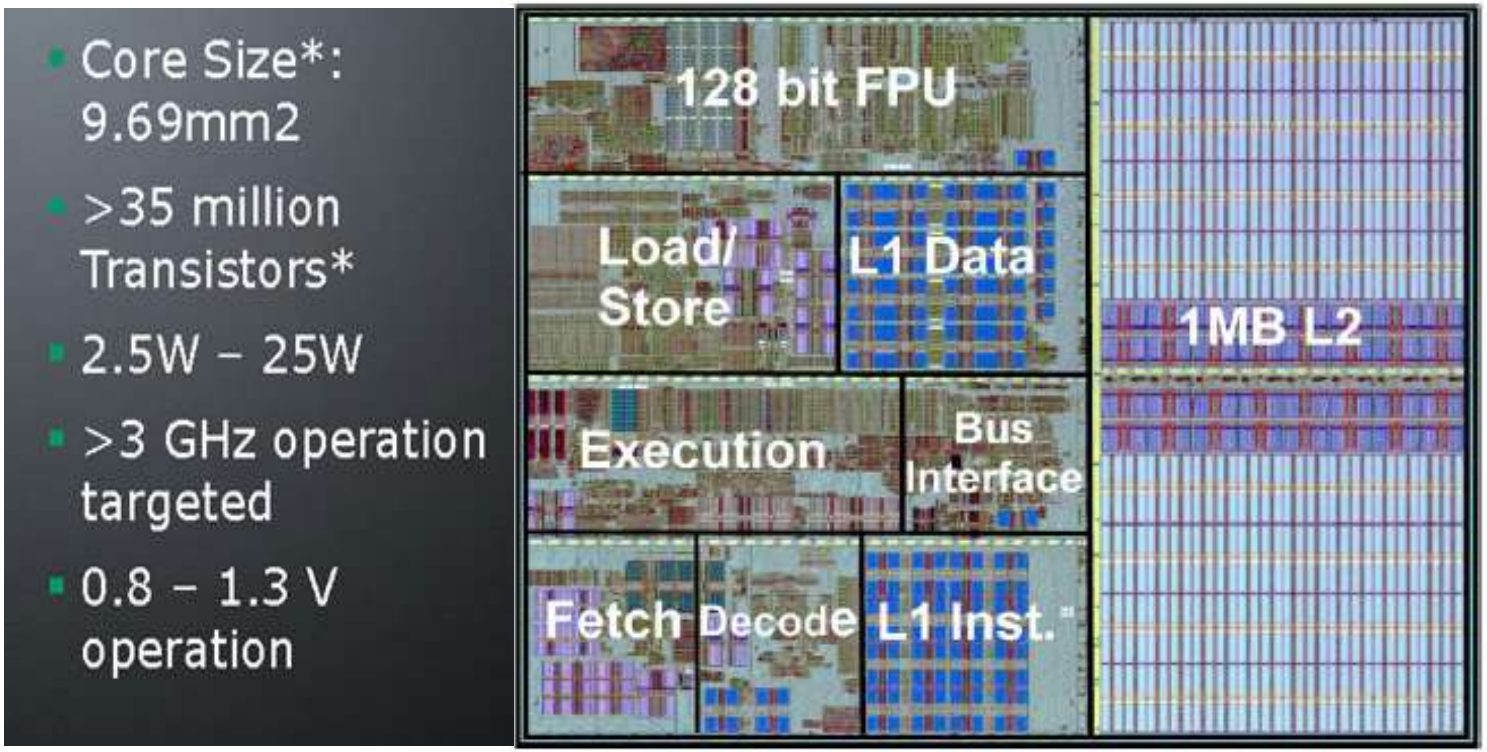
3.2 The microarchitecture of the Family 12h Llano lines (8)

Die plot of the Llano processor [12]



3.2 The microarchitecture of the Family 12h Llano lines (9)

Die plot of a single Llano core [14]
(L2 cache not included)

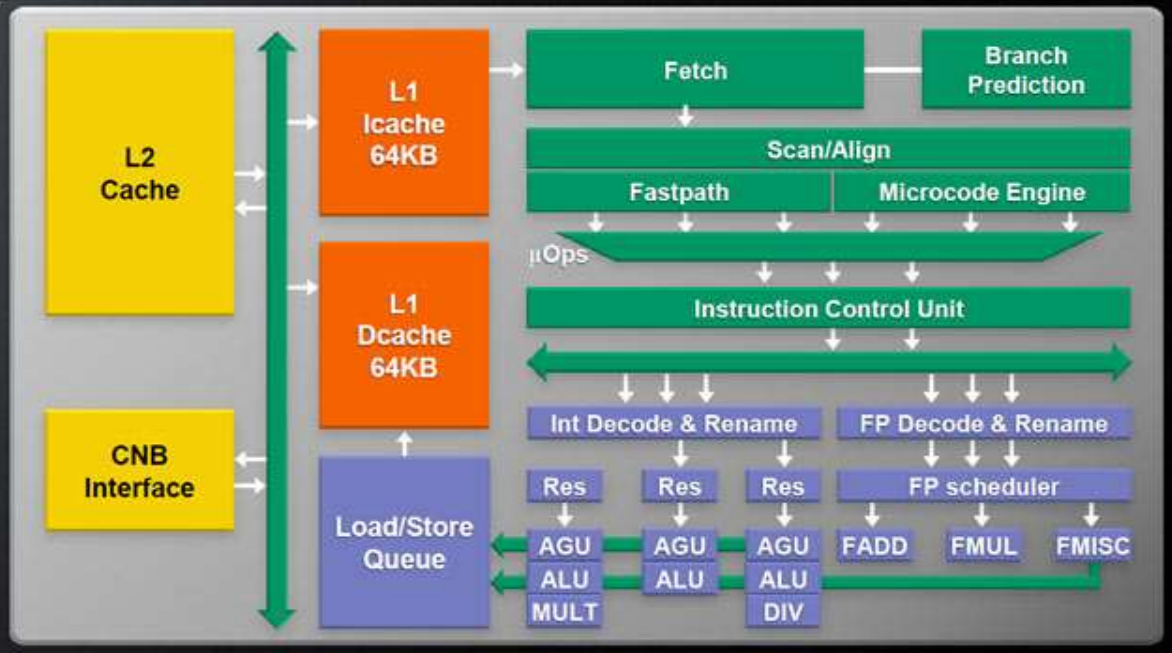


3.3 Microarchitecture enhancements aiming at increasing performance

3.3 Microarchitecture enhancements aiming at increasing performance [15]

32NM "STARS" CPU CORE

- 32nm
- Up to four x86 cores and 4x1MB L2
- >6% IPC improvement from previous x86 generation
  - Larger L2
  - Improved HW prefetcher (IP-based)
  - Bigger window size (larger reorder and load/store buffers)
  - Hardware divider
  - More...
- AMD Turbo Core support



35 & 45W Notebooks, 65 & 100W Desktops

1.4-2.9GHz CPU

400-600MHz GPU

3.3 Microarchitecture enhancements aiming at increasing performance (2)

a) Improved HW prefetcher (IP-based)

Enhanced vs. the K10.5 data prefetcher.

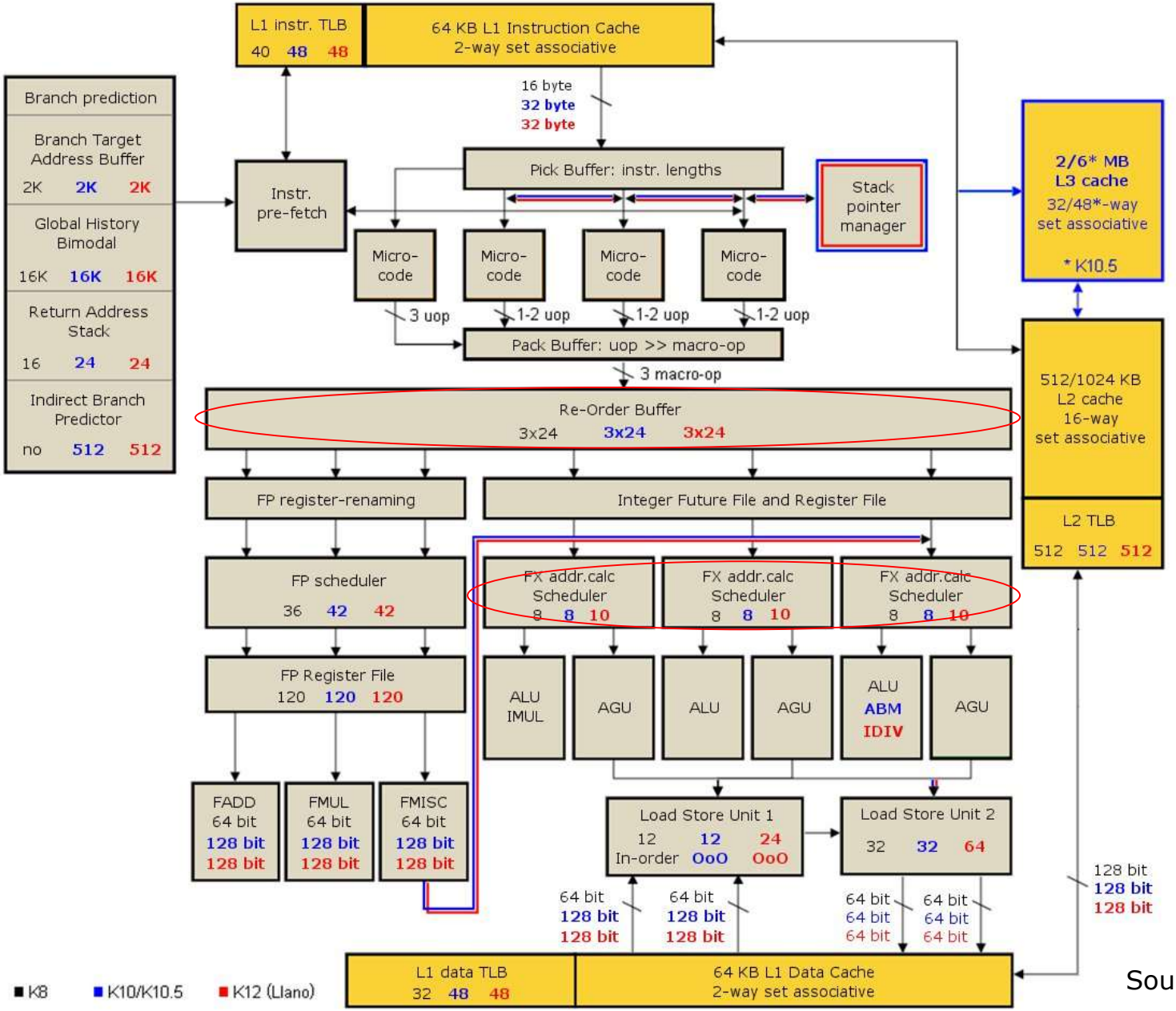
It will not be discussed here, details can be found in [12].

3.3 Microarchitecture enhancements aiming at increasing performance (3)

b) Larger instruction window sizes-1 [12]

- To increase ILP (Instruction Level Parallelism) Llano has
  - 12 more micro-ops in the reorder buffer (84 micro-ops in total) and
  - 6 more micro-ops in the reservation stations (30 micro-ops in total)

3.3 Microarchitecture enhancements aiming at increasing performance (4)



Source: [16]

3.3 Microarchitecture enhancements aiming at increasing performance (5)

b) Larger instruction window sizes-2 [12]

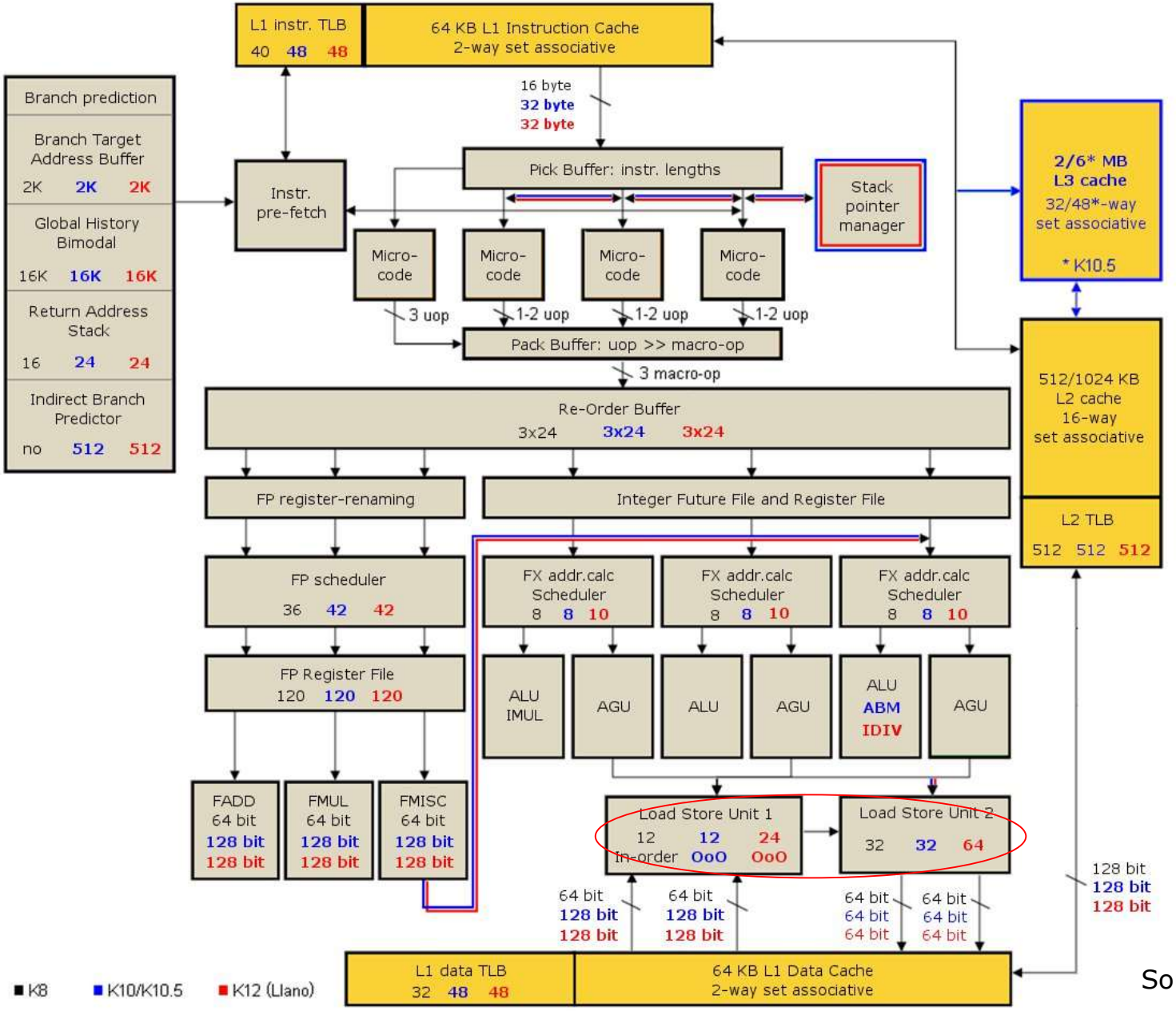
- To compensate for the lack of an L3 cache, Llano has
  - an increased number of load/store queue entries.

Remark

There is a confusion about the number of additional load/store queue entries;

- according to [12] there are 6 more load/store queue entries, whereas
- according to [16] Llano has 44 more load/store queue entries.

3.3 Microarchitecture enhancements aiming at increasing performance (6)

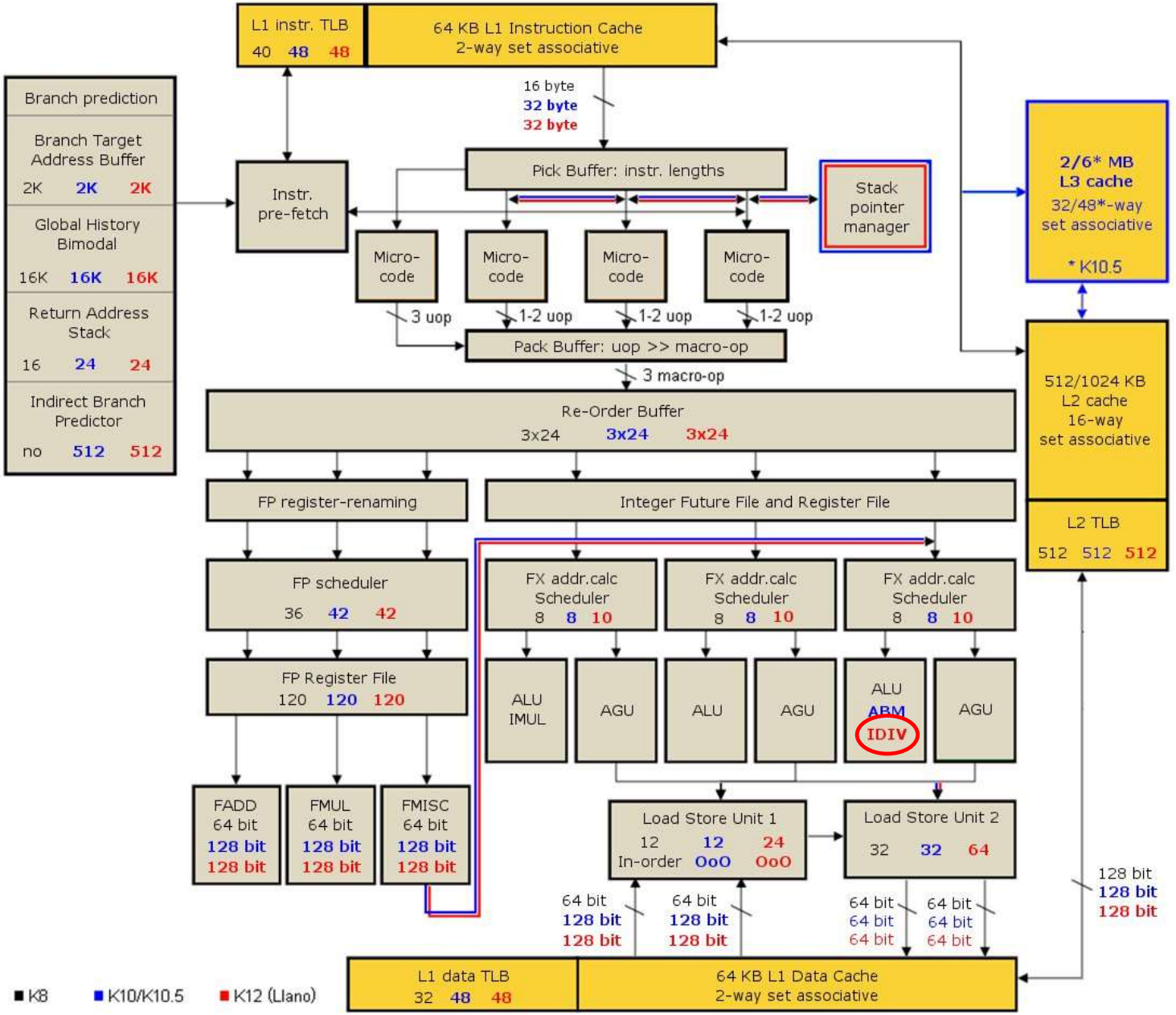


Source: [16]

3.3 Microarchitecture enhancements aiming at increasing performance (7)

c) Hardware FX divider (IDIV)

3.3 Microarchitecture enhancements aiming at increasing performance (8)

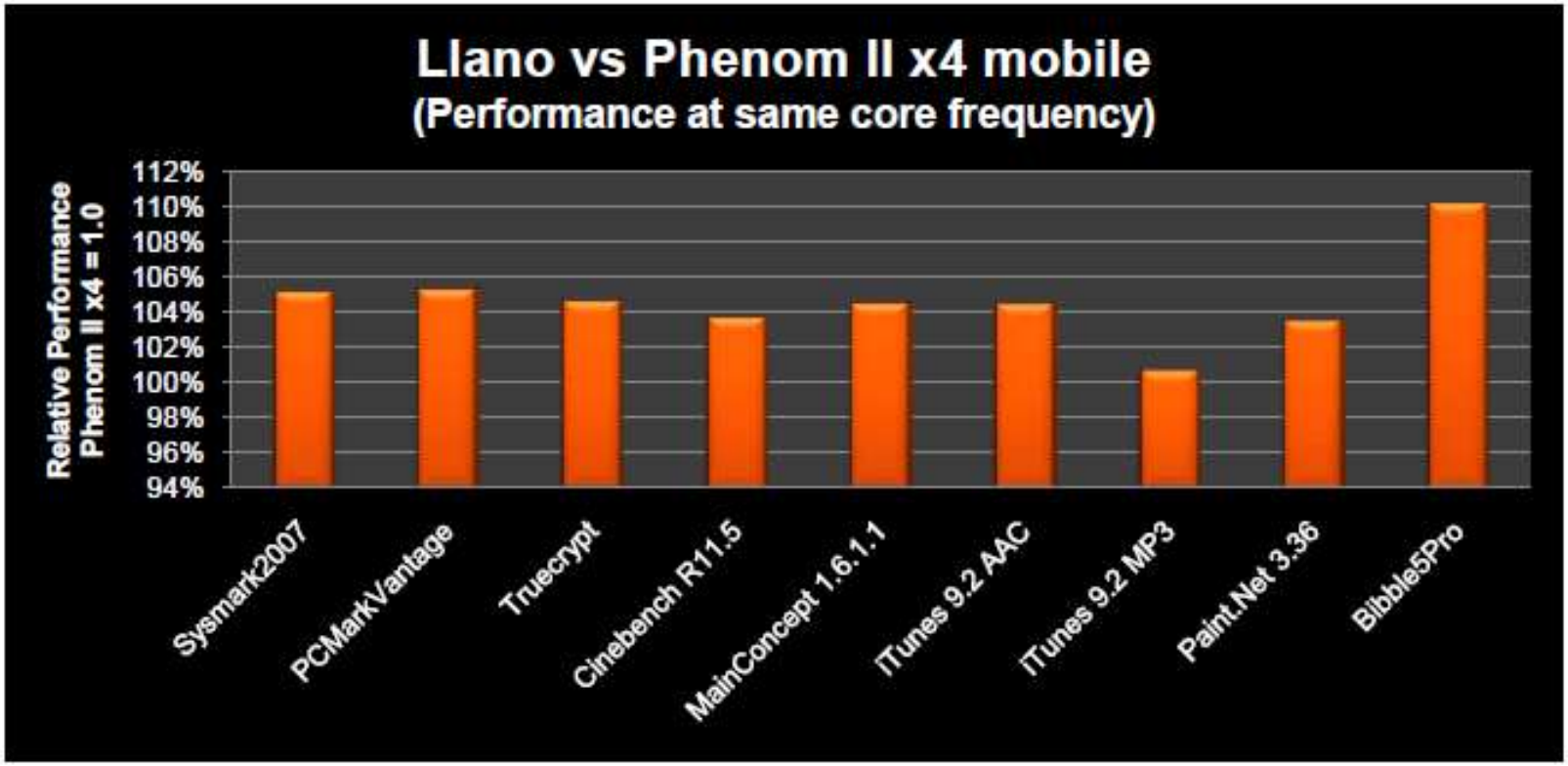


3.3 Microarchitecture enhancements aiming at increasing performance (9)

Performance increase of AMD's A8 APU vs. Phenom 2 X4 [12]

resulting from

- Improved HW prefetcher
- Larger instruction windows
- Hardware FX divider

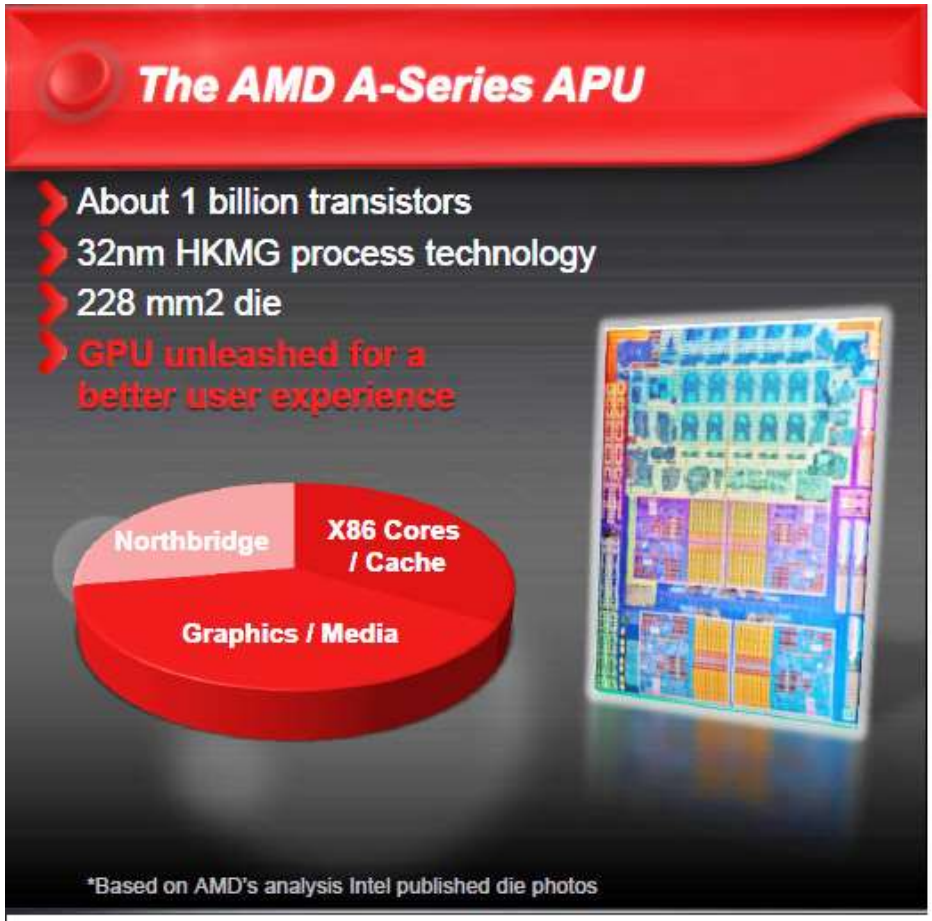


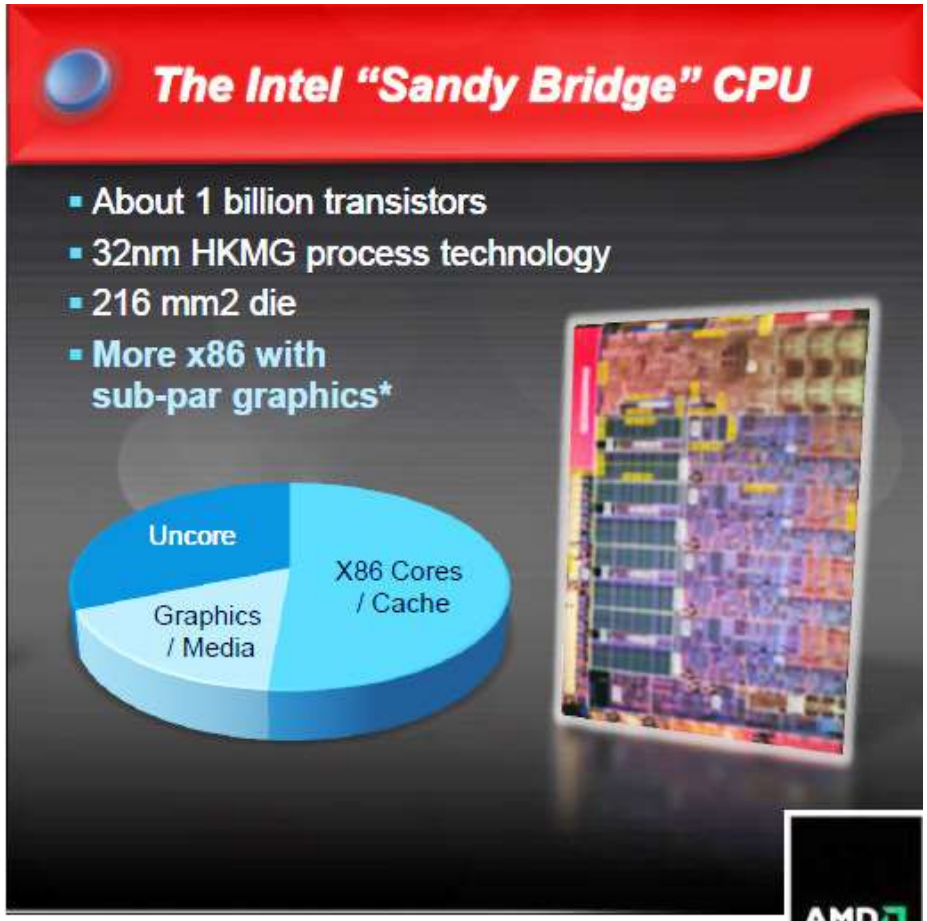
Preliminary measurements or calculations by AMD labs

3.3 Microarchitecture enhancements aiming at increasing performance (10)

Conceptual difference between AMD's Fusion APU's and Intel's Sandy Bridge CPUs [17]

- Llano shows that AMD puts more emphasis on GPU performance than to CPU performance and devotes accordingly more silicon area to graphics and media than to x86 computing.
- This is in sharp contrast to Intel's position as their Sandy Bridge devotes more emphasis and silicon area to x86 computing than to graphics and media.





3.3 Microarchitecture enhancements aiming at increasing performance (11)

Note

A comparison of both die plots reveals that for AMD GPU performance is more important than CPU performance, meaning that the CPU is „fast enough” for the vast majority of desktop and mobile configurations.

All in all, Intel’s Sandy Bridge offers higher X86 performance while AMD’s Llano better graphics and multimedia performance [17].

d) Turbo Core

Principle of operation-1

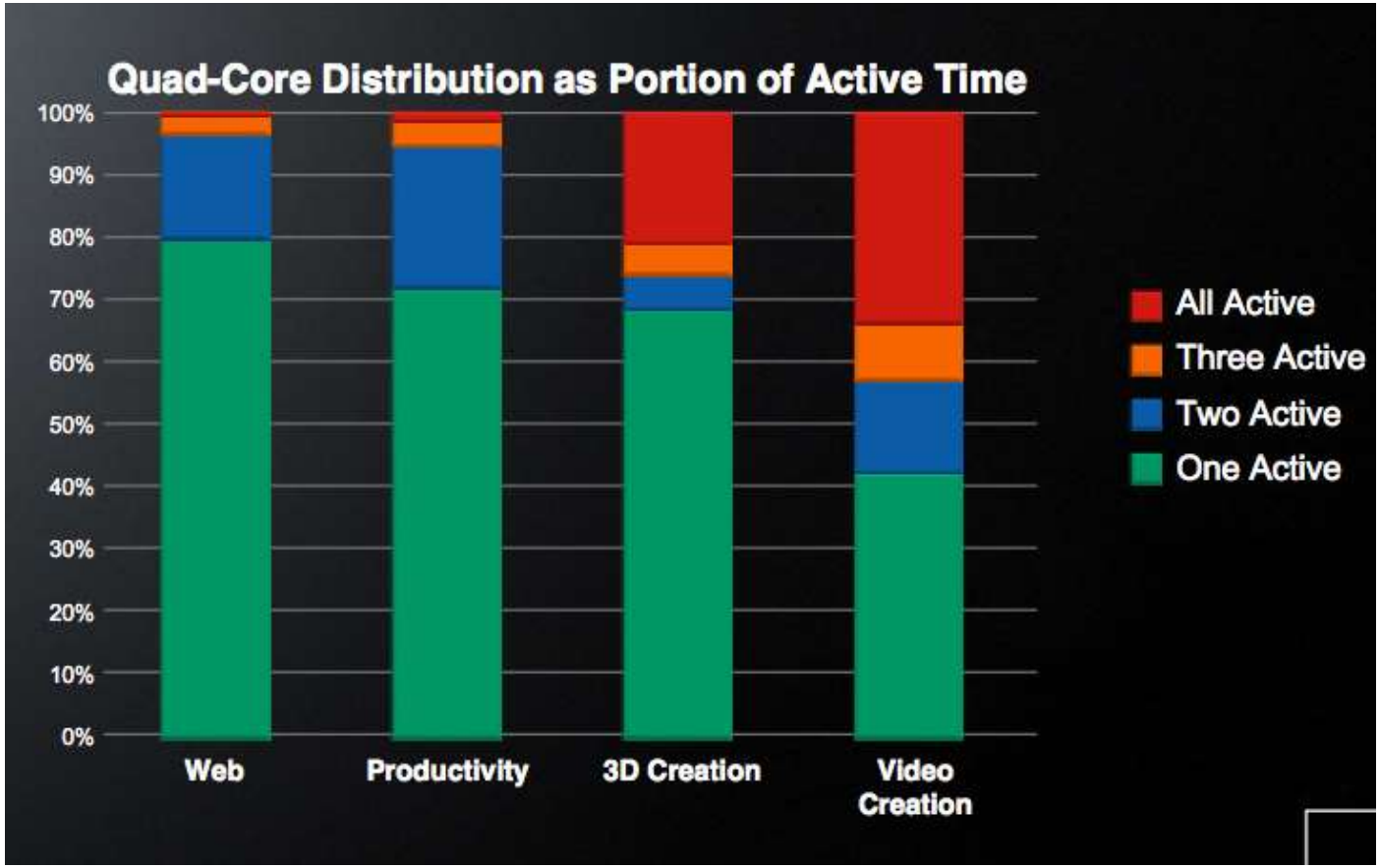
Chip level power consumption varies over time as both

- the number of active cores and
- the „loading" and thuis the actual power consumption of an active core

varies while running an application, as shown below.

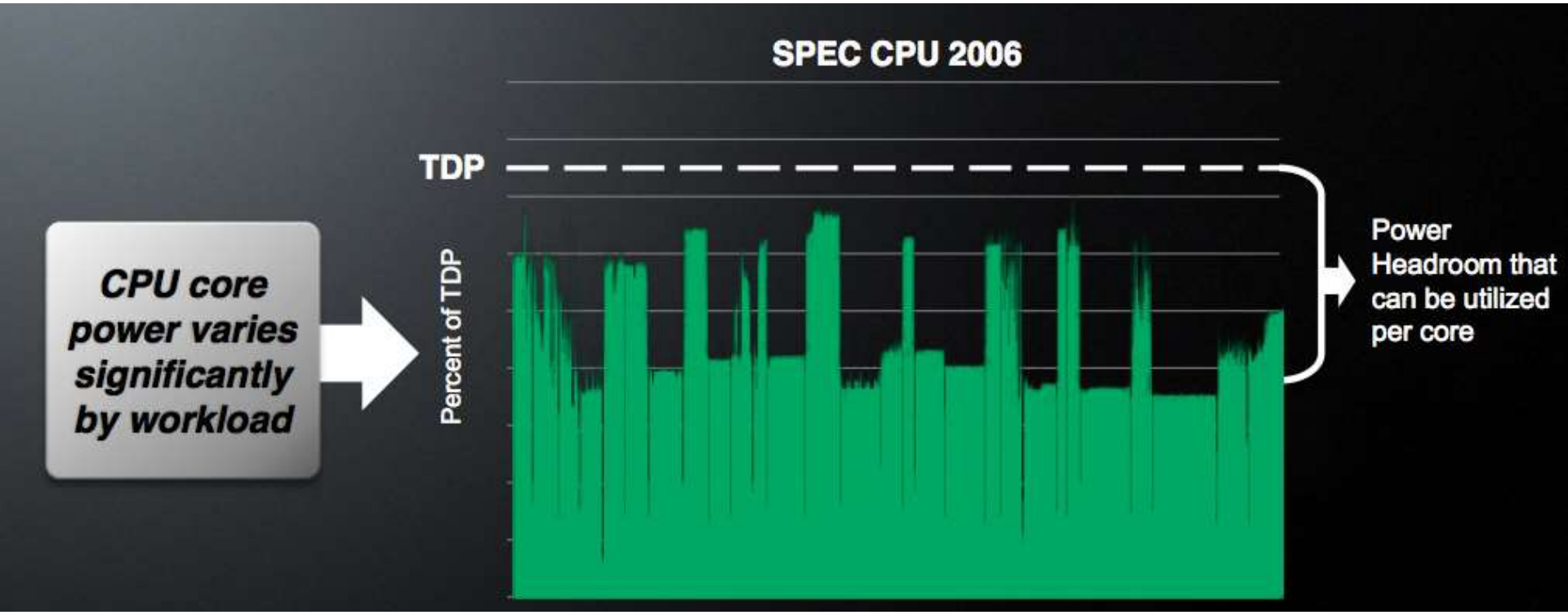
3.3 Microarchitecture enhancements aiming at increasing performance (13)

Number of active cores while running different kinds of applications [18]



3.3 Microarchitecture enhancements aiming at increasing performance (14)

Actual power consumption of a core vs TDP while running SPEC 2006 [18] -1



3.3 Microarchitecture enhancements aiming at increasing performance (15)

Actual power consumption of a core vs TDP while running SPEC 2006 [18] -2

- According to sources [12] common workloads consume no more than 60-70 % of the available TDP.
- It follows that with an accurate real time power consumption estimation it is feasible to exploit the 20-40 % gap between the TDP and the power consumption of the application running.

Principle of operation-2 [14]

- When chip level power consumption - averaged on a ms time scale - is less than the TDP, the remaining chip level power headroom can be utilized for boosting the frequency of the active cores.

  In this way common workloads with lower power consumption can ran faster.
- Improved clock gating and power gating (to be discussed later) increase the available power headroom considerably by reducing the power consumption of inactive cores or inactive parts of the processor.

3.3 Microarchitecture enhancements aiming at increasing performance (17)

Notes

1) The Turbo Core technology, as implemented in AMD's Llano processors is already the second, radically re-designed implementation of AMD's Turbo Core technology introduced in the K10.5 Istambul based desktop line (Thuban).
2) The implementation of AMD's Turbo Core technology is based on a patent of Naffziger [19].

Principle of the implementation of the Turbo Core technology in Llano-1

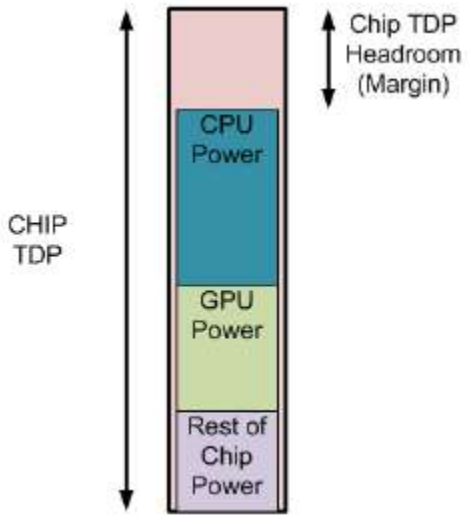
(Simplified) [12]

Power consumption of the chip (P_{CH}) will be determined basically by a digital power monitor.

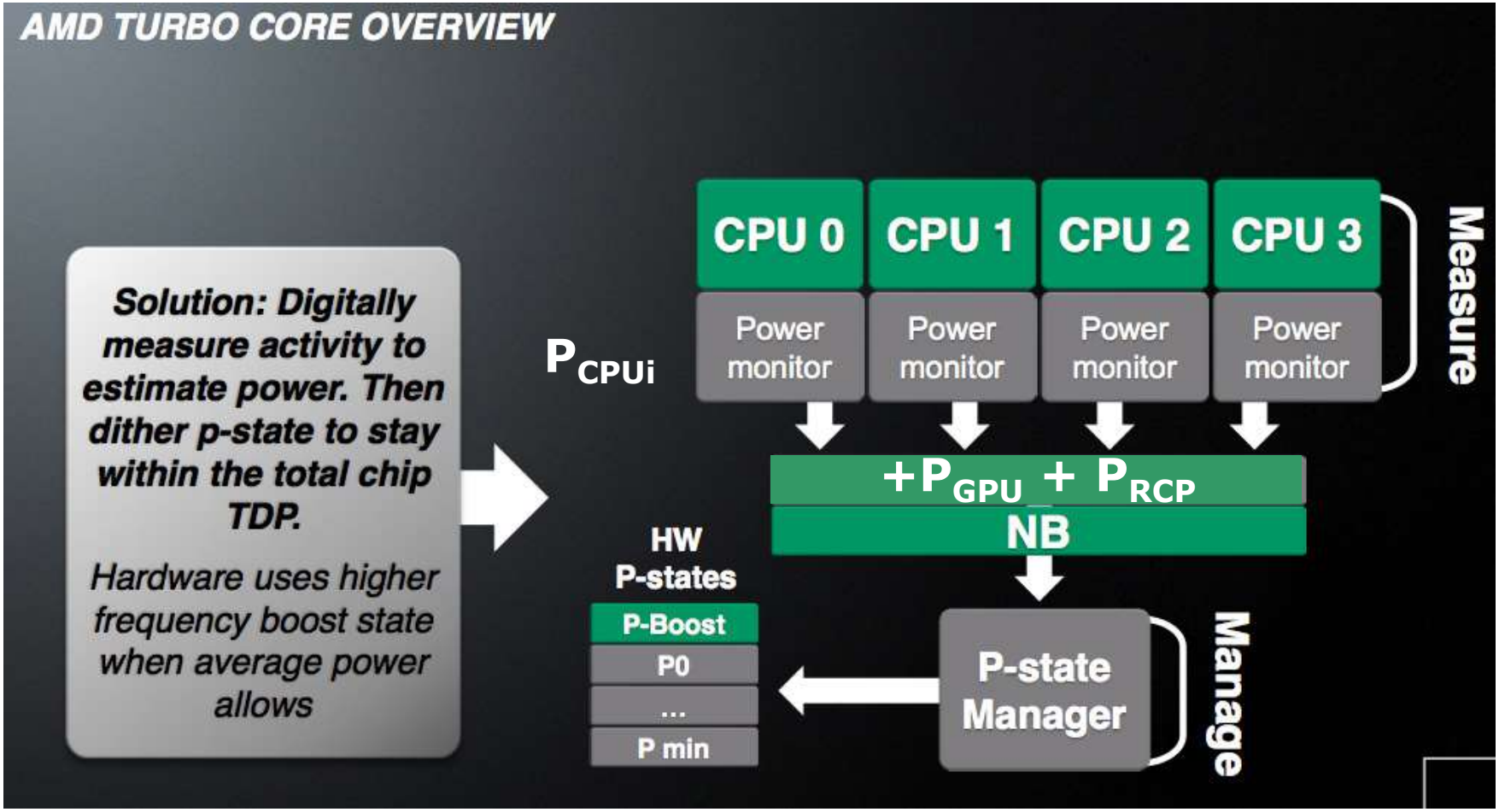
$$P_{CH} = \Sigma P_{CPUi} + P_{GPU} + P_{RCP}$$

with

P_{CPUi}: Power consumption of the CPUi
P_{PGU}. Power consumption of the GPU
P_{RCP}: Power consumption of the rest of the chip



Principle of the implementation of the Turbo Core technology in Llano-2
(Simplified) [18]



3.3 Microarchitecture enhancements aiming at increasing performance (20)

The power consumption of the cores is determined by

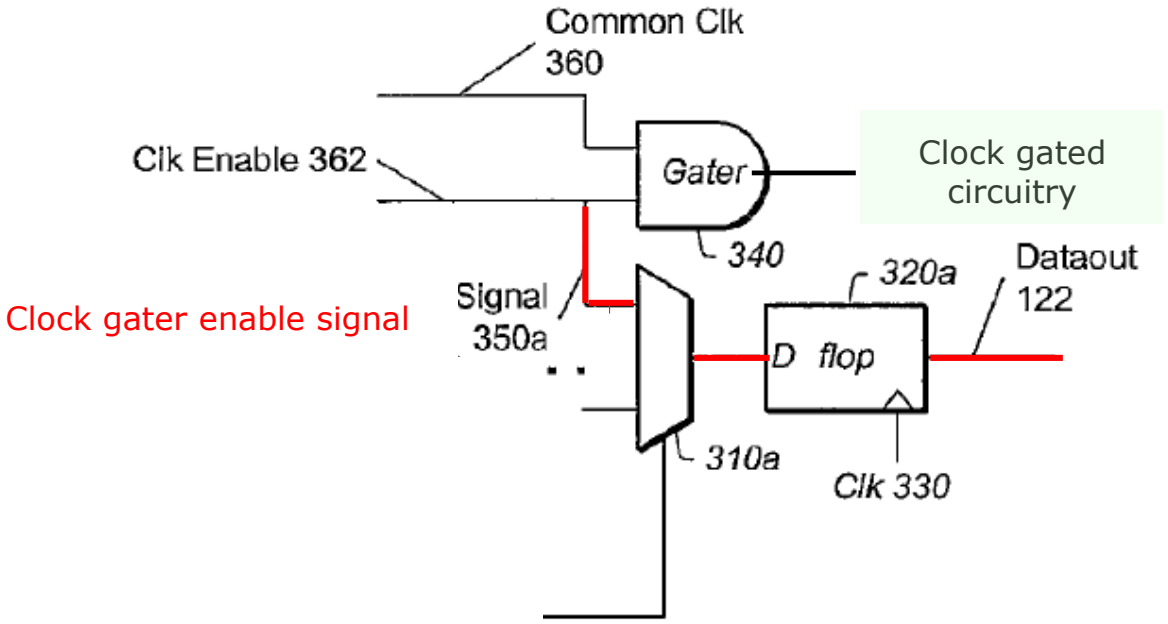
$$P_{CPUi} = P_{Leakage} + Cac \times V^2 \times fc$$

with
- $P_{Leakage}$: Leakage power consumption, will be determined by silicon testing
- Cac: Switching capacitance (will be on-line estimated as a sliding average, as described next
- V: Actual core voltage (known value)
- fc: Actual core clock frequency (known value)

Estimation of Cac (Switching capacitance)

Per core power monitoring circuitry samples a comprehensive set of 95 signals [14].

Most of these signals are clock gater enable signals that determine whether downstream circuitry should be active or not, since the downstream clock gated circuitry either contributes to the switching capacitance of the core or not [19].

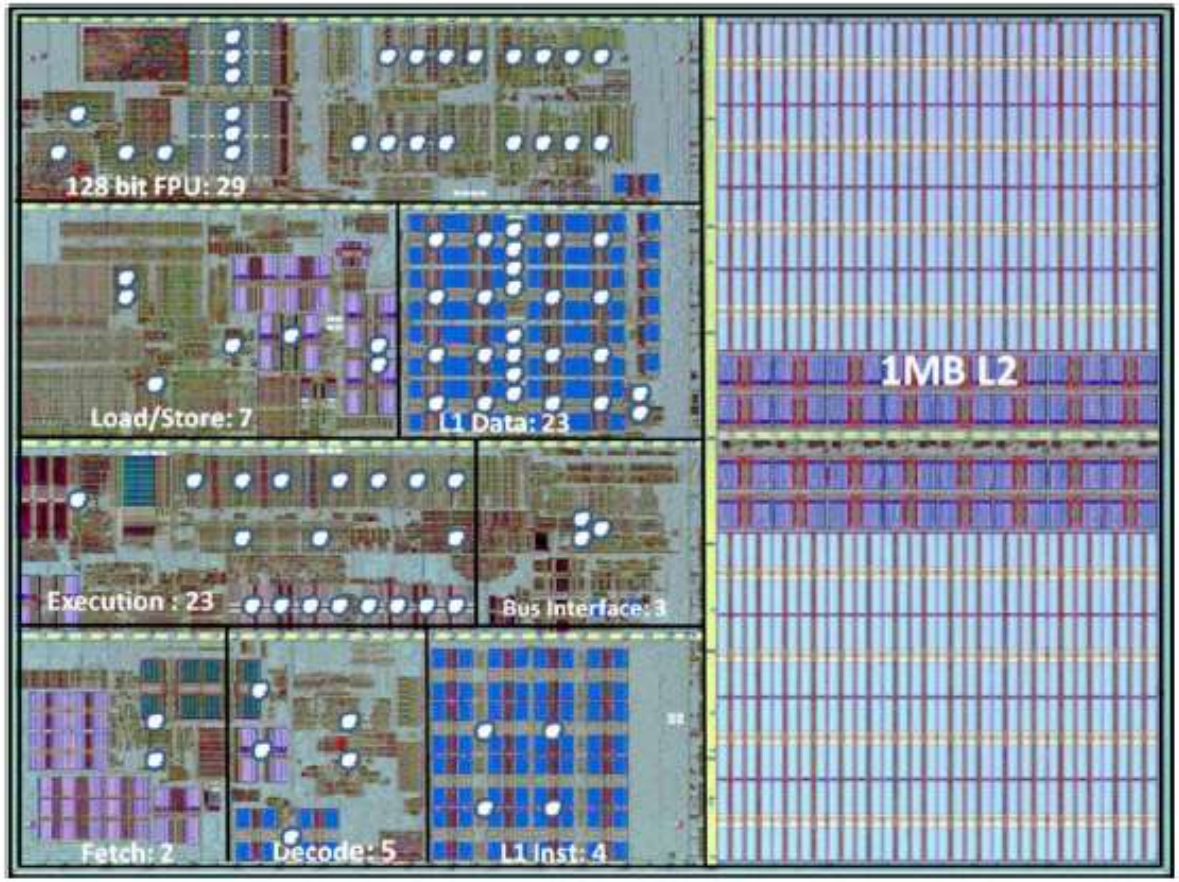


Multiplexer

3.3 Microarchitecture enhancements aiming at increasing performance (22)

Power monitor signal locations and signal count for each core unit [14]

(Some circles represent more than one signal in a given location)



Calculation of the momentary power consumption of a core P_{CPUi}

Let's designate the signals belonging to the core i by s_{ij} {j=0, 1, …94}

Furthermore, let's assume for a moment that all signals of the core i are sampled at regular time intervals t_s at the same time and let's consider all sampled signal values obtained at a time t^k: s_{ij}^k

Note that all signals are digital, so their sampled values are either 0 or 1

Then the momentary power consumption of core i at the sampling time t^k can be estimated as

$$P_{CPUi}^{tk} = \sum_j s_{ij}^{tk} \times w_{ij}$$

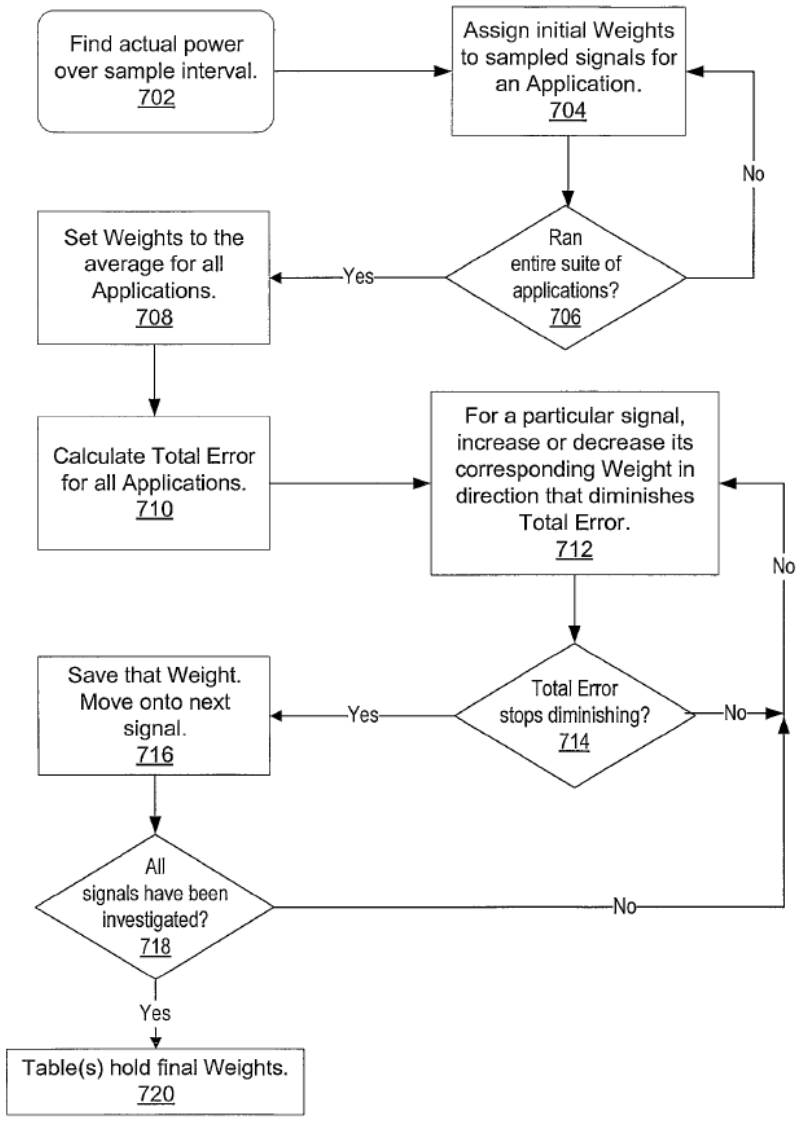
with

w_{ij}: weights representing the contribution of the circuitry associated with the sampled signal s_{ij}

Principle of determining the weights

The weights are determined based on extensive post-silicon characterization rather than relying on pre-silicon power consumption models [14].

The related algorithm is [19]:



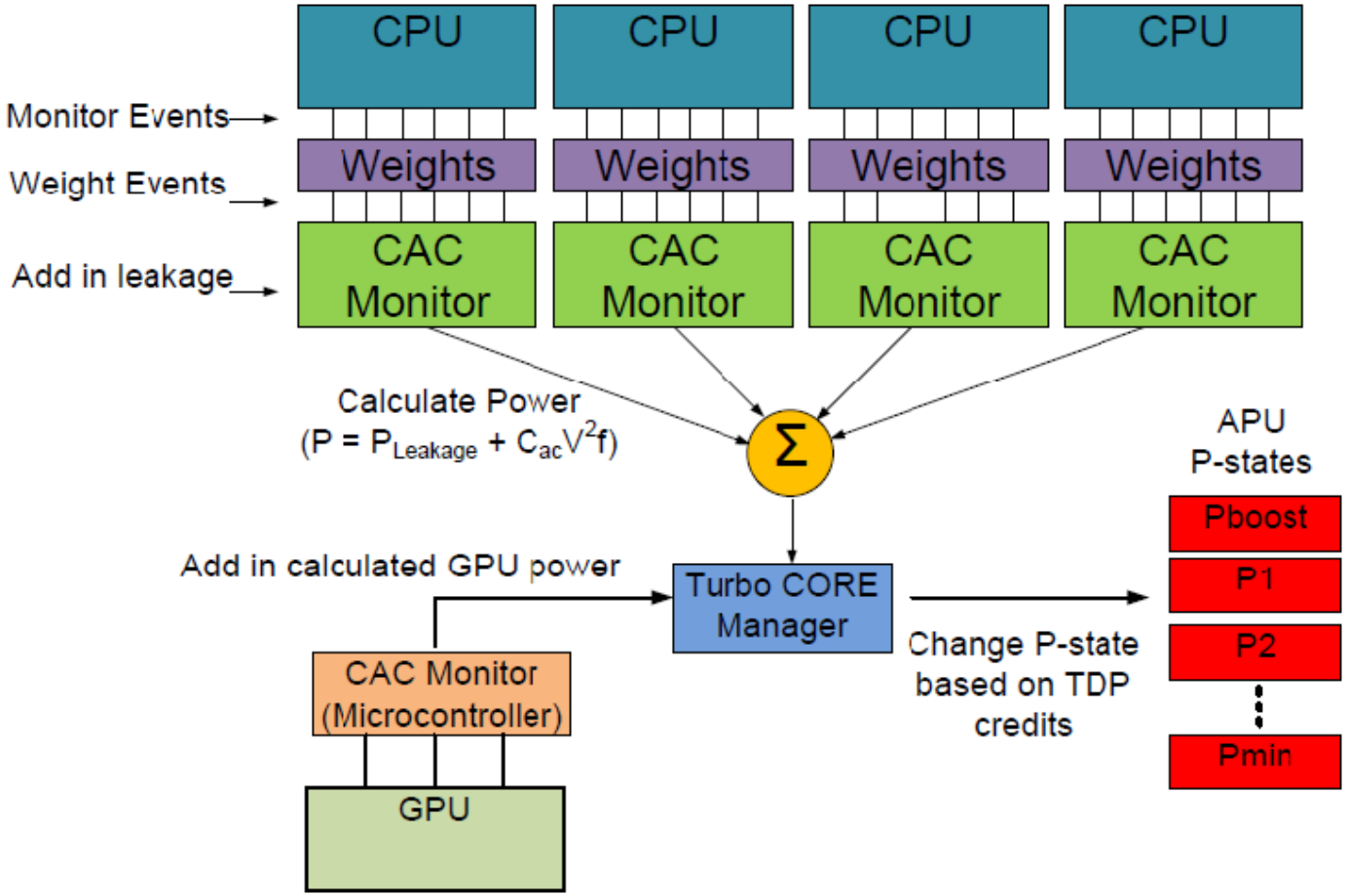
3.3 Microarchitecture enhancements aiming at increasing performance (25)

In the assumed solution a gliding average of a large enough number of momentary power consumption values (e.g. a few hundred samples) would yield a good enough estimation for the power consumption of the considered core in the given time interval.

Nevertheless, in-parallel sampling of a large number of signals would require the routing of a large number of high speed signals whereas actual thermal time frames are in the order of ms, this allows to implement a much simpler serial sampling of the signals.

The implemented Digital Monitor is accurate to within 2 % across a broad range of application types [14].

Simplified layout of the digital power monitoring system [12]



CAC: Switching Capacitance

Operation of the Turbo Core Manager (TCM) [12]

(Simplified)

TCM calculates the energy margin (EM) both at the chip level (EM_{CP}) and at the level of CPUs (EM_{CPUi})

$$EM_{CP} = TDP_{CP} - P_{CH}$$

with

$$P_{CH} = \Sigma P_{CPUi} + P_{GPU} + P_{RCP}$$

TDP_{CP}: Chip-level TDP
P_{CH}: Power consumption of the chip
P_{CPUi}: Power consumption of the CPUi
P_{PGU}. Power consumption of the GPU
P_{RCP}: Power consumption of the rest of the chip

$$EM_{CPUi} = TDP_{CPU} - P_{CPUi}$$

with

TDP_{CPUi}: CPU-level TDP

Interpretation of the energy margins

Positive margins indicate power headroom

Negative margins indicate power overage

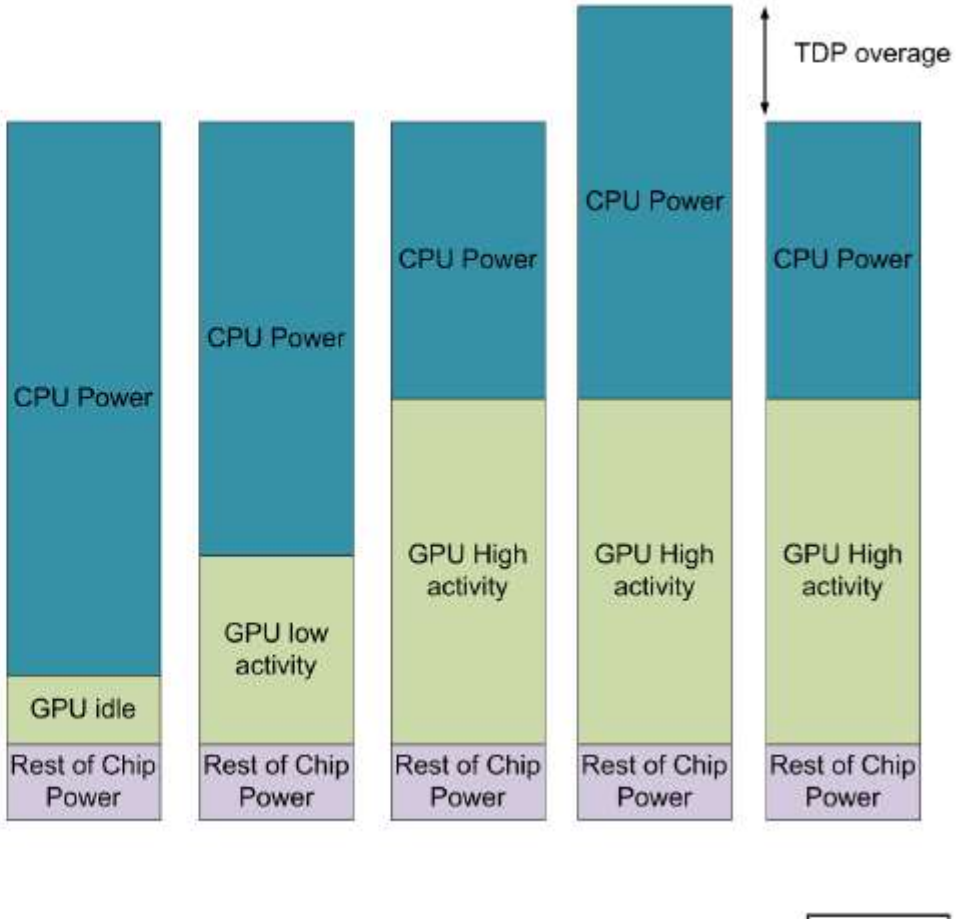
Power headrooms can be utilized to increase clock frequency

Power overages need to initiate throttling (clock reduction)

If there is available power headroom CPU clock frequencies can be increased but if the CPU cores are not fully utilized or are inactive the GPU frequency can not be boosted.

Example for the operation of the Turbo Core technology [12]

- Within the TDP limit power can be traded between CPU and GPU
- GPU performance is prioritized
- Can allow combined CPU/GPU thermal allowance which exceeds TDP of the part
- If temp exceeds thermal limit associated with CPU allowance, the CPU performance is reduced to fall back within TDP envelope
- Particularly useful in low-ambient conditions



Utilizing idle CPU cores or an idle GPU as a heat sink [12]

As idle CPU cores or an idle GPU core behave like a heat sink
idle cores increase the TDP limit of active cores by a factor called the Power Density multiplier (PDM).

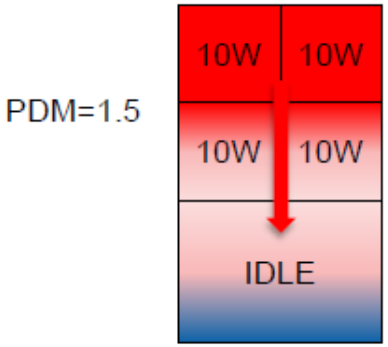
Its value depends on the topology of the idle cores and the ambient temperature.

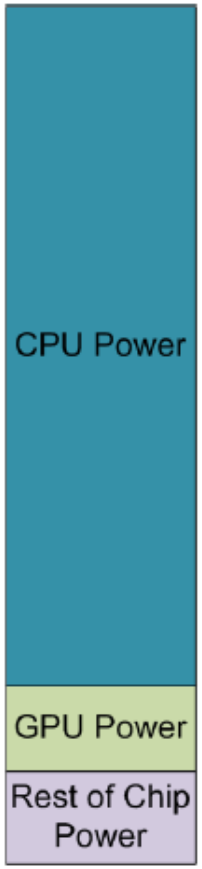
Note: The Turbo Core Manager (TCM) does not raise the TDP limit of the GPU.

Examples for operating the Turbo Core technology in case of idle CPU/GPU cores

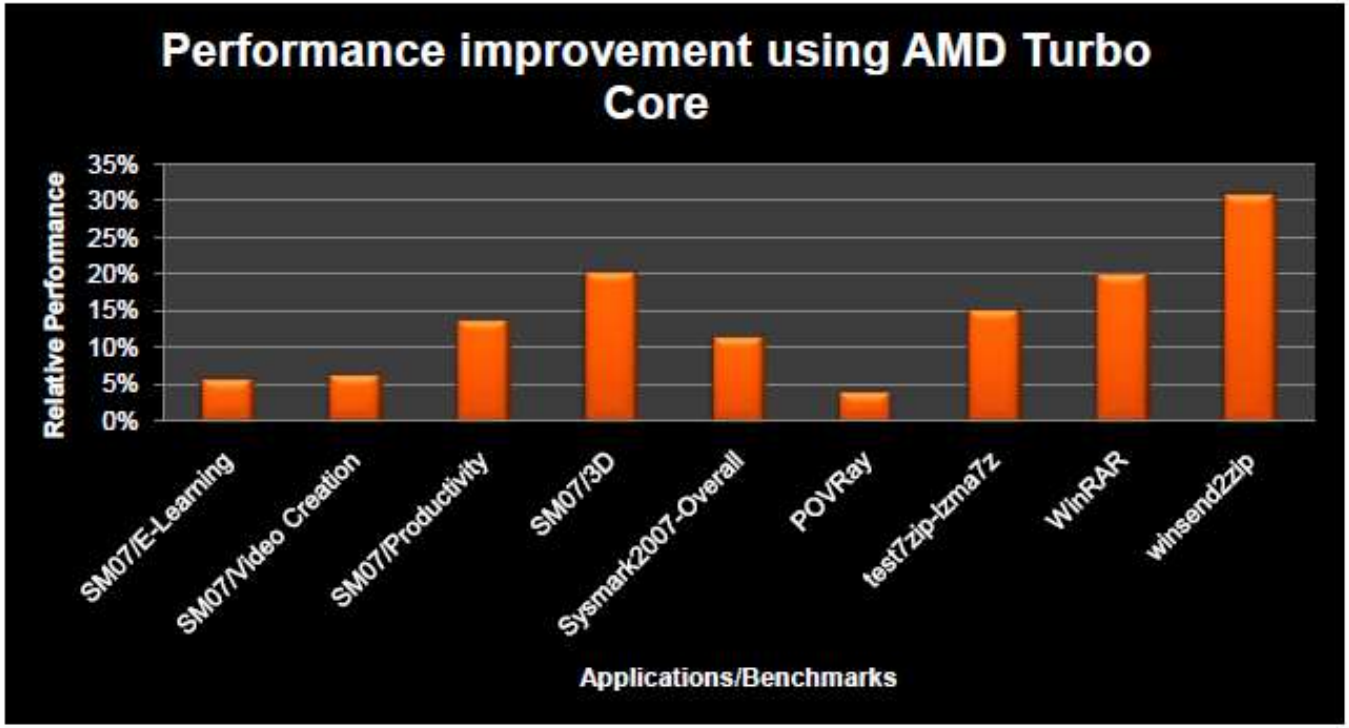
Using GPU power cooling to boost CPU performance [12]

- Shared cooling solution between CPU and GPU
- Idle GPU serves a heatsink for CPUs
- Heat transfer between CPU and GPU
- GPU Power Density Multiplier (PDM) applied
- Increasing the CPU Thermal and Power Headroom and the performance as a result
- Increased CPU TDP Budget
  - CPU TDP Limit + Re-allocated Power from GPU
- Increased CPU Thermal Headroom
  - CPU TDP Limit = 15W (10w x PDM)





Performance improvement achieved by AMD's Turbo Core [12]



- AMD Turbo Core technology maximizes performance on low-thread count apps

3.4 Microarchitecture enhancements aiming at reducing power consumption

3.4 Microarchitecture enhancements aiming at reducing power consumption

Overview

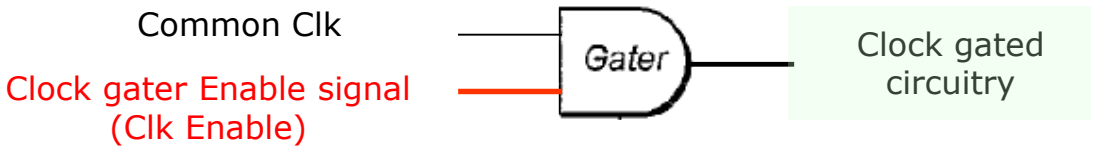
a) Power-aware clock grid design
b) Power gating
c) Core C6 state (CC6 state)
d) Package C6 state (PC6 state)

3.4 Microarchitecture enhancements aiming at reducing power consumption (2)

a) Power-aware clock grid design [20], [19]

Use of clock gating

- Recent processors, like Llano make use of clock gating instead of a straightforward clocking system.
- Clock gating aims at reducing power consumption by disabling the clocking of temporarily not needed circuitry.
- It is implemented by enabling/disabling the clocking of a certain part of a circuitry by a control signal, called the Clock Gater Enable signal (Clk Enable).



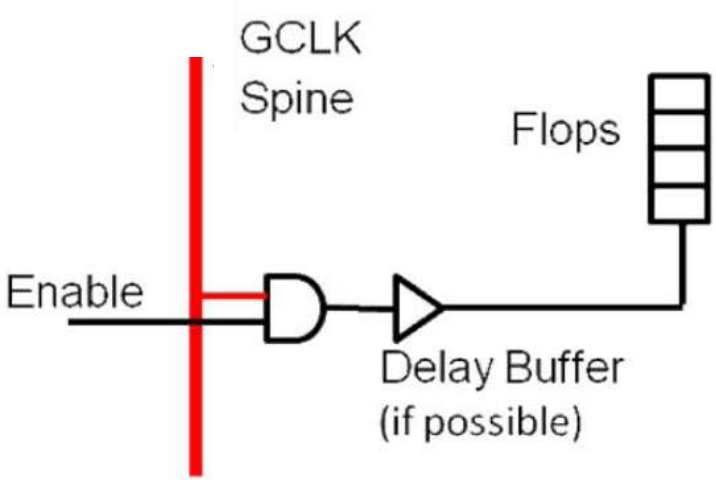
3.4 Microarchitecture enhancements aiming at reducing power consumption (3)

The clock grid-1 [14], [20]

- The clock signal has to be connected to every part of a chip with a low skew (say a few %).
- The typical solution for that is using a clock grid implemented as a metal grid.
- This clock grid needs to be combined with the clock gaters that are responsible for disabling momentarily not needed parts of the microprocessor, as shown below. [14]

3.4 Microarchitecture enhancements aiming at reducing power consumption (4)

Further on, often Delay Buffers are needed to align skew [14].



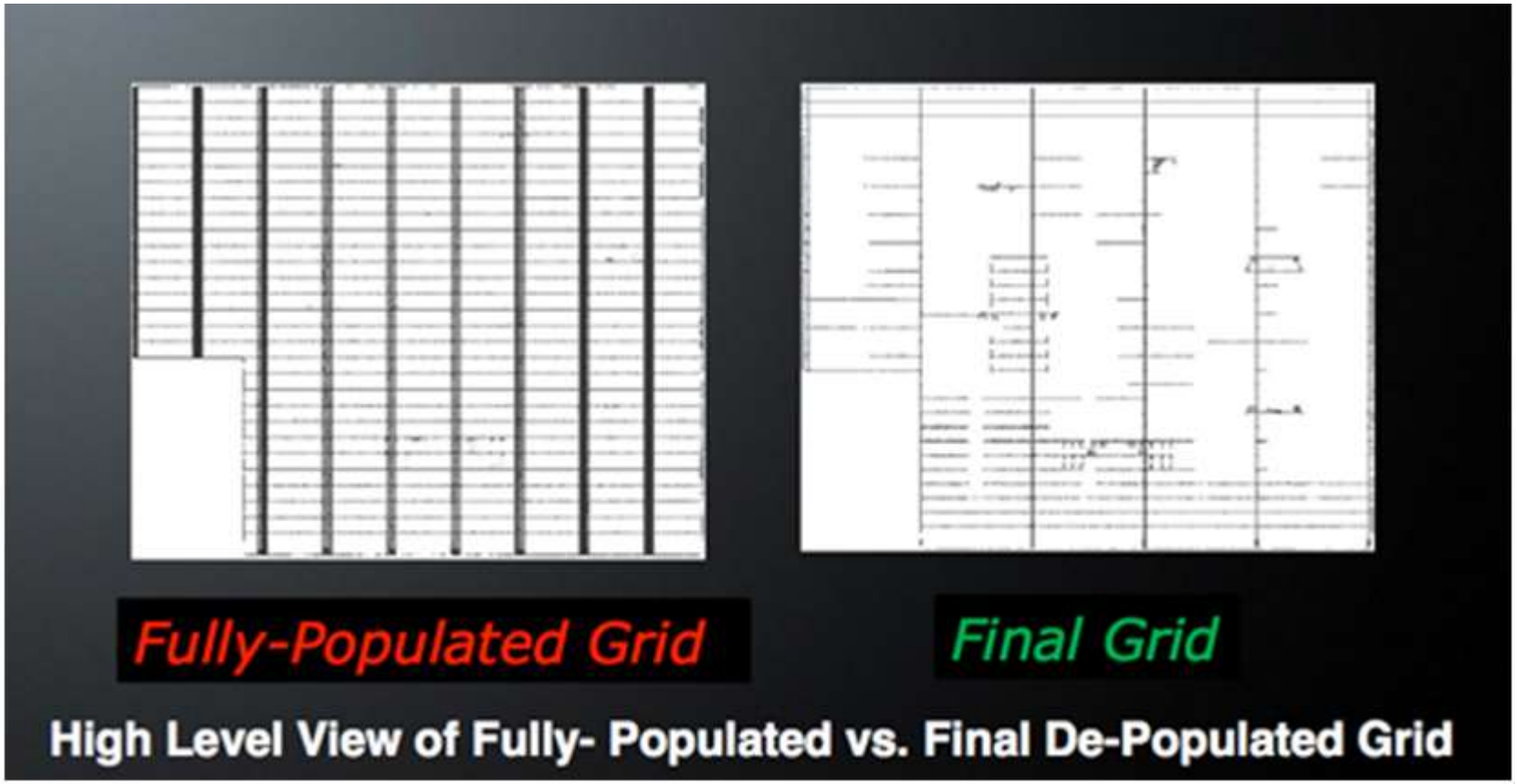
3.4 Microarchitecture enhancements aiming at reducing power consumption (5)

The clock grid-2 [21], [14]

- In a large microprocessor over 30 % of the total power consumption can be used to drive the clock grid.
- Designers of Llano
  - restricted the worst-case skew to less than 3 % of the cycle time, and
  - by a careful design of the clock gater placement they achieved a large-scale depopulation of the global clock grid metal and of the clock buffers, as shown in the nex Figure.

3.4 Microarchitecture enhancements aiming at reducing power consumption (6)

Clock grid design before and after depopulation [21]



By depopulating the clock grid designers achieved

- ~ 80 % reduction in clock grid metal capacitance and
- ~ 50 % reduction in the number of clock buffers.

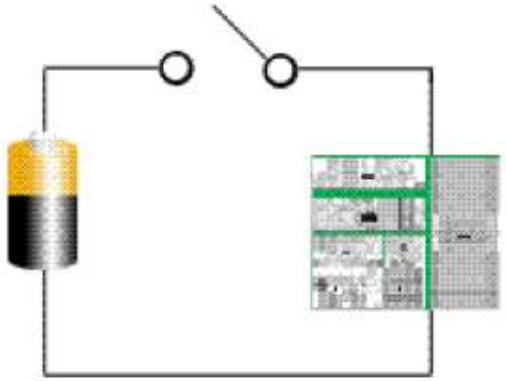
As a result, the clock grid of Llano consumes less than 10 % of the dynamic power.

3.4 Microarchitecture enhancements aiming at reducing power consumption (7)

b) Power gating

Principle of power gating [22], [23]

- Power gating means switching off the power supply for dedicated units of a die (like a core) entirely by switching transistors.
- It can virtually eliminate the leakage component of the power consumption.



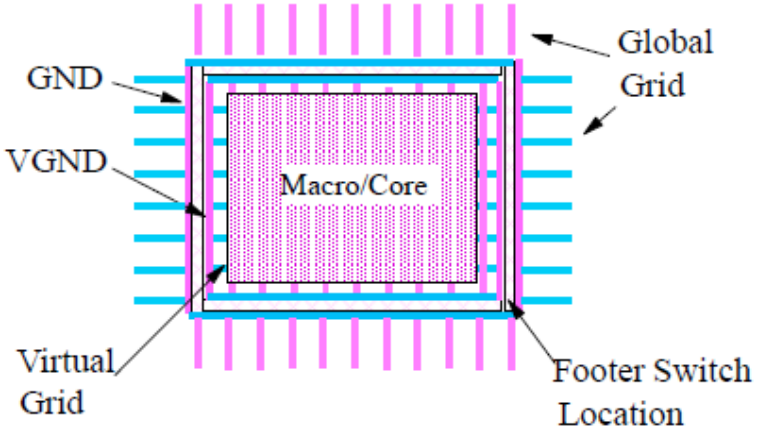
- In the Llano processor all major units, like CPU cores, the GPU core, memory controller etc. can be power-gated individually.

3.4 Microarchitecture enhancements aiming at reducing power consumption (8)

Implementation of power gating-1 [24], [22], [14]

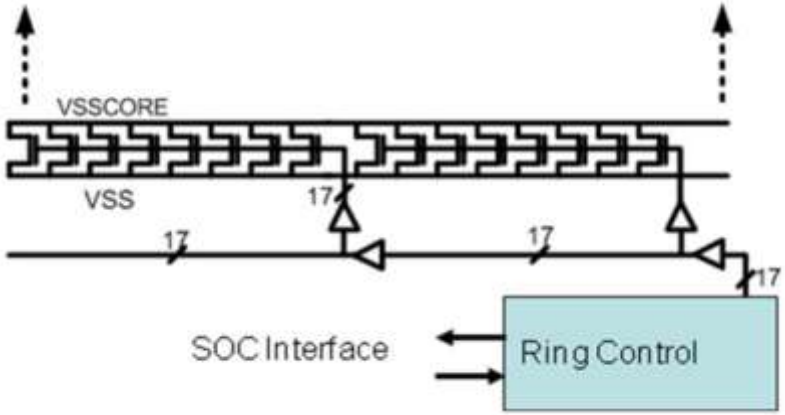
- Llano's power gating implementation is based on Kosonocky's patent application [24].
- In the Llano processor a unit, like a core is power-gated by isolating the ground plane (GND) from the rest of the die.

Then for the power-gated unit the ground plane (GND) is substituted by a virtual ground plane (VGND) that supplies the die [22].



Implementation of power gating-2 [14]

- The ground plane (GND) is carrying the voltage VSS whereas the virtual ground plane the voltage VSSCORE.
- Both planes are connected by a ring of NFET switching transistors, that are controlled by the Ring Control.



If switched on both planes are connected by a small resistance of about 1.1 mΩ.

If switched off, both planes are disconnected, effectively no leakage current can flow.

3.4 Microarchitecture enhancements aiming at reducing power consumption (10)

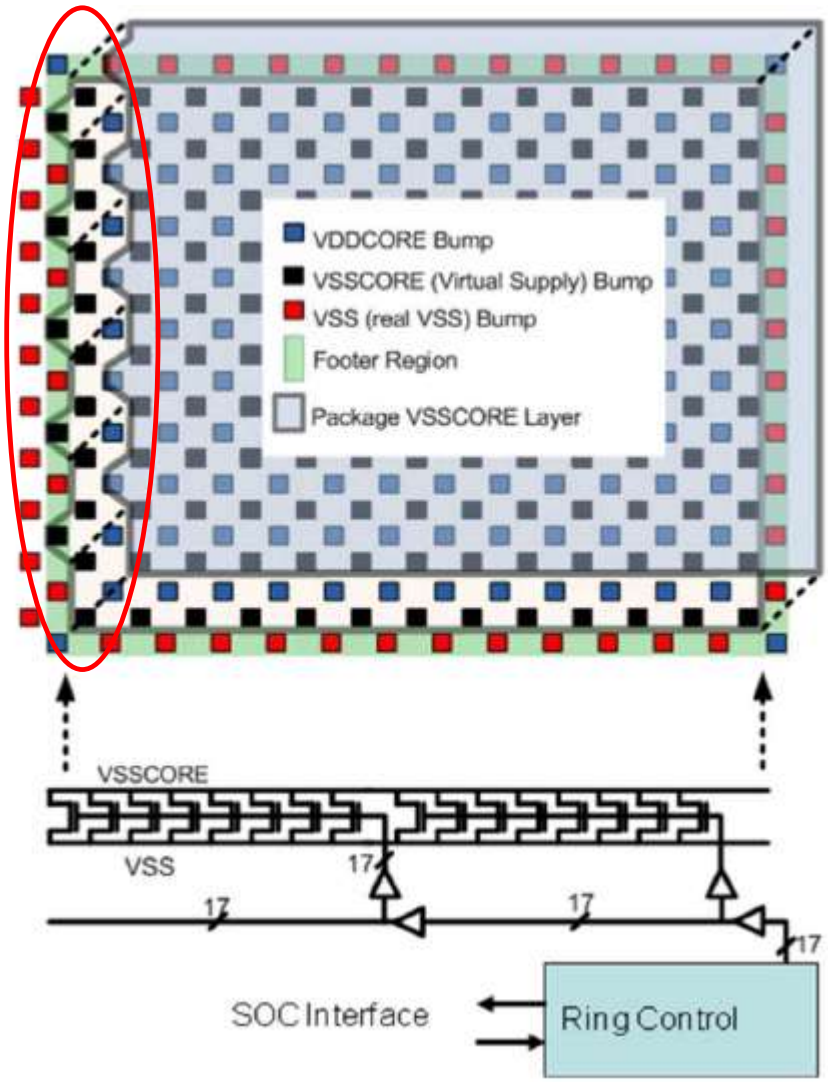
Remarks to the implementation of power gating in Llano-1 [14], [23]

1) The decision to power-gate VSS (ground) is a design decision, instead VDD could also be chosen to power-gate.

2) In Llano the power gates are arranged on one side (on the left side in the Figure) in zigzag pattern rather than along a line to increase contact density.

Note

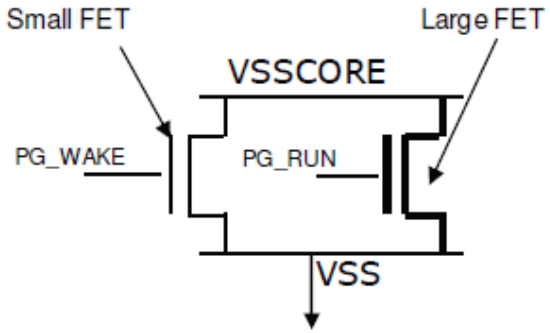
The switching transistors (power gates) connect/ isolate the VSS plane (red squares) to/from the VSSCORE plane (black squares).



3.4 Microarchitecture enhancements aiming at reducing power consumption (11)

Remarks to the implementation of power gating in Llano-2 [14], [23]

3. The NFET switching transistors are built up in fact of two switching transistors, termed as the Small FET and the Large FET.



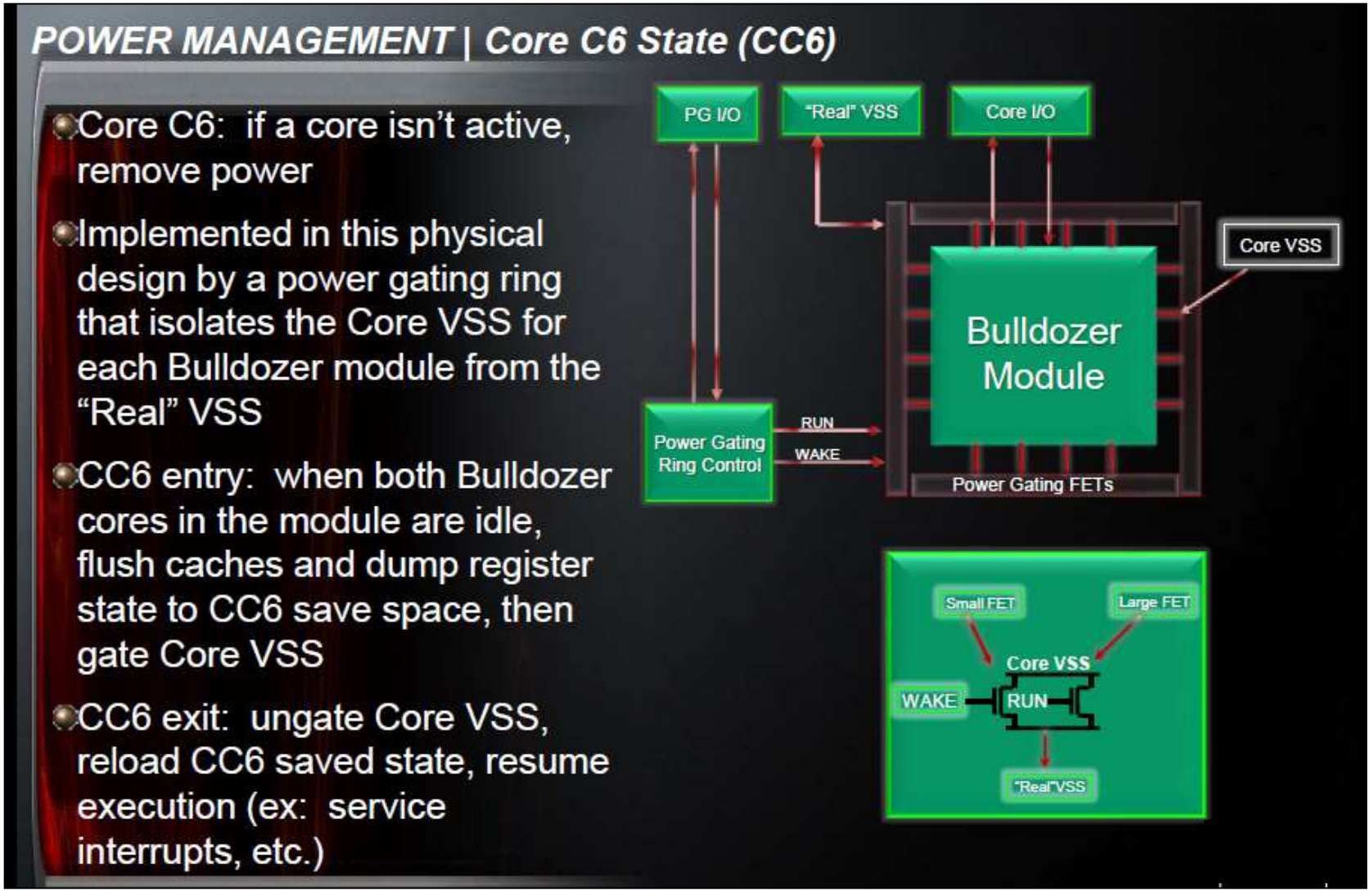
On power-on, first the Small FETs are enabled allowing the core to power up while limiting the di/dt transient current to reduce effects on neighboring circuits.

Subsequently, the Large FETs are also enabled to provide a low-resistance path (~ 1.1 mΩ) to VSS for core operation.

3.4 Microarchitecture enhancements aiming at reducing power consumption (12)

Remarks to the implementation of power gating in Llano-3 [25]

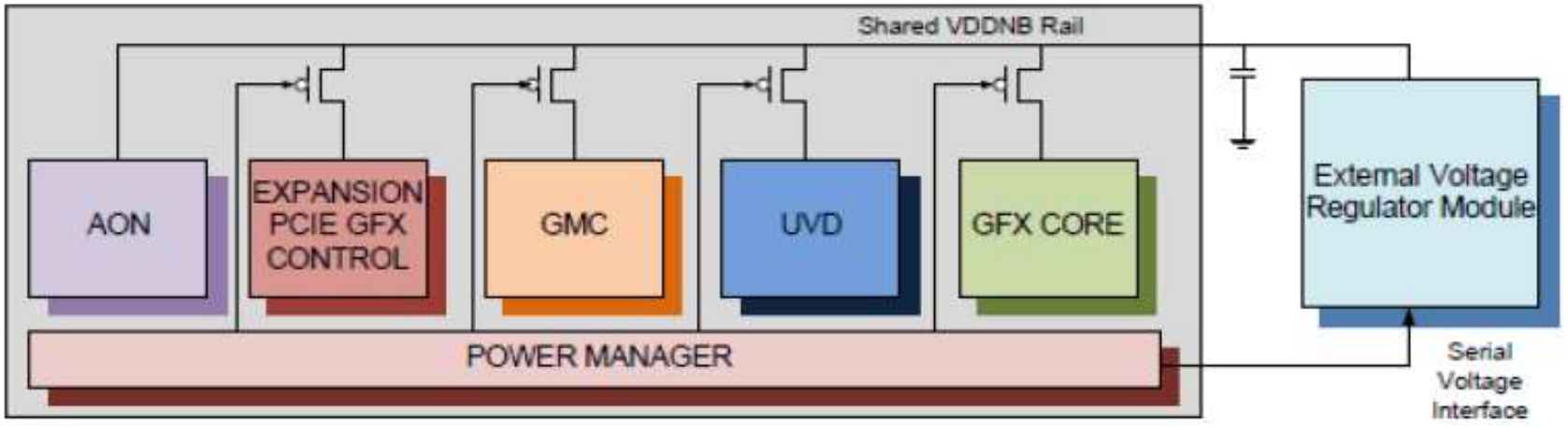
4) AMD's Bulldozer makes use of the same technology to implement power gating [25]



Use of power gating beyond CPU cores and L2 caches in Llano [12]

In Llano AMD power-gates virtually all units, such as

- the Graphics Core (GFX)
- the Graphics Memory Control (GMC)
  (when memory is in self-refresh)
- the Unified Video Decoder (UVD)
- the x16 PCIe Graphics Expansion Controller.

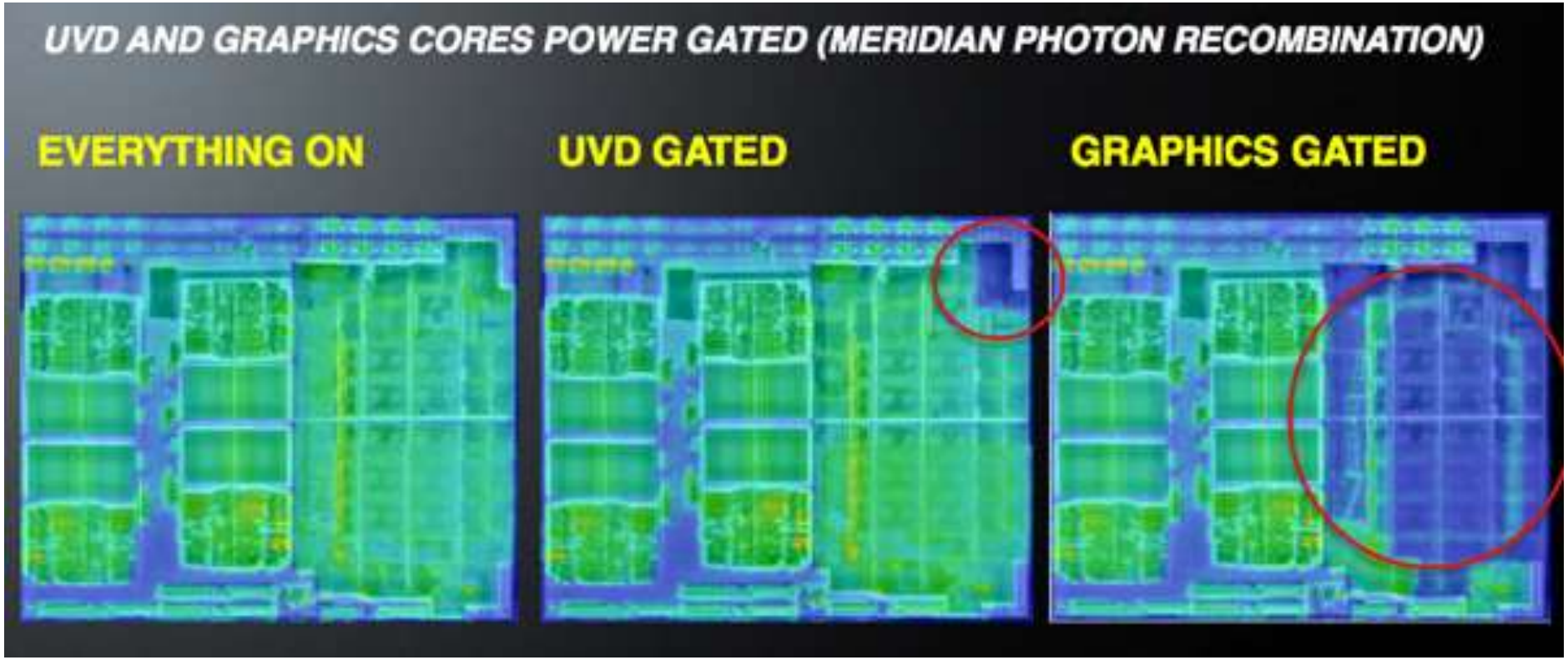


AON: Always on – refers to logic that is not power gated

The GFX and GMC units have dynamic (hardware) power gating whereas power gating of the other units is static, i.e. done under driver control.

3.4 Microarchitecture enhancements aiming at reducing power consumption (14)

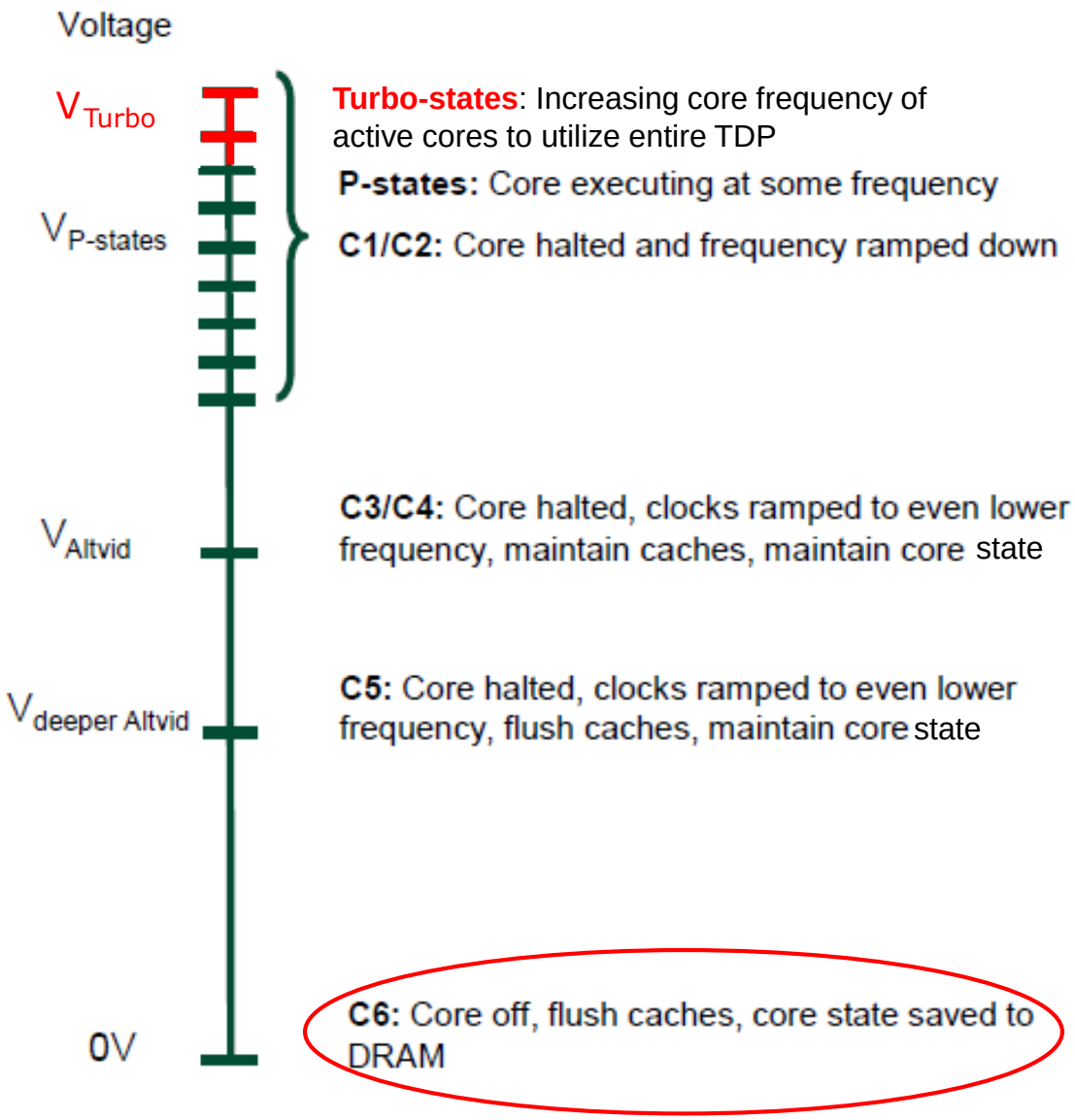
The effect of power gating the UVD (Unified Video Decoder) and GFX (GPU) units [18]



c) Core C6 state (CC6 state)

Overview of core P/C states

(Based on [22])



Core C6 state (CC6 state) [23], [12]

Preconditions for entering the CC6 state-1

- The CC6 state will be initiated by the OS when it requests the Halt state or a deeper C-state.
- The CC6 state is however a deeper C-state with the penalty of having long entry and exit times in the order of tens of μs due to the fact that before entering the CC6 state, i.e. before powering down the core, the core architectural state and the contents of the L2 cache needs to be flushed to main memory and this context needs to be restored before resuming execution.

Preconditions for entering the CC6 state-2

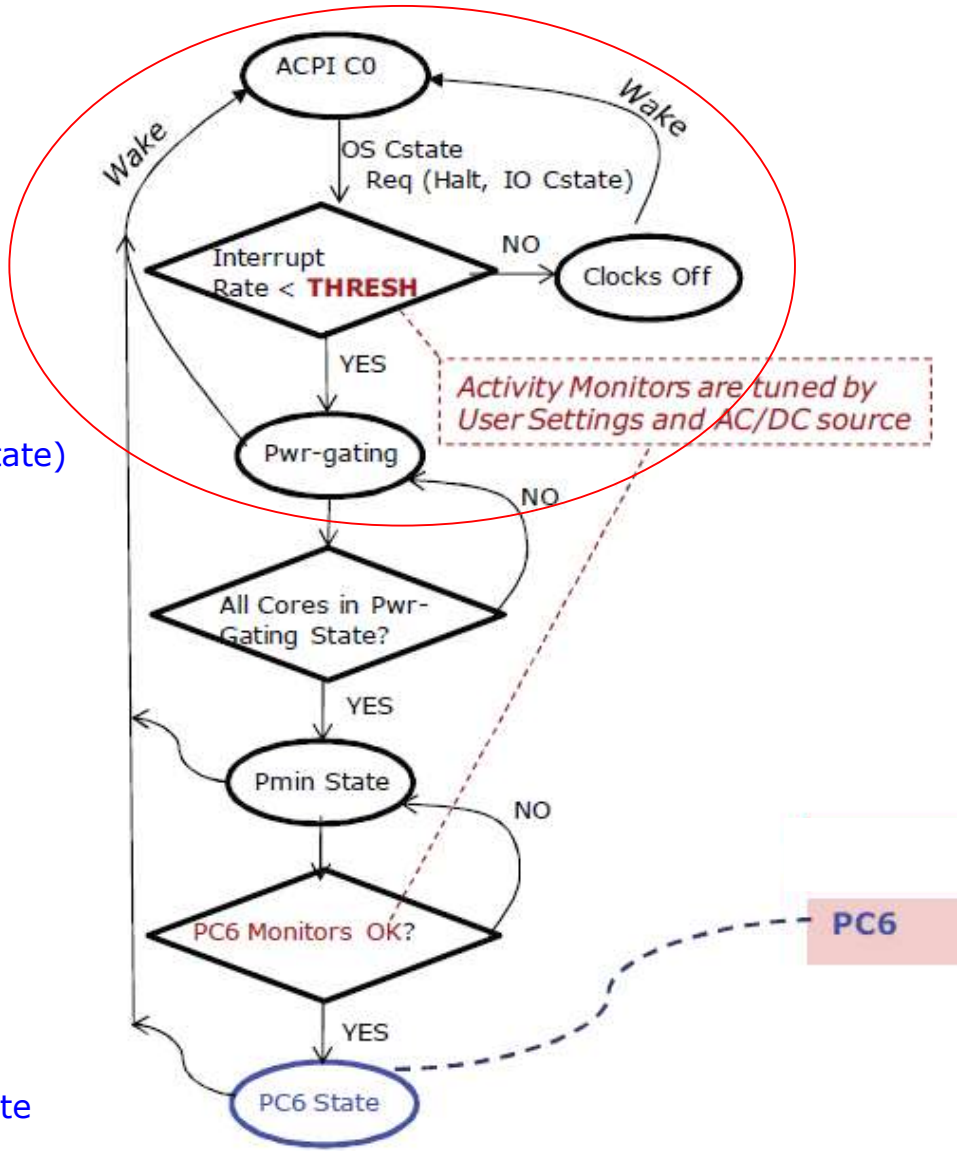
- There is an energy cost for saving and restoring the states of the core and its L2.
- On the other hand interrupts may wake up the system requesting a restoration of the saved context of the core and L2.

  Obviously, activating the CC6 state in the presence of a high interrupt activity may lead to a performance degradation and also to a reduction of the performance/power ratio due to the resulting longer interrupt service times.
- Therefore, the Power Management Controller (PMC) of Llano maintains a set of activity monitors, like the Interrupt Rate Tracker (IRT).

  IRT increments its counter if an interrupt arrives and decrements it at regular, pre-setable time intervals.

  Thus the contents of IRT represents the actual interrupt activity.
- PMC will initiate a CC6 state entry if the OS requests the halt state or a deeper C-state and the interrupt activity is lower than a given threshold else PMC will initiate a low power C state with clock-gating.

State transition diagram for the Core C6 state (CC6 State) [23]



The sequences of entering and exiting the CC6 state [14], [12]

CC6 entry sequence

- L1 and L2 caches are flushed to system memory
- The micro-architectural state of the core is saved in system memory
- CPU clocks are stopped
- The PLL of the CPU is powered down
- The core is powered down by isolating VSSCORE from VSS through power gating.

CC6 exit sequence

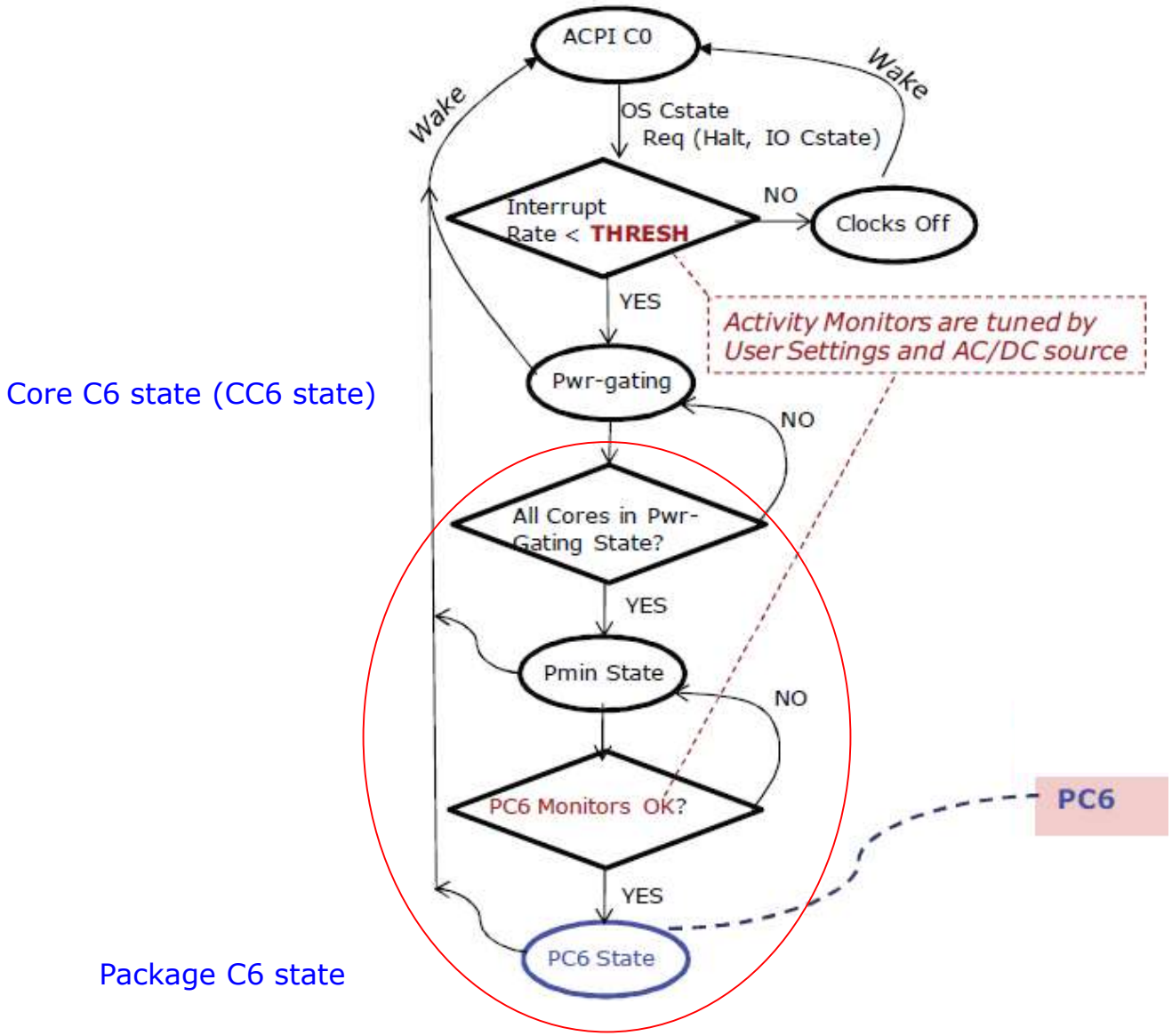
- Power up and lock core PLL
- Power up the core by activating power gating
- Set up clock frequency
- Run reset microcode
- Restore L1 and L2 from the system memory
- Restore the micro-architectural state of the core from the system memory
- Now the core is ready to resume execution

d) Package C6 state (PC6 state) [12], [23]

Entry into the PC6 state-1

- When all cores are already power-gated the PMC can consider to reduce VDD to 0 V.
- As PC6 transitions introduce an extra 100-150 μs interrupt service latency due to the need to ramp up VDD to the operational level after waking up from the PC6 state, PMC makes use of an another set of activity monitors, called the Power gating monitors or PC6 monitors, to decide whether or not a transition to the PC6 state can be guessed as beneficial.

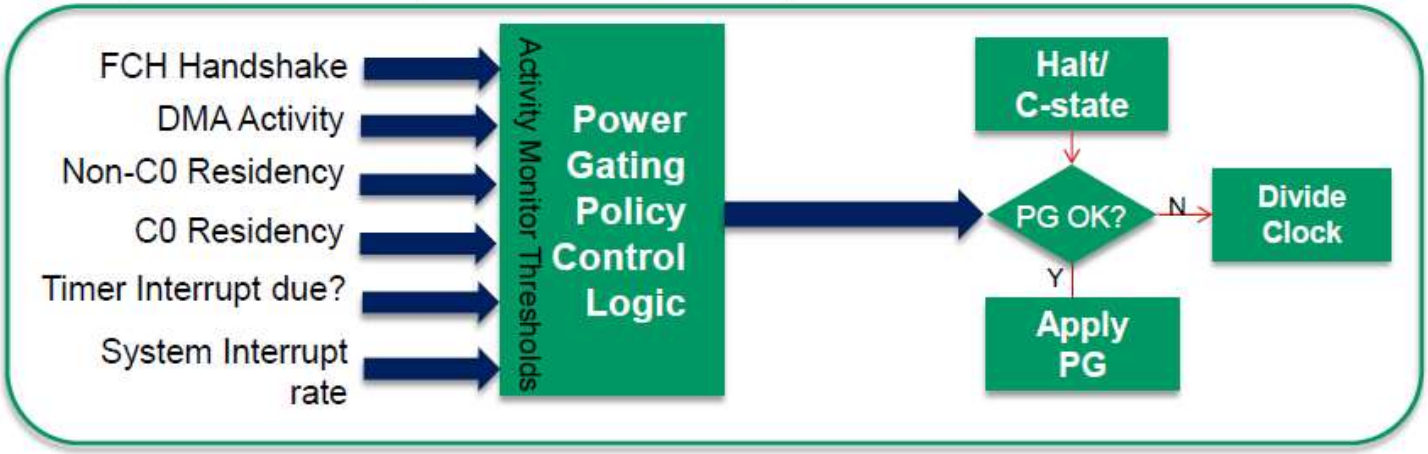
State transition diagram for the Package C6 state (PC6 State) [23]



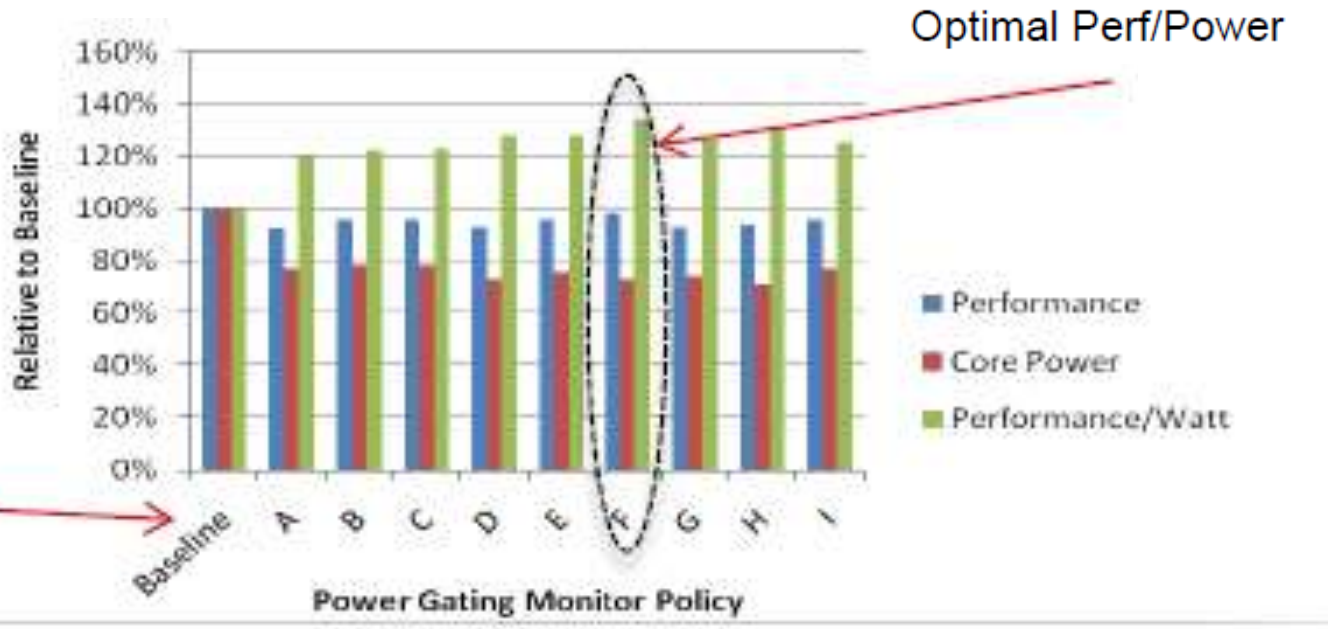
3.4 Microarchitecture enhancements aiming at reducing power consumption (22)

Power gating monitors [12]

- CC6 exit requires approximately 30µs
- PC6 exit can be >100µs (due to VRM power supply restoration)
- Power Gating Policy Control Logic monitors system activity to identify when power gating entry/exit latency will adversely affect performance



Choosing the optimal power gating monitor policy [12]



Different Monitor Policies evaluated for optimal Power/Performance across a variety of workloads

Package C6 state (PC6 state) [12], [23]

Entry into the PC6 state-2

- If PMC decides that a transition to the PC6 state would contribute to power saving, it initiates the entry into the PC6 state and removes VDD.
- Else it let's the core enter the Pmin state.

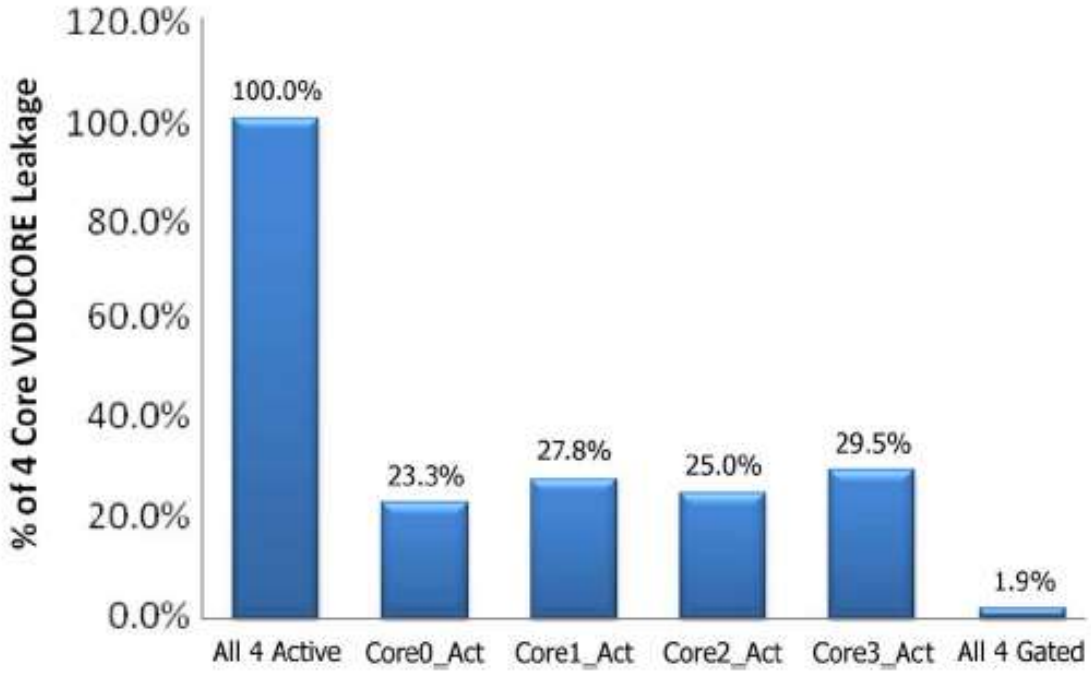
  In the Pmin state PMC reduces VDD in order to further lower leakage in the power gating structures and the remaining AON (Always ON) circuitry.

PC6 State residency while running applications [23]

PC6 (Package C6) APU State Residency

	BluRay	Youtube	Win Idle	3DMark06
PC6	37.98%	37.13%	98%	26.7%

Reduction of power consumption while utilizing the PC6 state [14]



(The measurement is taken with one core active and three with the power gate ring activated. The Figure shows the mean power reduction on more than 1300 die from multiple lots).

Note [18]

- Introducing power gating has an eminent influence on power consumption.
- Without power gating idle cores or units are clock gated.
  Clock gating however, does not reduce leakage currents, so with clock gating alone a considerable dissipation remains due to leakage currents.
- Power gating and associated CC6 as well as PC6 states are also prerequisites for an efficient Turbo Core technology since without implementing these power saving techniques the power headroom is typically too small to activate the Turbo Core technology effectively, i.e. in this case the Turbo Core technology can not contribute for a noteworthy performance boost.

3.5 Family 12h (Llano)-based desktop lines

3.5 Family 12h (Llano)-based Fusion desktop lines (1)

3.5 Family 12h (Llano)-based desktop lines

	Launched in	2008-2009	2011
		Family 11h (**Griffin**)	**Family 12h** (**Llano**)
Servers	**4P servers**		
	2P servers		
	1P servers		
	(85-140 W)		
Desktops	**High perf.** (~95-125 W)		
	Mainstream (~65-100 W)		Llano A8/A6/A4/E2 Sempron X2
	Entry level (40-60 W)		
Notebooks	**High perf.** (~30-60 W)	Turion X2 Ultra (ZM-xx) Turion X2 (RM-xx)	Llano A8 M
	Mainstream/Entry (~20-30 W)	Athlon X2 (QL-xx) Sempron (SI-xx)	Llano A6/A4/E2 M
	Ultra portable (~10-15 W)	Turion Neo X2 (L6xx) Turion X2 (RM-xx) Athlon Neo X2 (L3xx) Sempron (200U/210U)	
Tablet (~5 W)			
Embedded (~10 – 20 W)		Turion Neo X2 (L6xx) Athlon Neo X2 (L3xx) Sempron (200U/210U)	

3.5 Family 12h (Llano)-based Fusion desktop lines (2)

Family 12h (Llano)-based desktop lines – Overview [11]

Llano based desktop lines

Desktop Fusion APU models

- *Lynx desktop platform (65/100 W)*

  Fusion A/E2 series *(6/2011-12/2011)*
  2/4 C, 512 KB/1 MB per C, GPU, 65/100 W

Turbo Core on select desktop models

GPU-less desktop models

Lynx desktop platform (65/100 W)

- ***Athlon II X4 6xx****, (8/2011- 2/2012)*
  4C, 1 MB/C, 65/100 W
- ***Athlon II X2 221****, (8/2011)*
  2C, 512 KB/C, 65 W
- ***Sempron 198****, /8/2011)*
  2C, 512 KB/C, 65 W

GPU disabled, no Turbo Core

Socket FM1

3.5 Family 12h (Llano)-based Fusion desktop lines (3)

Main features of the Family 12h (Llano)-based Fusion A8 high-performance desktop line

Base arch./ stepping		Intro	High perf. DT family	Series	Techn.	Core count (up to)	L2 (up to)	L3 (up to)	Memory (up to)	HT/ dir. (up to)	Socket
K8	CG	9/2003	Claw-Hammer	Athlon 64	130 nm	1	1 MB	-	DDR-400	HT 2.0: 4.0 GB/s	754/ 939
	E4	4/2005	San Diego	Athlon 64	90 nm	1	1 MB	-	DDR-400	HT 2.0: 4.0 GB/s	939
	E6	5/2005	Toledo	Athlon 64 X2	90 nm	2	2*1 MB	-	DDR-400	HT 2.0: 4.0 GB/s	939
	E2/E3	5/2006	Windsor	Athlon 64 X2	90 nm	2	2*1 MB	-	DDR2-800	HT 2.0: 4.0 GB/s	AM2
K10	B2 B3	11/2007 3/2008	Agena	Phenom X4	65 nm	4	4*½ MB	2 MB	DDR2-1066	HT 3.0: 8.0 GB/s	AM2+
K10.5	C2 C2/C3	1/2009 2/2009	Deneb	Phenom II X4	45 nm	4	4*½MB	6 MB	DDR2-1066 DDR3-1333	HT 3.0: 8.0 GB/s	AM2+ AM3
	E0	4/2010	Thuban	Phenom II X6	45 nm	6	6*½MB	6 MB	DDR2-1066 DDR3-1333	HT 3.0: 8.0 GB/s	AM3
Fam. 11h (Griffin)		-	-	-	-	-	-	-	-	-	-
Fam. 12h (Llano)		6/2011	Llano	Fusion A8	32 nm	4	4*1 M	-	DDR3-1866	UMI: 5 GT/s	FM1
Fam. 14h (Bobcat)		-	-	-	-	-	-	-	-	-	-
Fam. 15h Models 00h-0Fh (Bulldozer)		10/2011	Zambezi	FX-series	32 nm	4 CM (8 C)	4x2 MB/CM	8 MB	DDR3-1866	HT 3.1: 12.8 GB/s	AM3+
Fam. 15h Models 10h-1Fh (Piledriver)		10/2012	Vishera	FX-series	32 nm	4 CM (8 C)	4*2 MB/CM	8 MB	DDR3-1866	HT 3.1: 12.8 GB/s	AM3+
No further Fam. 15h based lines		-	-	-	-	-	-	-	-	-	-

3.5 Family 12h (Llano)-based Fusion desktop lines (4)

Family 12h Llano-based desktop Fusion APU lines

Platform segment			Core count	L2	DDR3	GPU
Desktops	Mainstream	A8	4C	4*1MB	DDR3-1866	HD 6530D
		A6	4C	4*1MB	DDR3-1866	HD 6530D
			3C	3*1MB	DDR3-1866	HD 6530D
		A4	2C	2*512KB	DDR3-1600	HD 6410D
		E2	2C	2*512KB	DDR3-1600	HD 6370D

6/11

Llano
228 mm^2, 1450 mtrs
Turbo Core on select models
FM1 65/100W

A8-38xx

A6-36xx

A6-35xx

A4-3xxx

E2-3200

2011

3.5 Family 12h (Llano)-based Fusion desktop lines (5)

Family 12h Llano-based GPU-less desktop lines

	Platform segment		Core count	L2	DDR3
Desktops	Mainstream	Athlon II	4C	4*1MB	DDR3-1866
			2C	2*512KB	DDR3-1600
		Sempron	2C	2*512KB	DDR3-1600

8/11

Llano
228 mm^2, 1450 mtrs
GPU disabled, no Turbo Core
65/100W, FM1

X4 6xx

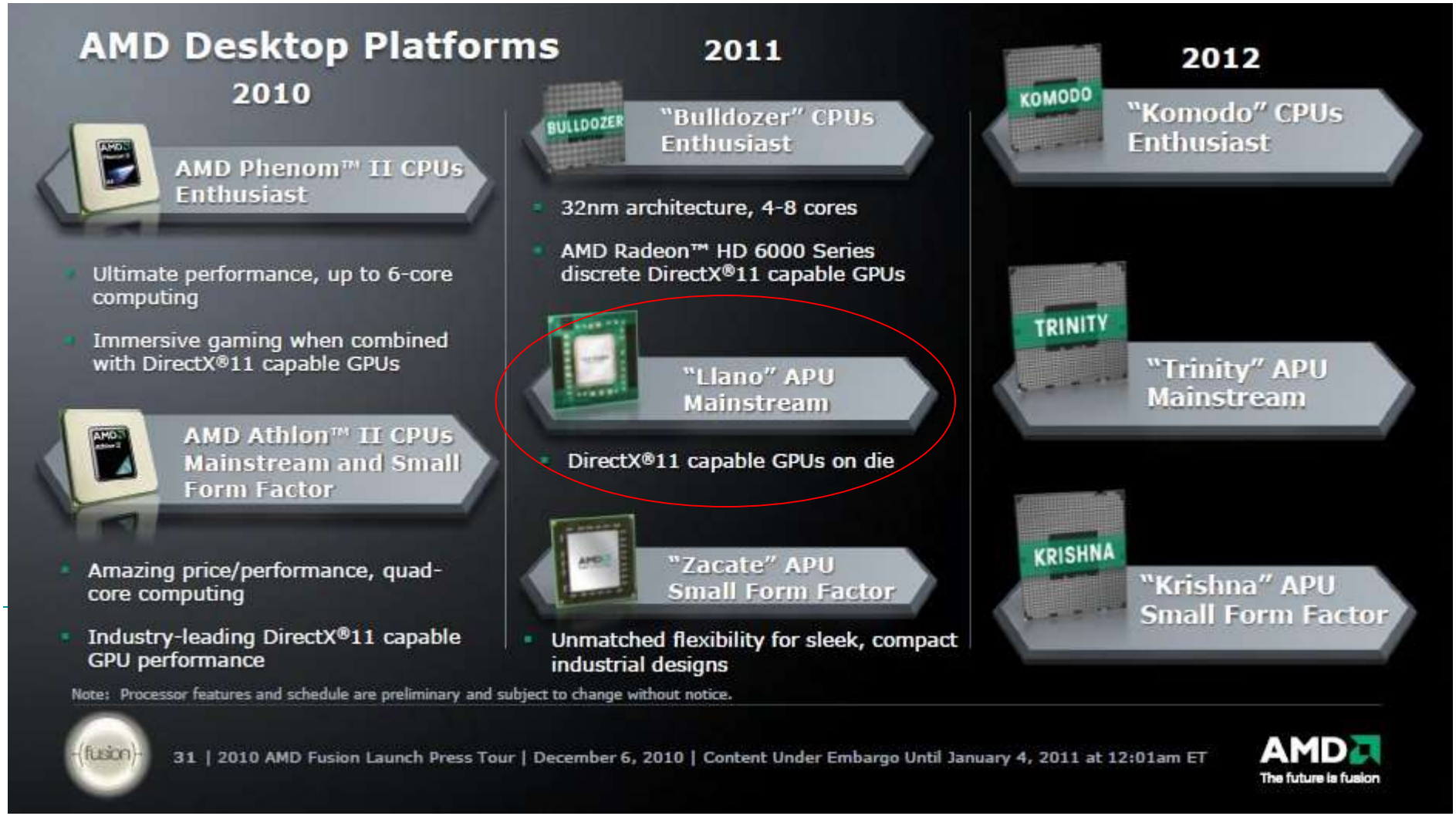
X2 2xx

X2 198

2011

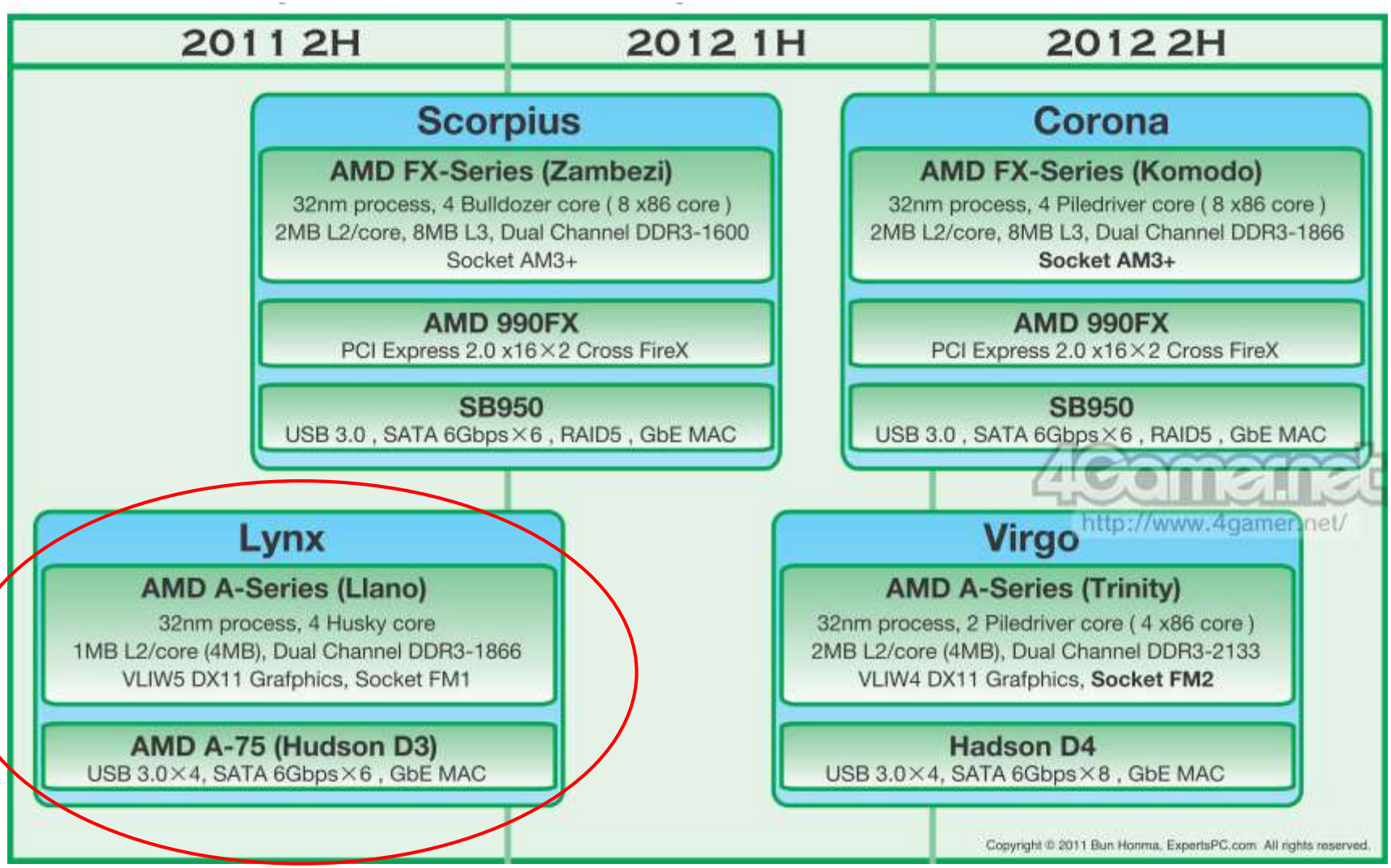
3.5 Family 12h (Llano)-based Fusion desktop lines (6)

Family 12h (Llano)-based desktop lines on AMD's desktop roadmap [26]



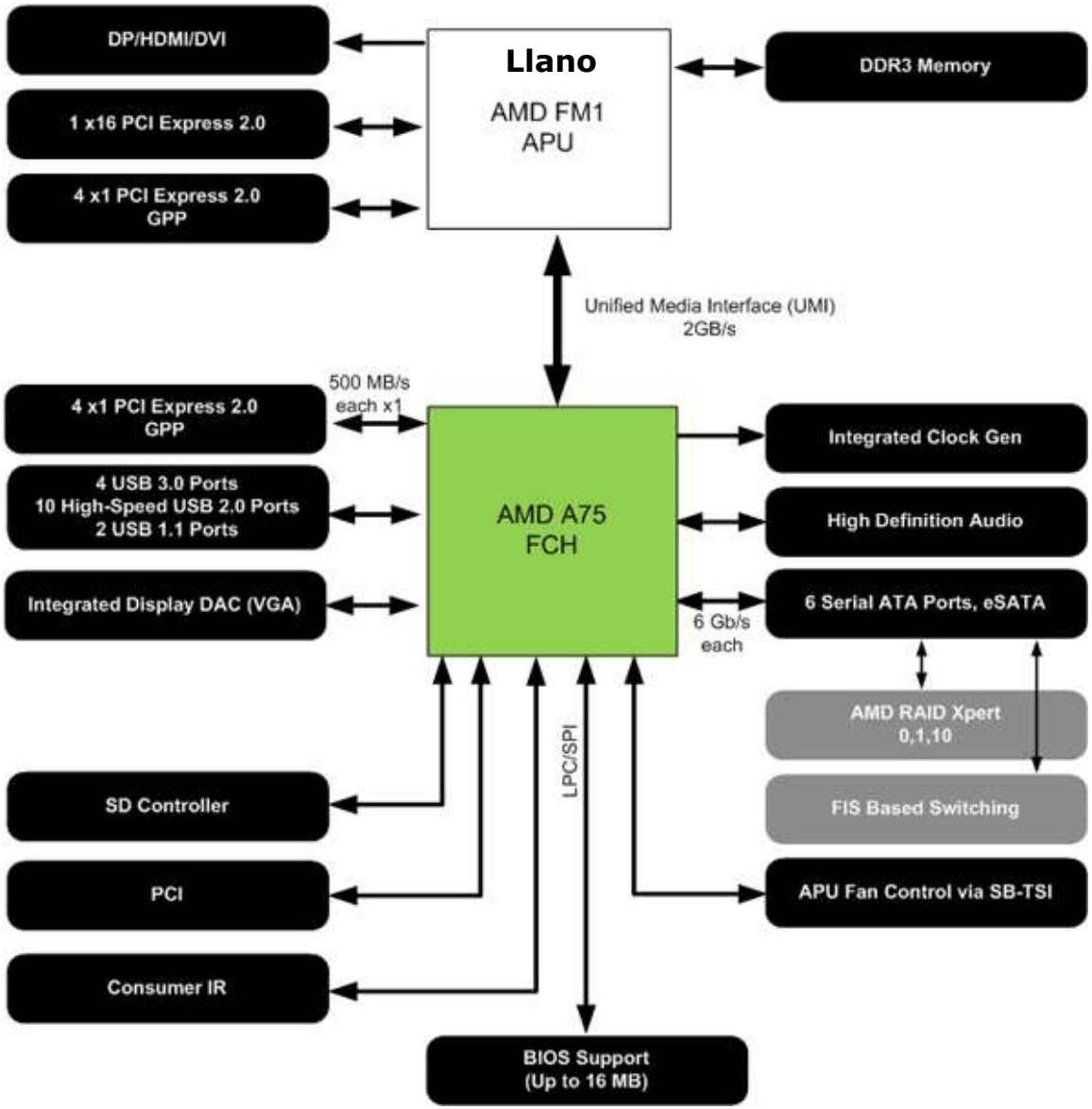
3.5 Family 12h (Llano)-based Fusion desktop lines (7)

AMD desktop platform roadmap [33]



3.5 Family 12h (Llano)-based Fusion desktop lines (8)

AMD's Llano-based mainstream desktop platform [17]



3.6 AMD’s Family 12h (Llano)-based Fusion mobile lines

3.6 AMD's Family 12h (Llano)-based Fusion mobile lines

	Launched in	2008-2009	2011
		Family 11h (**Griffin**)	**Family 12h** (**Llano**)
Servers	**4P servers**		
	2P servers		
	1P servers		
	(85-140 W)		
Desktops	**High perf.** (~95-125 W)		
	Mainstream (~65-100 W)		Llano A8/A6/A4/E2 Sempron X2
	Entry level (40-60 W)		
Notebooks	**High perf.** (~30-60 W)	Turion X2 Ultra (ZM-xx) Turion X2 (RM-xx)	Llano A8 M
	Mainstream/Entry (~20-30 W)	Athlon X2 (QL-xx) Sempron (SI-xx)	Llano A6/A4/E2 M
	Ultra portable (~10-15 W)	Turion Neo X2 (L6xx) Turion X2 (RM-xx) Athlon Neo X2 (L3xx) Sempron (200U/210U)	
Tablet (~5 W)			
Embedded (~10 – 20 W)		Turion Neo X2 (L6xx) Athlon Neo X2 (L3xx) Sempron (200U/210U)	

3.6 AMD's Family 12h (Llano)-based Fusion mobile lines (2)

Positioning of AMD's high performance Family 12h mobile APU lines

Base arch./ stepping		Intro	High perf. mobile family	Series	Techn.	Core count (up to)	L2 (up to)	L3	Memory (up to)	HT/ dir. (up to)	Sock et
K8	C0, CG	9/2003	Claw-hammer	Mobile Athlon 64	130 nm	1	512 KB	-	DDR-400	HT 1.0: 3.2 GB/s	754
	E5	3/2005	Lancaster	Turion 64	90 nm	1	1 MB	-	DDR-400	HT 1.0: 3.2 GB/s	754
	F2	5/2006	Trinidad	Turion 64 X2	90 nm	2	2*½ MB	-	DDR2-667	HT 1.0: 3.2 GB/s	S1
K10.5	DA-C2	9/2009	Caspian	Turion II	45 nm	2	2*½ MB/ 2*1 MB[1]	-	DDR2-800	HT 3.0: 7.2 GB/s	S1g3
	DA-C3	5/2010	Champlain	Turion X4	45 nm	4	4*½ MB	-	DDR3-1066	HT 3.0: 7.2 GB/s	S1g4
Fam. 11 (Griffin)	B1	6/2008	Lion	Turion X2 Ultra	65 nm	2	2x½ MB/ 2*1 MB[2]	-	DDR2-800	HT 3.0: 10.4 GB/s	S1g2
Fam. 12 (Llano)	B0	6/2011	Llano APU	Fusion A8 M	32 nm	4	4x1 MB	-	DDR3-1600	-	FM1
Family 15h Mod. 10h-1Fh (Piledriver)		5/2012	Trinity APU	A10-A4 M	32 nm	2 CM (4C)	2 MB/CM	-	DDR3-1600	PCIe 2.0x16 UMI	FS1r2
Family 15h Mod. 20h-2Fh (Piledriver)		2/2013	Richland APU	A10-A4 M	32 nm	2 CM (4C)	2 MB/CM	-	DDR3-1866	PCIe 2.0x16 ???UMI	FS1r2
Family 16h (Jaguar)		H1/2013	Kabini APU (SOC)	A/E Series	28 nm	2 CM (4C)	2 MB shared	-	DDR3-1866	PCIe ???	BGA

[1]: 2*512 KB for Turion II, 2*1 MB for Turion II Ultra
[2]: 2*512 KB for Turion X2, 2*1 MB for Turion X2 Ultra

UMI: Universal Media Interface

3.6 AMD's Family 12h (Llano)-based Fusion mobile lines (3)

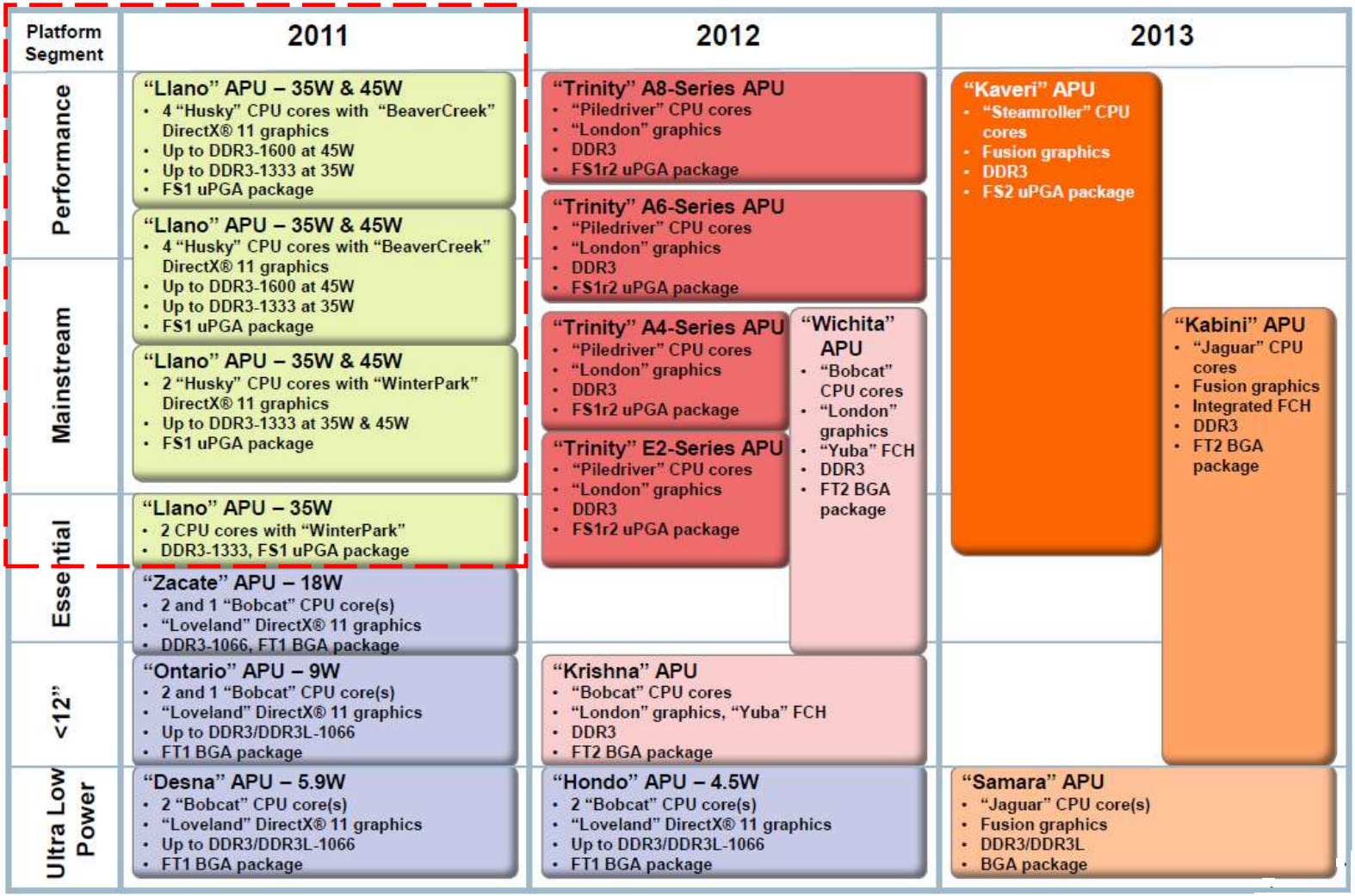
Family 12h Llano-based mobile APU lines

	Platform segment		Core count	L2	GPU	
						6/11 **Llano** 228 mm², 1480 mtrs DDR3L-1333 Up to DDR3-1600 Integrated PCIe 2.0 contr. Turbo Core ~~35/45 W~~
M o b i l e s	Performance	A8	4C	4*1MB	HD 6620G	A8-35xxM
	Mainstream	A6	4C	4*1MB	HD 6520G	A6-34xxM
		A4	2C	2*1MB	HD 6480G	A4-33x0M
				2*512KB	HD 6480G	A4-3305M
	Essential	E2	2C	2*512KB	HD 6380G	E2-3000M

2011

3.6 AMD's Family 12h (Llano)-based Fusion mobile lines (4)

Family 12h Llano-based mobile APU lines on AMD's mobile roadmap [27]

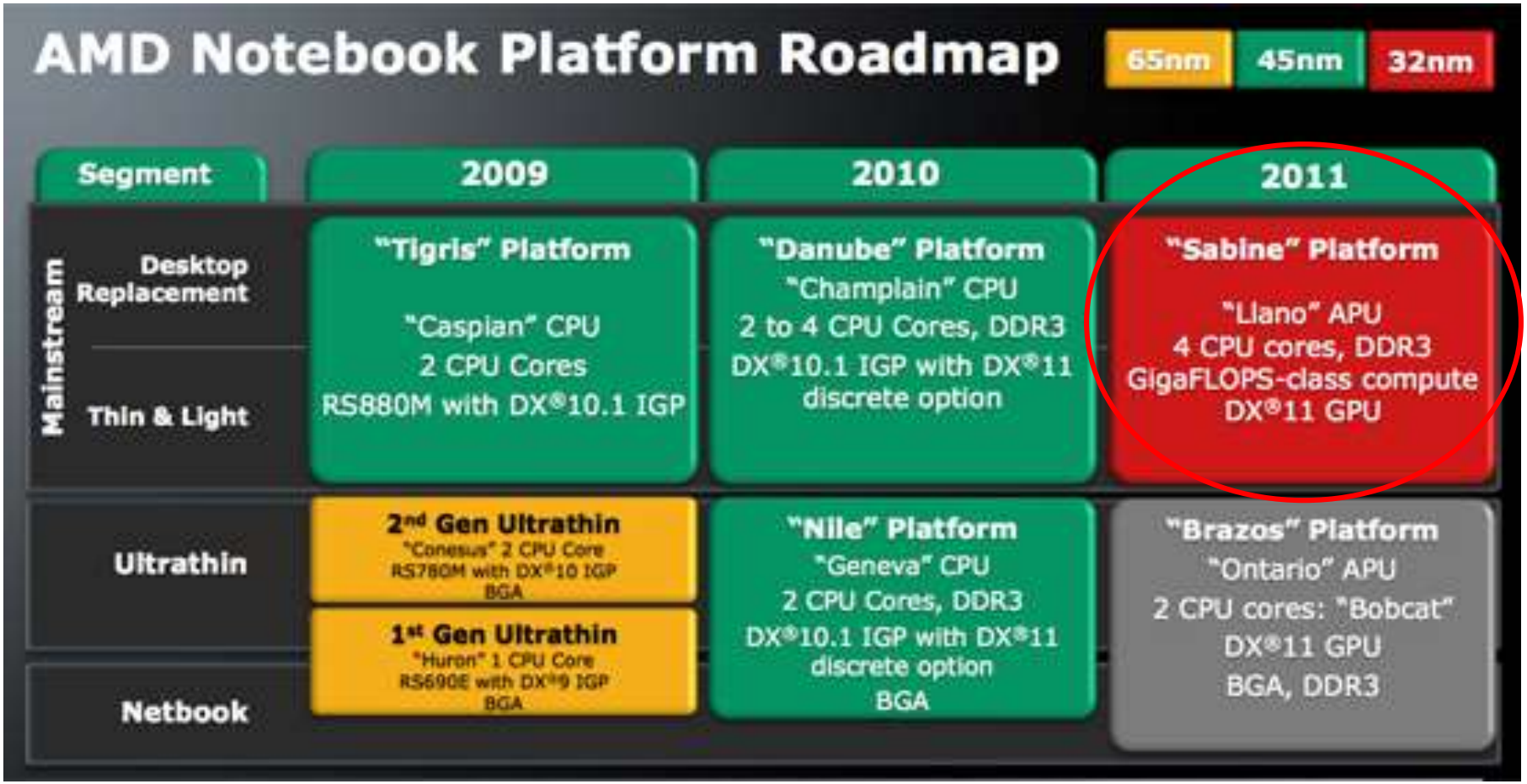


Note: Processor features and schedule are preliminary and subject to change without notice.

Mobile Client Solutions July 2011

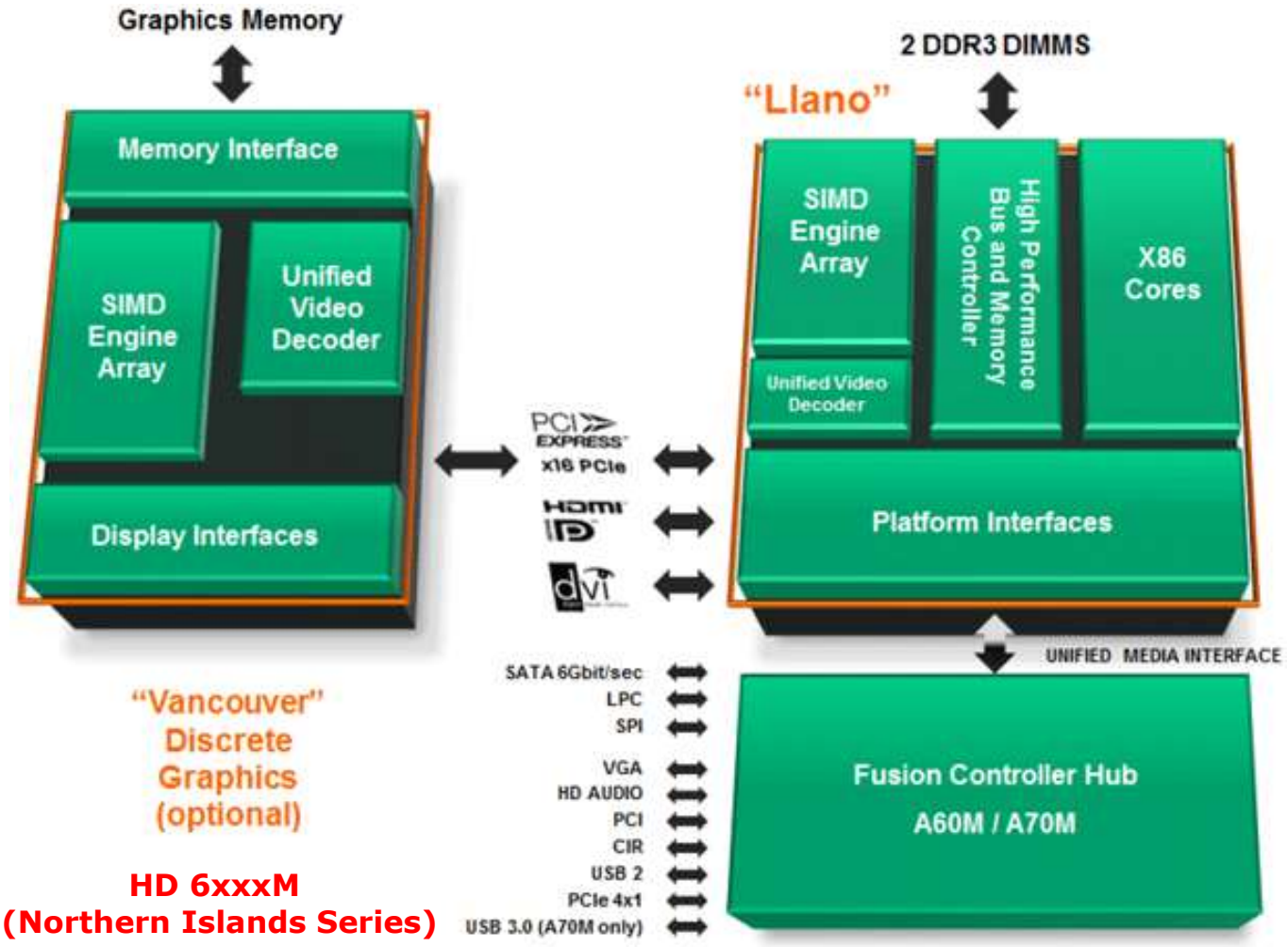
3.6 AMD's Family 12h (Llano)-based Fusion mobile lines (5)

The Llano-based Sabine mainstream notebook platform [34]



3.6 AMD's Family 12h (Llano)-based Fusion mobile lines (6)

Sabine mainstream notebook platform with optional HD 6xxxM discrete graphics [15]



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