

AMD's processor lines belonging to the
low-power oriented Cat family
(Families 14h/16h)

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AMD's processor lines belonging to the low-power oriented Cat family (Families 14h/16h)

- 1. Introduction to AMD's low power oriented processor lines
- 2. Family 14h Models 00h-0Fh (Bobcat-based) APU lines
- 3. Family 16h Models 00h-0Fh (Jaguar-based) APU lines
- 4. Family 16h Models 30h-3Fh (Puma+ based) APU lines
- 5. AMD's withdrawal from the mobile market
- 6. References

1. Introduction to AMD's low power oriented processor lines

1. Introduction to AMD's low power oriented processor lines (1)

1. Introduction to AMD's low power oriented processor lines

AMD's move to reshape their mobile and embedded market strategy -1

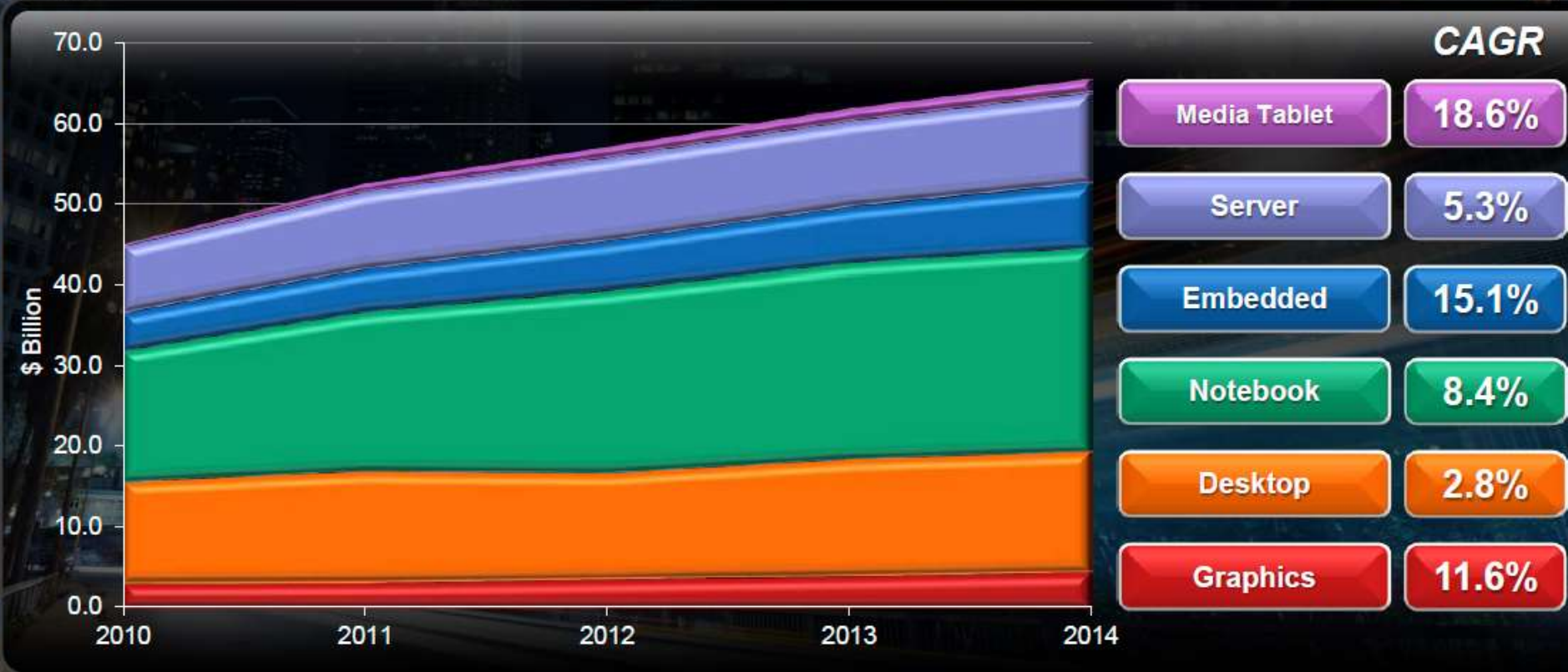
- a) About 2011 AMD recognized the [immensely increasing role of the mobile and embedded market segments](#), as demonstrated in one slide of their 2012 Financial Analyst Day presentations [1], shown below.

1. Introduction to AMD's low power oriented processor lines (2)

AMD's view of worldwide turnover and growth rate of different processor segments [1]

TREMENDOUS MARKET OPPORTUNITY

CAGR: Compound Annual Growth Rate



1. Introduction to AMD's low power oriented processor lines (3)

AMD's move to reshape their mobile and embedded market strategy -2

- b) In 1/2011 AMD's CEO (Chief Executive Officer) and President Dirk Meyer resigned mainly due to his alleged ignorance of the netbooks, handheld and embedded market space.
- c) In 2011/2012's roadmaps and product announcements AMD put much more emphasis on mobile, laptop and embedded products, and also
- d) In 1/2012 AMD re-branded their Fusion APU concept to Heterogeneous Systems Architecture (HAS) to indicate their broader scope of interest (broader than alone considering accelerated graphics) on the processor market.

Remarks

- Dirk Meyer was an outstanding processor architect, he has co-designed three very successful processors; DEC's Alpha 21064, 21264 as well as AMD's Athlon processors.
- In his role as CEO (2008-2011) he focused on the PC and data center market and intended to address the mobile and consumer electronics markets later [16].

1. Introduction to AMD's low power oriented processor lines (4)

AMD's revised concept for addressing the breadth of the processor market -1

Traditionally, AMD covered all market segments by the same processor design typically with two alternative implementations, including

- **one full-fledged processor design** that addresses the performance oriented server and desktop segments and **a number of low cost, low power design** for the mainstream desktop to the mobile segments, **as derivatives of the full-fledged basic architecture.**
- These derivative designs **provide typically less resources**, such as less cores, smaller L2 cache size or lack of the L3 cache, and **are running at lower clock speeds.**
All in all these designs provide **lower power consumption at lower price and performance.**

1. Introduction to AMD's low power oriented processor lines (5)

Example

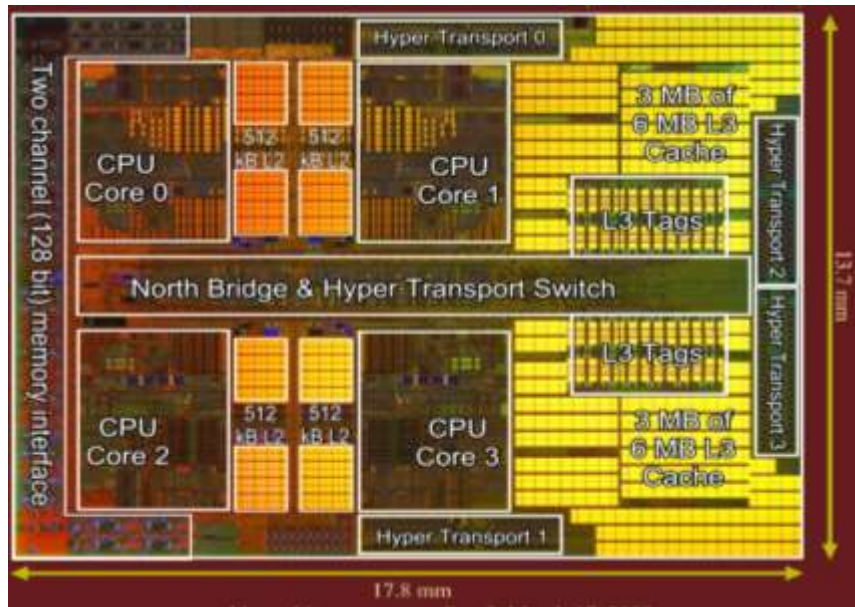
AMD's K10.5 Shanghai based server-, desktop- and mobile lines -1

As shown below

- a) the Shanghai-based high performance desktop core (Deneb) is obviously based on the original Shanghai core,

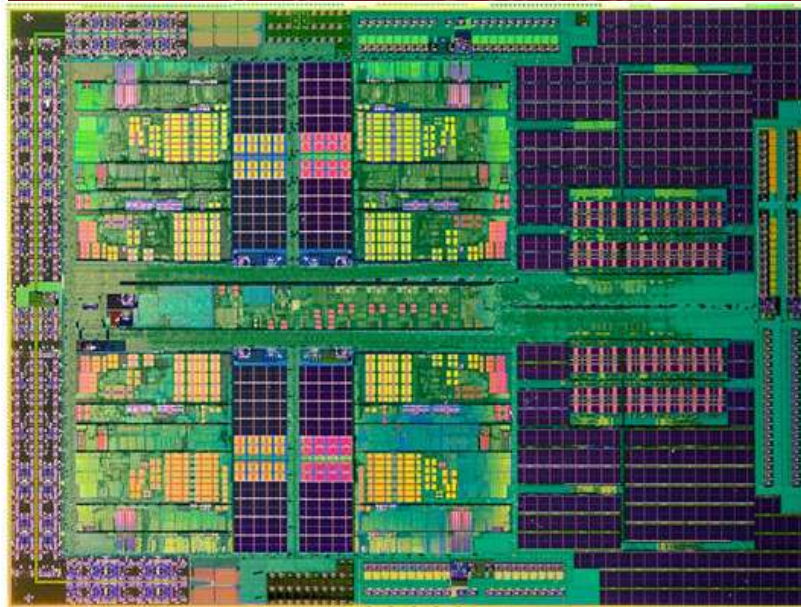
1. Introduction to AMD's low power oriented processor lines (6)

Contrasting the K10.5-based Shanghai server and Deneb desktop dies



Shanghai core [17]

4 C
L2: 512 KB/C
L3: 6 MB
258 mm², 758 mtrs



Deneb core [18]

4 C
L2: 512 KB/C
L3: 6 MB
258 mm², 758 mtrs

1. Introduction to AMD's low power oriented processor lines (7)

AMD's K10.5 Shanghai based server-, desktop- and mobile lines -2

- b) the K10.5 Shanghai-based mainstream and value desktop cores (Propus, Regor) are L3-less derivatives of Deneb with reduced L2/Core cache size or core count.

1. Introduction to AMD's low power oriented processor lines (8)

AMD-s K10.5-based native desktop architectures

Deneb

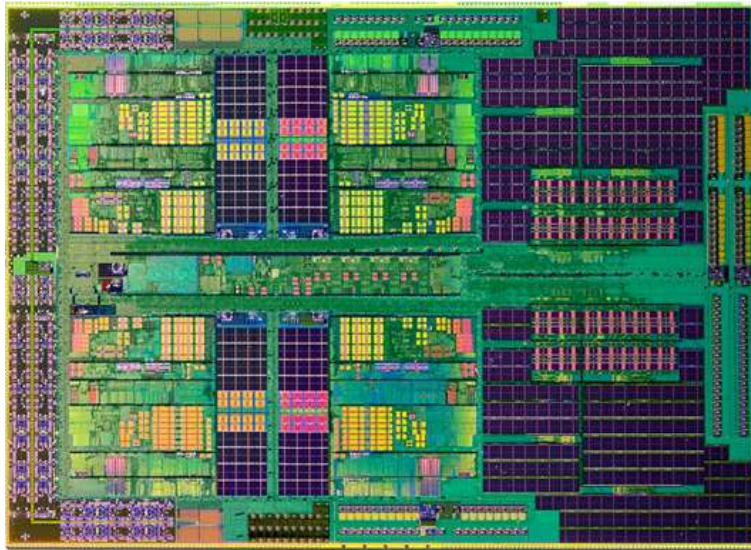
4 C
L2: 512 KB/C
L3: 6 MB
258 mm², 758 mtrs

Propus

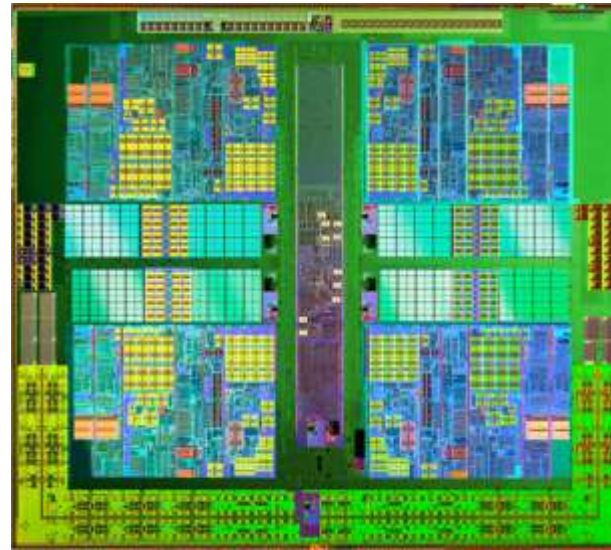
4C
L2: 512 KB/C
L3: -
169 mm², 300 mtrs

Regor

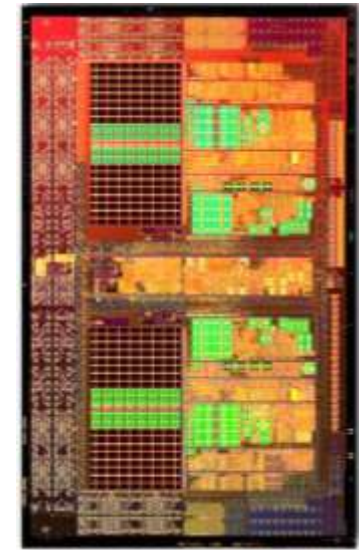
2C
L2: 1 MB/C
L3: -
117 mm², 234 mtrs



[18]



[19]



[20]

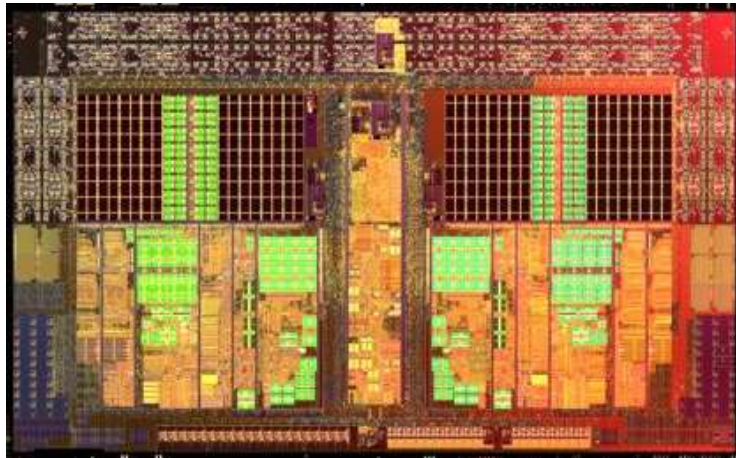
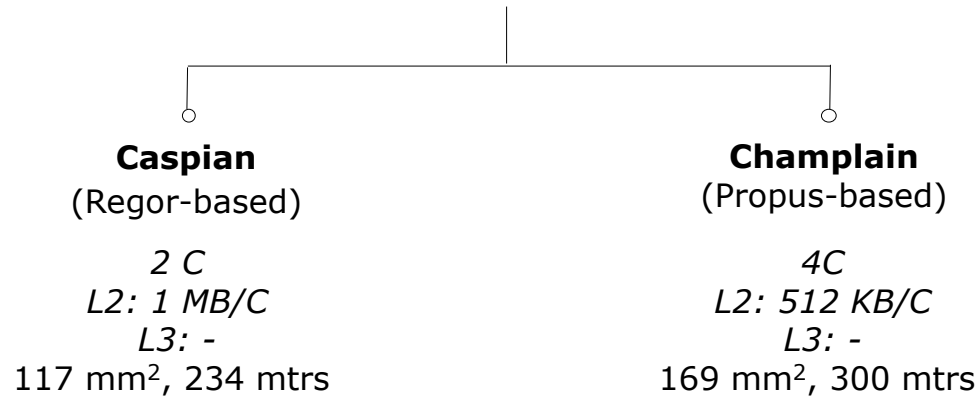
1. Introduction to AMD's low power oriented processor lines (9)

AMD's K10.5 Shanghai based server-, desktop- and mobile lines -2

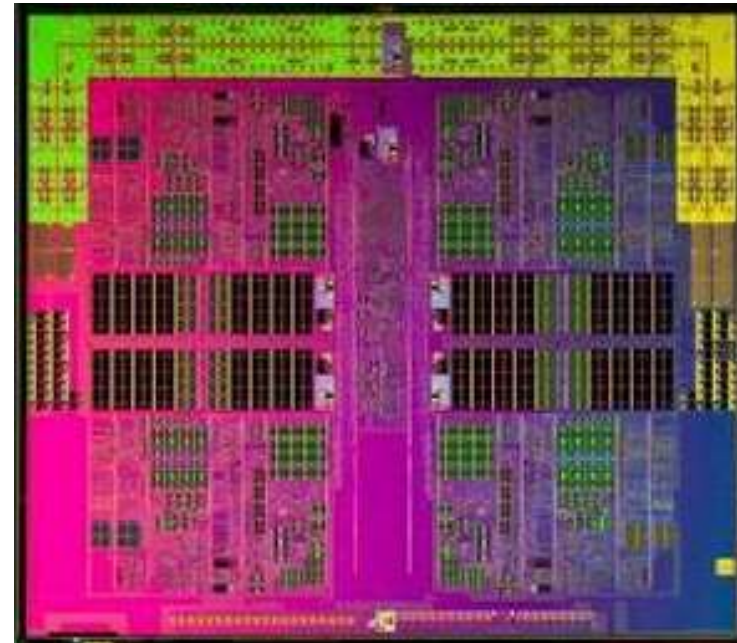
- c) The K10.5 Shanghai-based **mobile cores** (Caspian, Champlain) are then **derivatives of the mainstream and value desktop cores** (Regor and Propus).

1. Introduction to AMD's low power oriented processor lines (10)

AMD-s K10.5 Shanghai-based native mobile architectures



[21]



[22]

1. Introduction to AMD's low power oriented processor lines (11)

AMD's K10.5 Shanghai based server-, desktop- and mobile lines -2

To sum it up, despite of the wide variety of K10.5 Shanghai-based **server, desktop and mobile cores**, all of these designs are in fact **derivatives of the basic K10.5 Shanghai core**, i.e.

in their K10.5 Shanghai based cores AMD maintained in fact the same basic design.

1. Introduction to AMD's low power oriented processor lines (12)

AMD's revised concept for addressing the breadth of the processor market -2

In 2011, along with the introduction of their Bobcat lines, AMD changed their design concept and opted henceforth for covering the wide processor market by **two distinct processor designs** rather than one in order to better optimize power and performance features of their lines [23].

According to the new concept

- the **Bulldozer design** focuses on the **performance oriented server and desktop market**, whereas
- the **Bobcat design** addresses the **low cost, low power mobile, entry-level desktop and embedded market**.

In addition, **desktop, mobile and embedded devices** provide basically an **integrated graphics** as well.

This is **in line with** AMD's visionary **Fusion system architecture concept**, announced after AMD's merger with ATI in 2006 that became renamed to the **Heterogeneous System Architecture concept** in 2012.

Remark

Intel made the same movement already in 2008 when they introduced their **Atom line**.

Since then Intel pursues two major designs lines;

- their major line that focuses on **performance oriented servers and desktops**, whereas
- their **Atom line** that addresses **low cost, low power mobile devices**.

1. Introduction to AMD's low power oriented processor lines (13)

Evolution of AMD's basic architectures

AMD's processors built on a Common Architecture with optimized micro-architectures

Optimized Power/Performance
Microarchitecture

AMD
Bulldozer
Family 15h

~10/2011

Bulldozer
Models 00h-0Fh
32 nm

~5/2012

Piledriver
Models 10h-1Fh
32 nm

1/2014

Steamroller
Models 30h-3Fh
28 nm

6/2015

Excavator
Models 60h-6Fh
28 nm

4-wide
out-of-order

Low Power
Microarchitecture

AMD
Family 14h/16h

1/2011

Bobcat
Family 14h Models 00h-0Fh
40 nm

5/2013

Jaguar
F. 16h M. 00h-0Fh
28 nm

4/2014

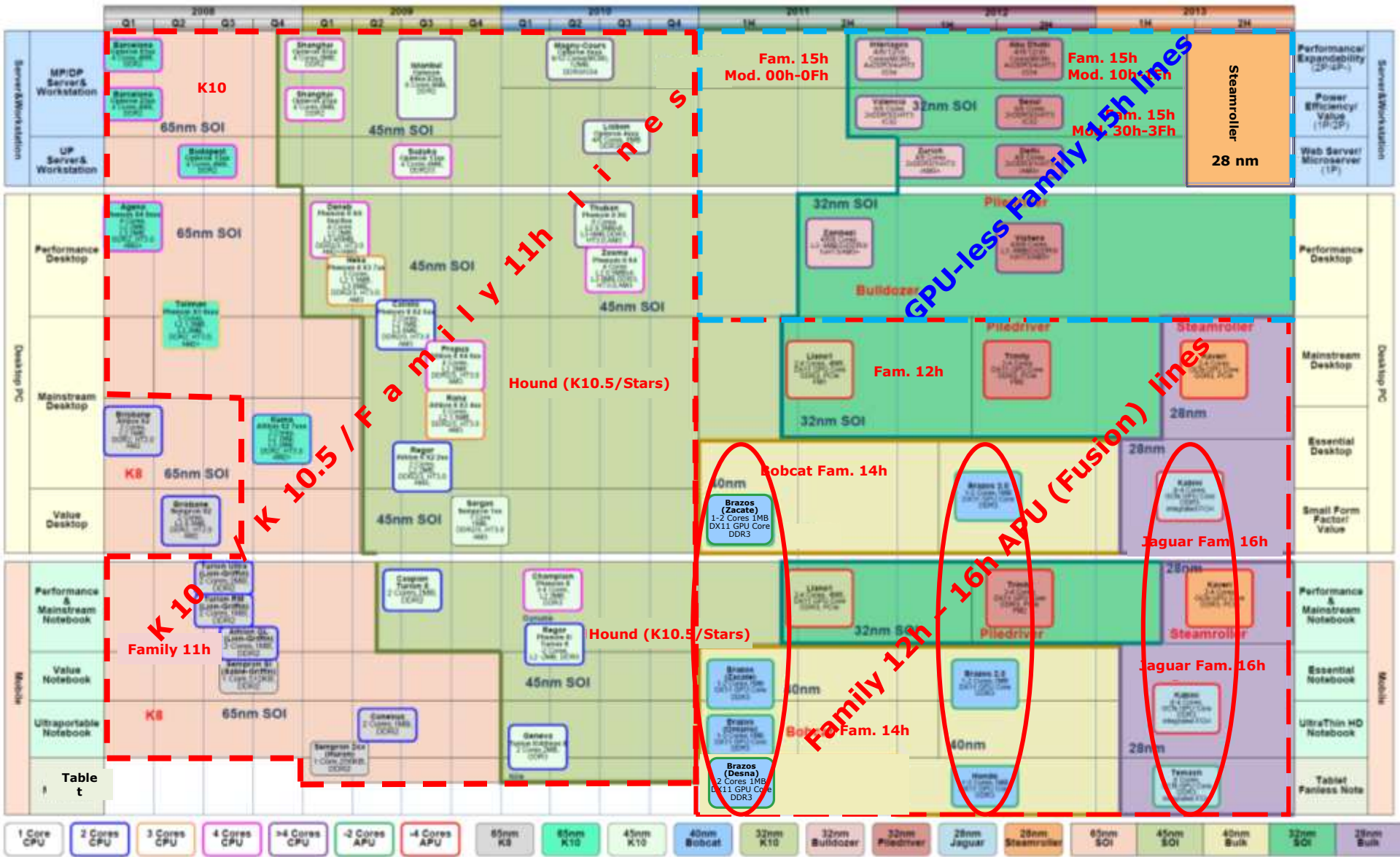
Puma+
Family 16h Models 30h-3Fh
28 nm

2-wide
out-of-order



1. Introduction to AMD's low power oriented processor lines (14)

Overview of AMD's low power oriented APU lines (embedded/microserver APUs not shown) [14]



1. Introduction to AMD's low power oriented processor lines (15)

Brand names of AMD's Family 14h and 16h processor lines

	Launched in	2011	2012	2013	2014	2015
		Family 14h (00h-0Fh) (Bobcat)	Family 14h (00h-0Fh) (Bobcat)	Family 16h (00h-0Fh) (Jaguar)	Family 16h (30h-3Fh) (Puma+)	Family 16h (30h-3Fh) (Puma+)
Servers	4P servers					
	2P servers					
	1P servers					
	(85-140 W)					
Desktops	High perf. (~95-125 W)					
	Mainstream (~65-100 W)					
	Entry level (~30-60 W)					
Notebooks	High performance/ mainstream/entry (~30-60 W)			Kabini A6		
	Ultra portable (~10-15 W)	Zacate E-Series Ontario C-Series	Zacate E1/E2	Kabini A/E-Series	Beema A/E-Series	Carrizo-L A/L-Series
	Tablet (~5 W)	Desna Z-Series		Temash A Series	Mullins A Series/E1	

1. Introduction to AMD's low power oriented processor lines (16)

Main features of AMD's Family 14h/16h (Cat-based) ultra-thin notebook processor lines

Base arch.	Intro	Ultra-thin mobile family	Series	Techn.	Core count (up to)	L2 (up to)	L3	GPU (APU)	Memory (up to)	TDP [W]	Socket
Family 14h (00h-0Fh) (Bobcat)	1/2011	Zacate (not SoC)	E Series	40 nm	2	512 KB/ core Private	-	Yes	DDR3L- 1333	18	FT1 (BGA)
	6/2012	Zacate (not SoC)	E1/E2 Models	40 nm	2	512 KB/ core Private	-	Yes	DDR3L- 1333	18	FT1 (BGA)
	1/2011	Ontario	C Series	40 nm	2	512 KB/ core private	-	Yes	DDR3- 1066	9	FT1 (BGA)
Family 16h (10H-1fH) (Jaguar)	5/2013	Kabini (SoC)	A Series	28 nm	4 cores with a shared L2 cache	2 MB shared	-	Yes	DDR3L- 1866	15	FT3
Family 16h (30H-3fH) (Puma+)	4/2014	Beema (SoC)	A Series	28 nm		2 MB shared	-	Yes	DDR3L- 1866	15	FT3b
	5/2015	Carrizo-L (SoC)	A Series	28 nm		2 MB shared	-	Yes	DDR3L- 1866	10/ 15	FP4
Family 17h (00H-0fH) (Zen)	10/2017	Raven Ridge (SoC)	Ryzen 7/5/3	14 nm	4-core CCX, private L2 and shared L3 cache(s)	½ MB/ core	1 MB/ core	Yes	DDR4- 2400	15	AM4

APU: Accelerated Processing Unit (CPU +GPU) CCX: Core Complex

²: 2*512 KB for Turion X2, 2*1 MB for Turion X2 Ultra

UMI: Universal Media Interface

2. Family 14h Models 00h-0Fh (Bobcat-based) APU lines

- 2.1 Overview of the Bobcat-based APU lines
- 2.2 The Bobcat core
- 2.3 APU-lines of the Brazos platform
- 2.4 APU lines of the Brazos 2.0 platform
- 2.5 APU lines of the Embedded G-Series platform

2.1 Overview of the Bobcat-based APU lines

2.1 Overview of the Bobcat-based APU lines (1)

2.1 Overview of the Bobcat-based APU lines

- **Bobcat-based APUs** are **AMD's first products** with the **Fusion brand name**, that were introduced at the Consumer Electronics Show (CES) in 1/2011.
They are the **basic parts** of the **Brazos platform** that focuses **on the mobile market**, but includes **desktop models** as well.
- The Brazos platform became **one of AMD's most successful products** that is typically used in **ultra-light notebooks and tablets** [24], [25].
- Bobcat-based APUs **compete with Intel's Atom processors**.
- They mark **AMD's new market strategy** that positively repositions the mobile and desktop market segments in AMD's overall market policy.
- Bobcat based Fusion products include basically **up to two Bobcat cores and a GPU** with similar capabilities than a low-end discrete graphics card.
- 40 nm technology, 75 mm², 450 mtrs.

2.1 Overview of the Bobcat-based APU lines (2)

Remark [26]

Bobcat based Brazos systems was a turning point for AMD.

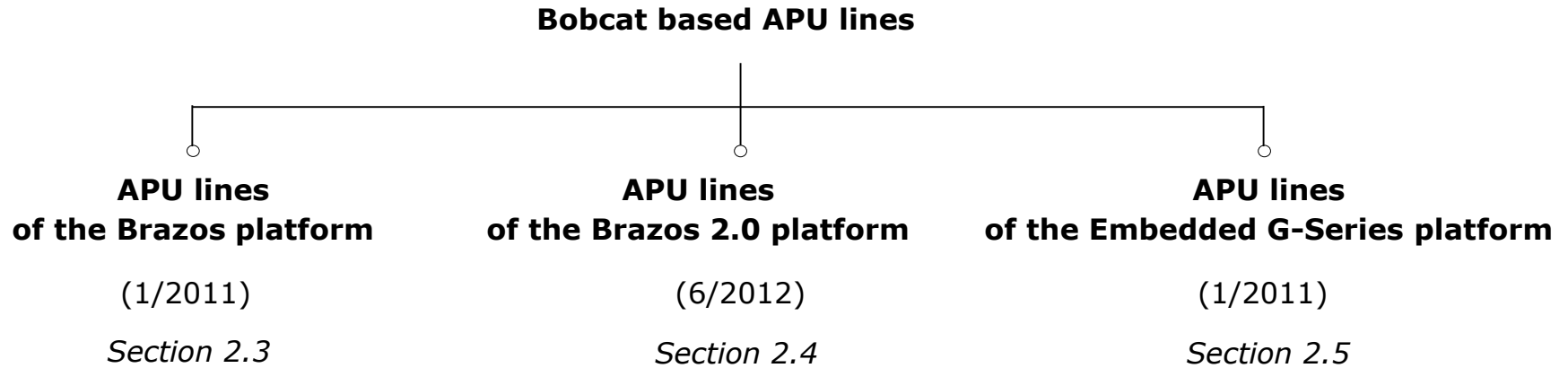
The firm sold until the launch of the Jaguar-based 28 nm mobile products (Temash, Kabini) nearly 50 million Brazos systems.

Jaguar-based systems improve both IPC (about 20 %) and power consumption (also about 20 %) vs. the previous products.

According to industry sources [27] these low power systems seems to be AMD's last hope to avoid bankruptcy and remain alive.

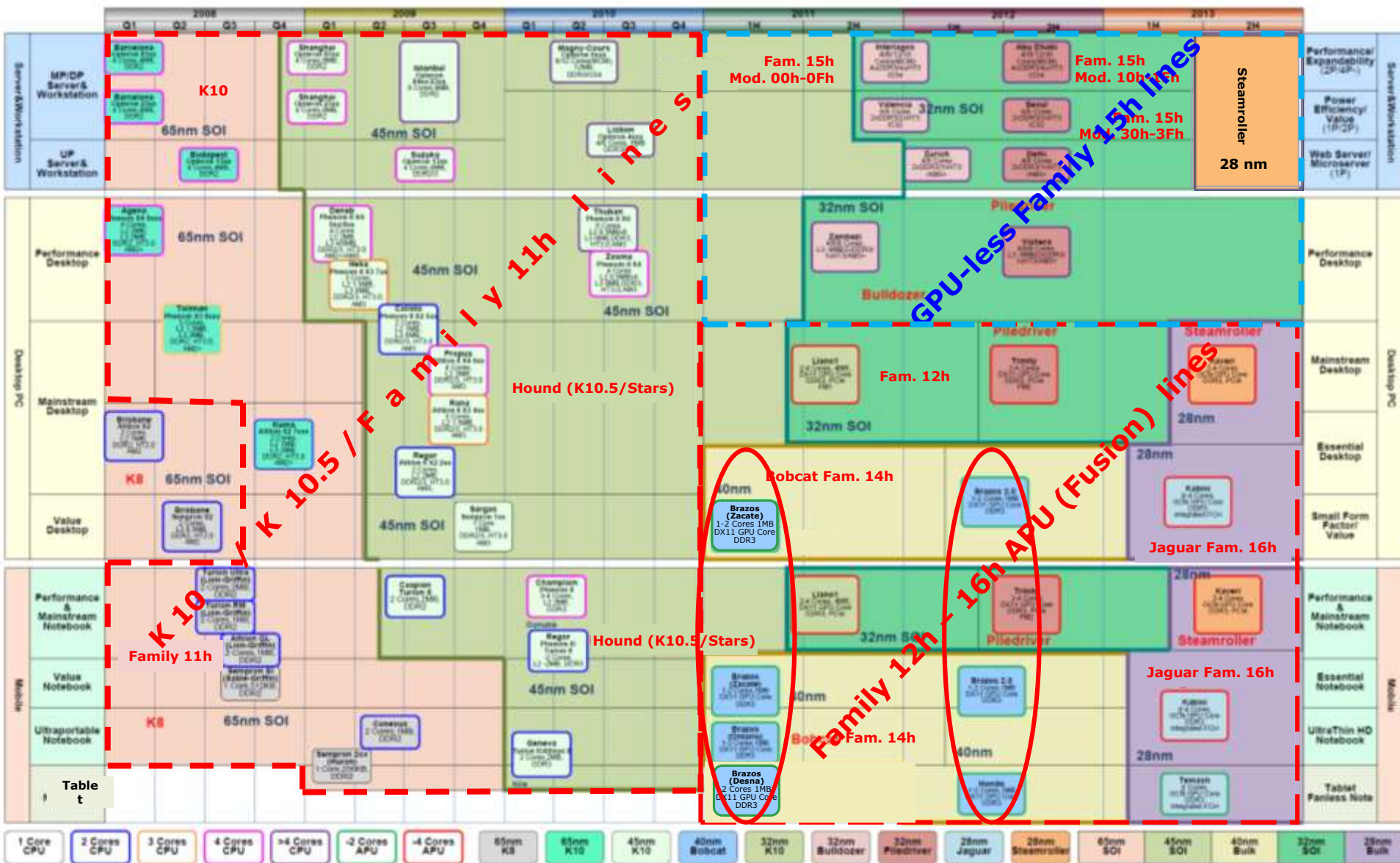
2.1 Overview of the Bobcat-based APU lines (3)

Overview of the Bobcat-based APU lines



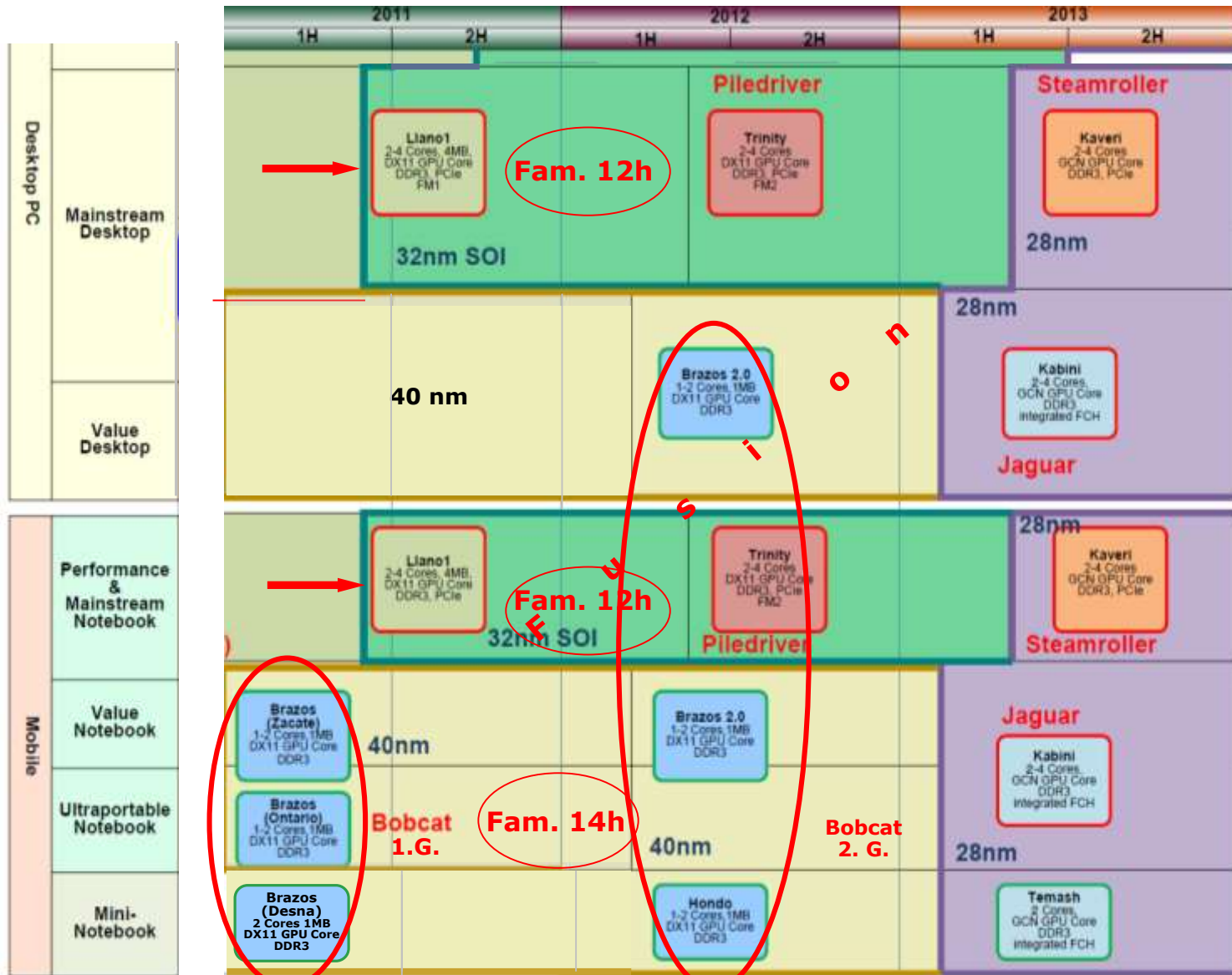
2.1 Overview of the Bobcat-based APU lines (4)

Positioning of the Bobcat-based APU lines-1 (embedded lines not shown) [based on 14]



2.1 Overview of the Bobcat-based APU lines (5)

Positioning of the Bobcat-based APU lines-2 (embedded lines not shown) [14]



2.1 Overview of the Bobcat-based APU lines (6)

Brand names of Bobcat-based processor lines

	Launched in	2011	2012	2013	2014	2015
		Family 14h (00h-0Fh) (Bobcat)	Family 14h (00h-0Fh) (Bobcat)	Family 16h (00h-0Fh) (Jaguar)	Family 16h (30h-3Fh) (Puma+)	Family 16h (30h-3Fh) (Puma+)
Servers	4P servers					
	2P servers					
	1P servers					
	(85-140 W)					
Desktops	High perf. (~95-125 W)					
	Mainstream (~65-100 W)					
	Entry level (~30-60 W)					
Notebooks	High performance/ mainstream/entry (~30-60 W)			Kabini A6		
	Ultra portable (~10-15 W)	Zacate E-Series Ontario C-Series	Zacate E1/E2	Kabini A/E-Series	Beema A/E-Series	Carrizo-L A/L-Series
	Tablet (~5 W)	Desna Z-Series		Temash A Series	Mullins A Series/E1	

2.2 The Bobcat core

- 2.2.1 The microarchitecture of the Bobcat core
- 2.2.2 Main features of the Bobcat core

2.2.1 The microarchitecture of the Bobcat core

2.2.1 The microarchitecture of the Bobcat core (1)

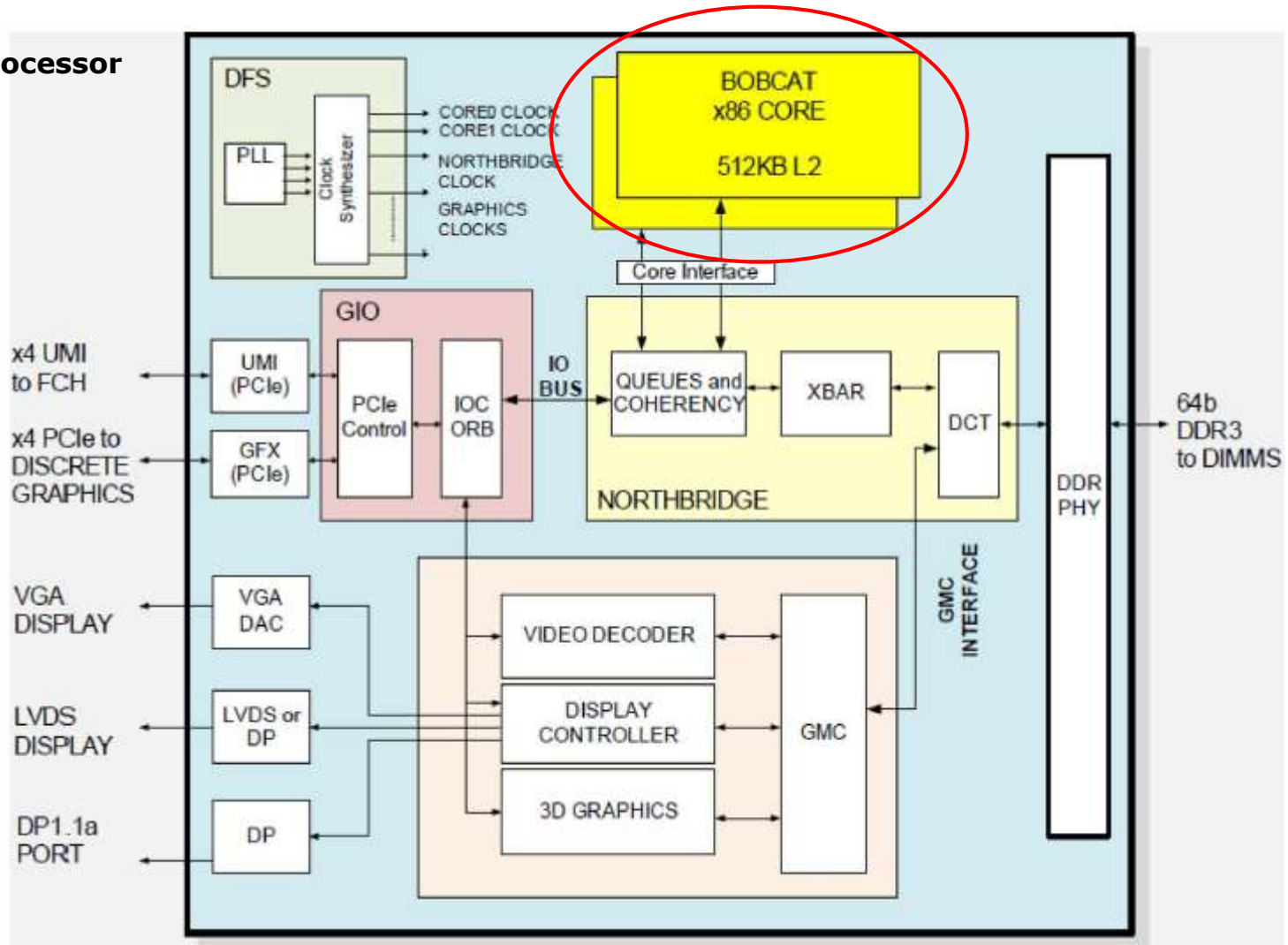
2.2.1 The microarchitecture of the Bobcat core

The **Bobcat core** is the x86 “engine” of Bobcat-based APUs, as indicated in the next example.

2.2.1 The microarchitecture of the Bobcat core (2)

Example: Use of dual Bobcat cores in the Zacate processor [28]

Zacate processor

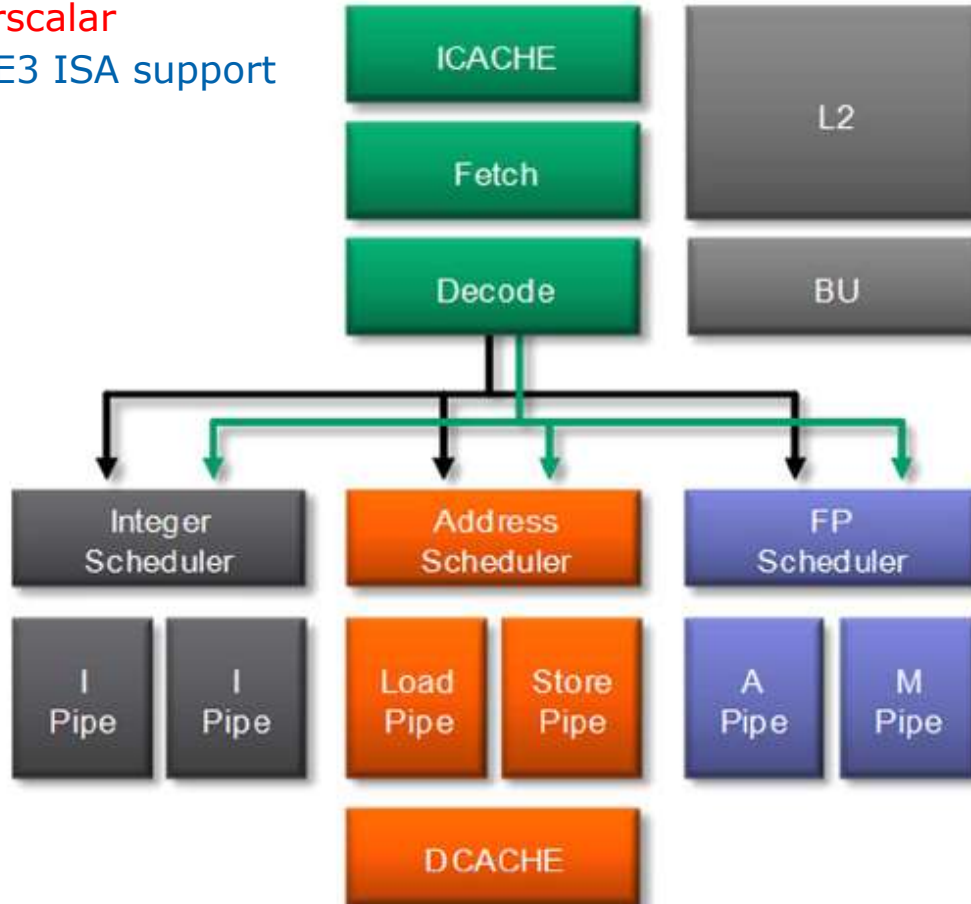


2.2.1 The microarchitecture of the Bobcat core (3)

Rough block diagram of the microarchitecture of the Bobcat core [28]

Dual-issue superscalar

SSE1, 2, 3, SSSE3 ISA support



512 KB/core
ECC protected L2,
clocked at 1/2 clock rate
to reduce power

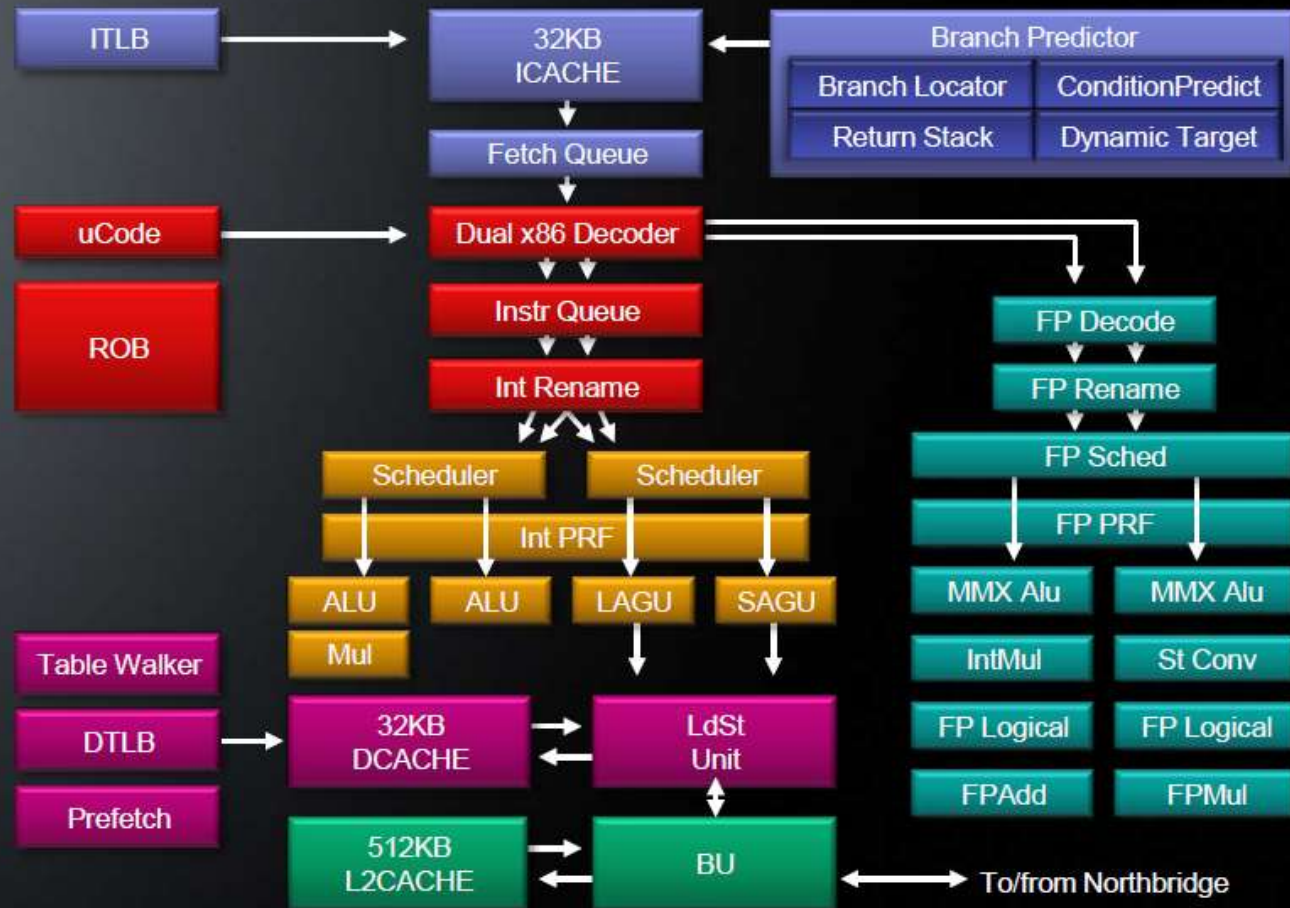
2.2.1 The microarchitecture of the Bobcat core (4)

More detailed block diagram of the microarchitecture of the Bobcat core [8]

Bobcat Micro-Architecture

In-breadth support
of dual issue

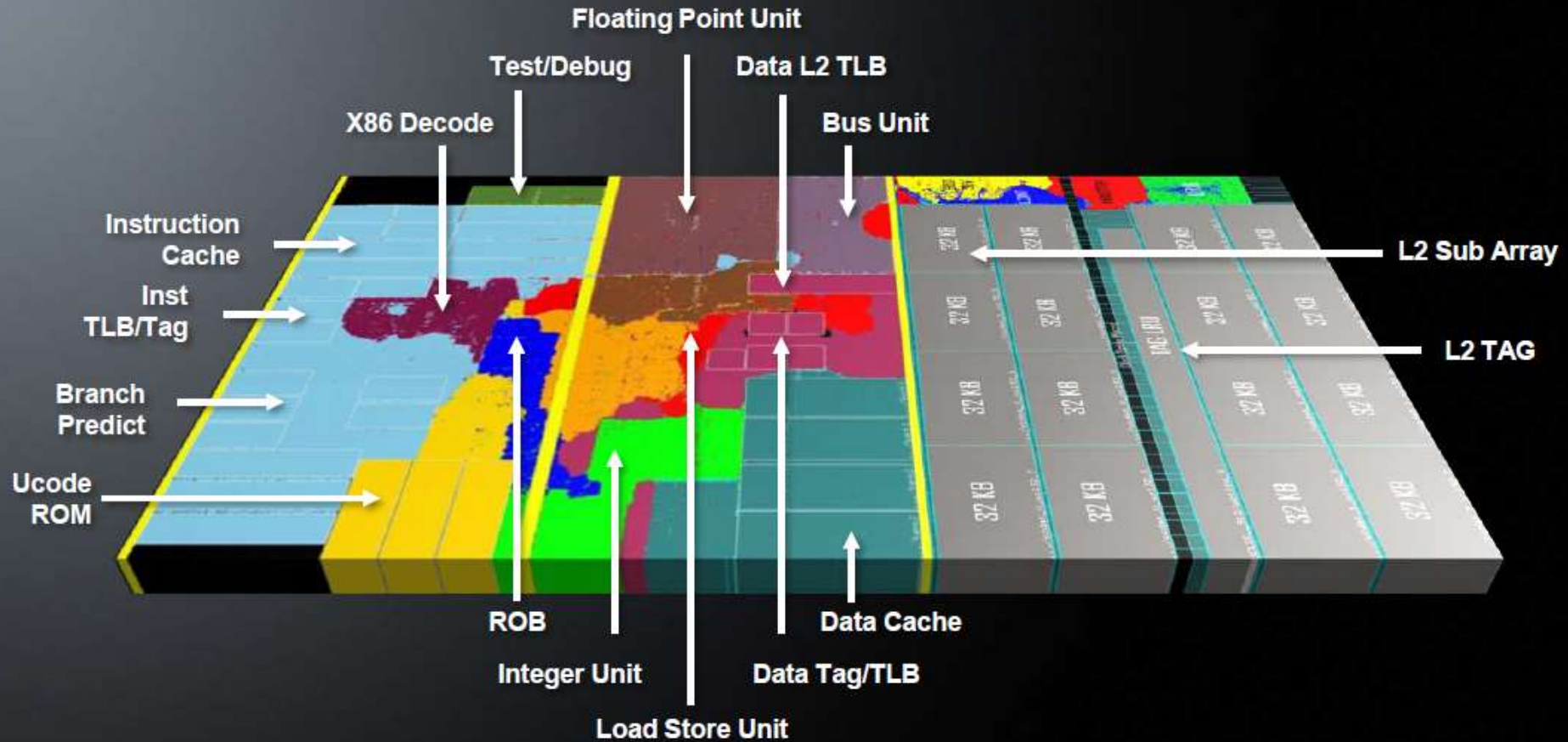
L2 is ECC protected
and clocked at 1/2 clock rate



2.2.1 The microarchitecture of the Bobcat core (5)

Bobcat's floorplan [8]

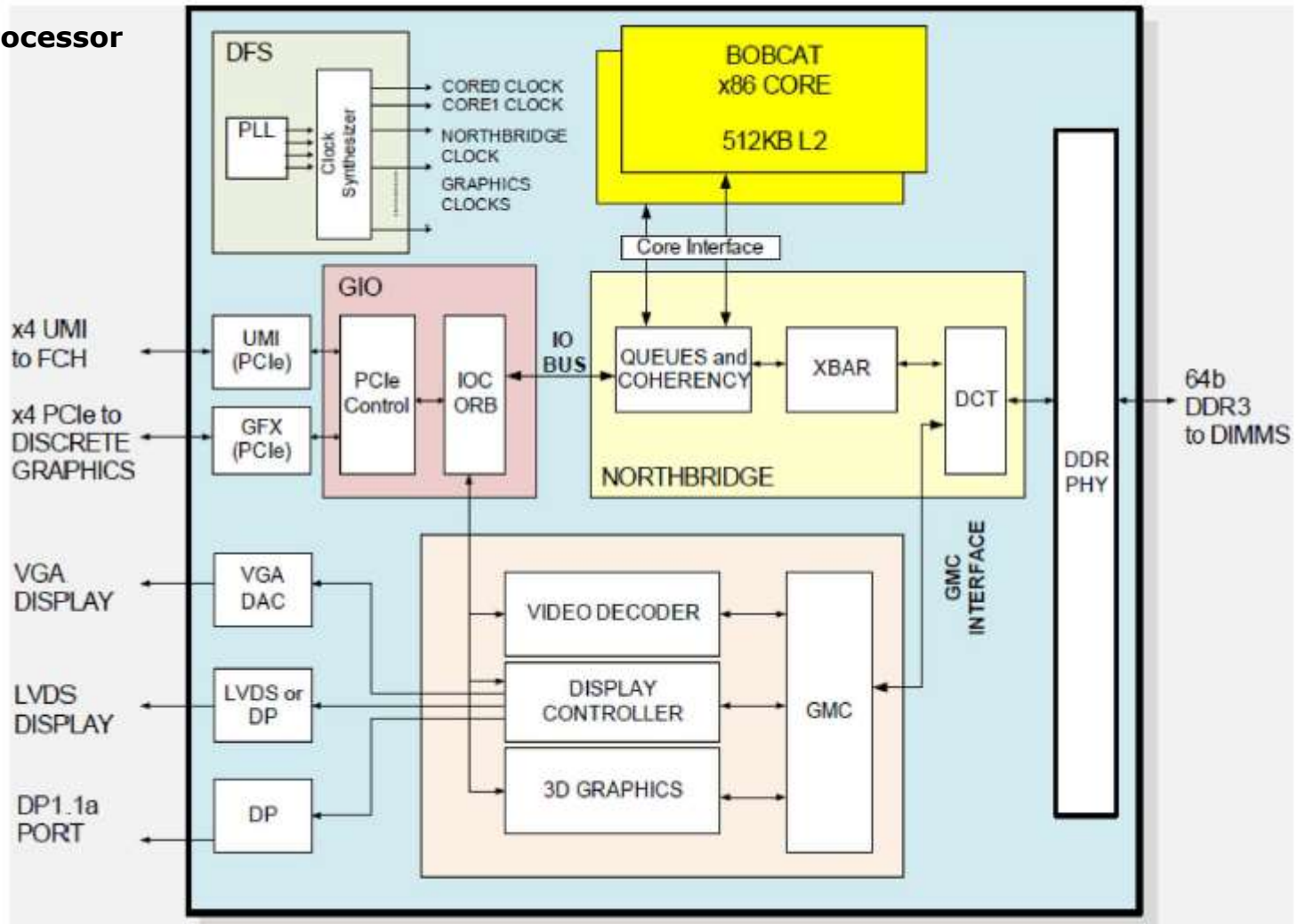
Core Floor Plan



2.2.1 The microarchitecture of the Bobcat core (6)

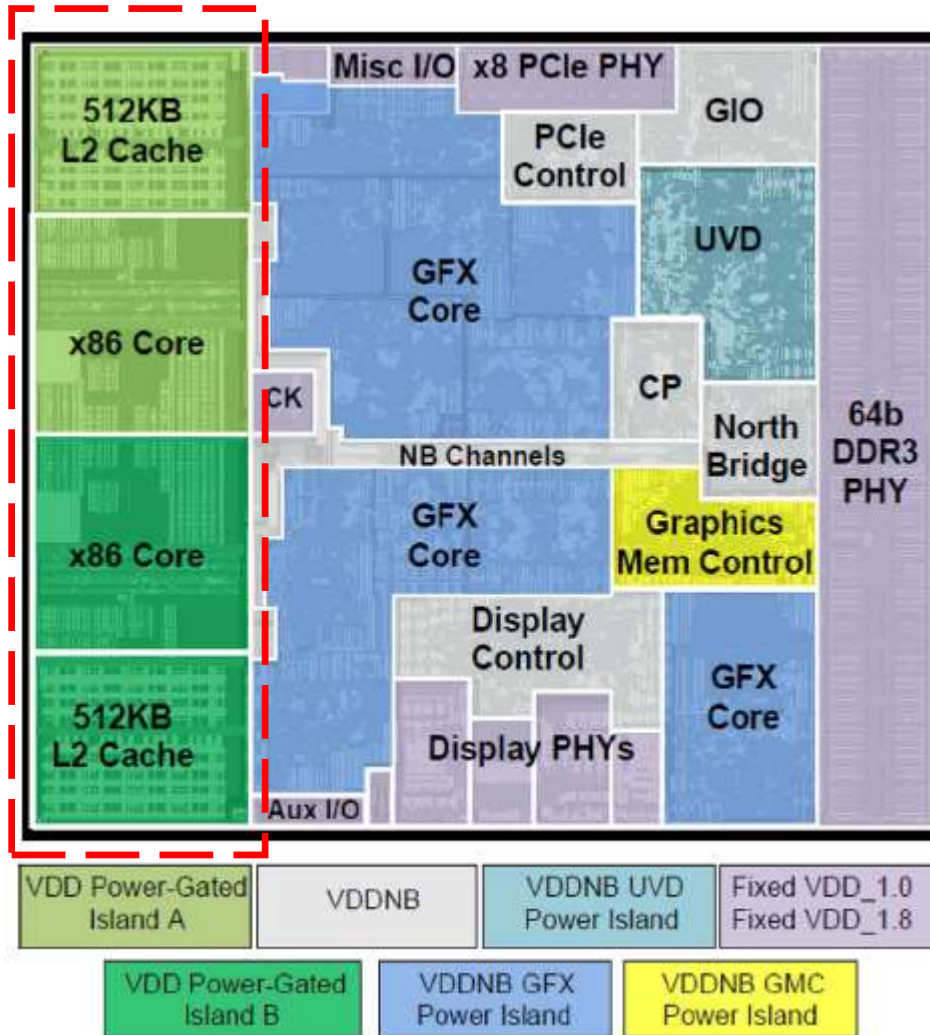
Example: Block diagram of the Zacate APU [28]

Zacate processor



2.2.1 The microarchitecture of the Bobcat core (7)

Example: Floorplan and power domains of the Zacate die that includes 2 Bobcat cores
[28]



2.2.1 The microarchitecture of the Bobcat core (8)

Use of the Bobcat CPU core in AMD's Family 14h-based mobile and embedded lines

- All the Bobcat based Zacate, Ontario and Desna mobile and G-series Fusion APUs have the **same common design** that includes basically two Bobcat CPU cores and a GPU, as detailed in Sections 4.xx and in Sections 4.xx and 4.xx.
- Nevertheless, in different models AMD disables a CPU or the GPU core or both and includes different GPU cores, as indicated next.

2.2.1 The microarchitecture of the Bobcat core (9)

Use of different GPU cores in Bobcat-based Ontario, Zacate and Desna mobile models [29]

"Zacate" (40 nm)

Model	Step.	CPU						GPU				Memory	TDP	Released
		Cores	Freq.	Turbo	L2 Cache	Multi ¹	V _{core}	Model	Config ²	Freq.	Turbo			
E-240	B0	1	1.5 GHz	N/A	512 KB	15×	1.175 - 1.35	HD 6310	80:8:4	500 MHz	N/A	DDR3-1066	18 W	Jan 4, 2011
E-300	B0	2	1.3 GHz		13×	2 × 512 KB	1.25 - 1.35			488 MHz		DDR3-1333		Aug 22, 2011
E-350	B0		1.6 GHz		16×		492 MHz			DDR3-1066		Jan 4, 2011		
E-450	C0	1.65 GHz	16.5×		508 MHz	600 MHz	DDR3-1333			Aug 22, 2011				
E1-1200		1.4 GHz	14×		500 MHz	N/A	DDR3-1066			Q1 2012				
E2-1800		1.7 GHz	17×		523 MHz	680 MHz	DDR3-1333							

"Ontario" (40 nm)

Model	Step.	CPU						GPU				Memory	TDP	Released
		Cores	Freq.	Turbo	L2 Cache	Multi ¹	V _{core}	Model	Config ²	Freq.	Turbo			
C-30	B0	1	1.2 GHz	N/A	512 KB	12×	1.25 - 1.35	HD 6250	80:8:4	276 MHz	N/A	DDR3-1066	9 W	Jan 4, 2011
C-50		2	1.0 GHz		10×	1.05 - 1.35	276 MHz			Aug 22, 2011				
C-60	C0	2	1.0 GHz	1.33 GHz	2 × 512 KB	10-13.3×		HD 6290	80:8:4	276 MHz	400 MHz			Aug 22, 2011

"Desna" (40nm)

Model	Step.	CPU						GPU				Memory	TDP	Released
		Cores	Freq.	Turbo	L2 Cache	Multi ¹	V _{core}	Model	Config ²	Freq.	Turbo			
Z-01	B0	2	1.0 GHz	N/A	2 × 512 KB	10×		HD 6250	80:8:4	276 MHz	N/A	DDR3-1066	5.9 W	June 1, 2011
Z-03													4.5 W	Q1 2012

2.2.2 Main features of the Bobcat core

2.2.2 Main features of the Bobcat core (1)

2.2.2 Main features of the Bobcat CPU core-1 [8]

2.2.2.1 Main features of the Bobcat core affecting the performance or security

Bobcat Core Overview

Advanced Micro-architecture

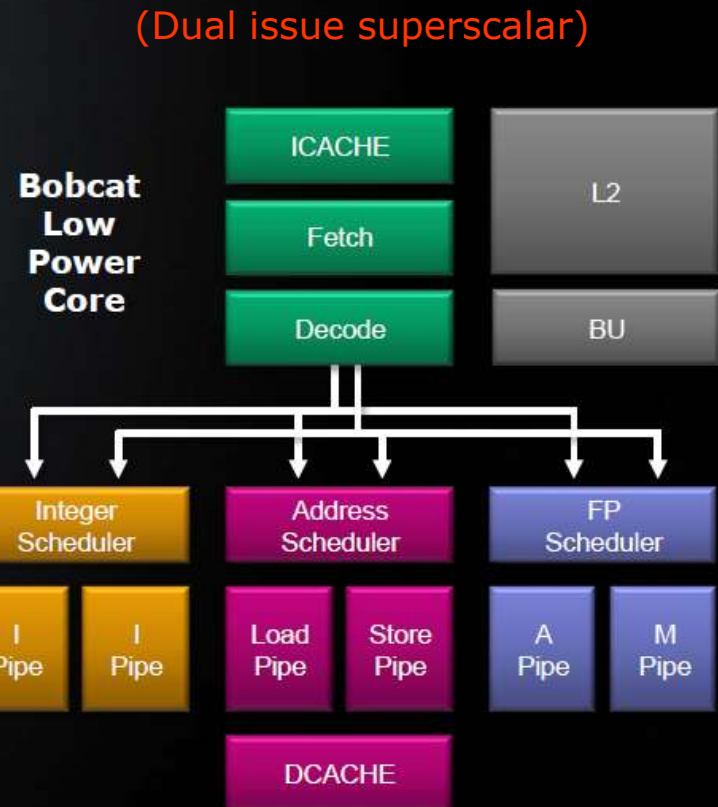
- Dual x86 Decode
- Advanced Branch Predictor
- Full OOO instruction execution
- Full OOO load/store engine
- High Performance Floating Point
- AMD64 64-bit ISA
- SSE1,2,3, SSSE3 ISA
- Secure Virtualization
- 32kb L1s, 512kb L2

Low Power Design

- Power Optimized Execution
- Micro-architecture that minimizes data movement and unnecessary reads
- Clock gating, Power gating
- System Low Power States

Small Core

- Area efficient balance of high performance and low power



2.2.2 Main features of the Bobcat core (2)

The Turbo Core technology in Bobcat cores

- First Bobcat based models were Stepping B0 devices, they were introduced in 1/2011, they did not provide the Turbo Core technology.
- Turbo Core technology appeared along with select dual core Stepping C0 mobile devices that appeared in 8/2011, such as
 - the E450 (Zacate) model that supports Turbo Core for the GPU and
 - the C60 (Ontario) model that supports Turbo Core for both the CPU and the GPU cores [29].

There is no available publication to date that gives details of how Turbo Core is implemented in Bobcat-based processors, nevertheless, it can be assumed that Turbo Core is implemented in these processors in the same way as in the Llano processors, i.e. based on a digital power monitor circuitry, described in [30].

2.2.2 Main features of the Bobcat core (3)

Supporting the Turbo Core mode in different Bobcat-based mobile models [29]

"Zacate" (40 nm)

Model	Step.	CPU						GPU				Memory	TDP	Released
		Cores	Freq.	Turbo	L2 Cache	Multi ¹	V _{core}	Model	Config ²	Freq.	Turbo			
E-240	B0	1	1.5 GHz	N/A	512 KB	15×	1.175 - 1.35	HD 6310	80:8:4	500 MHz	N/A	DDR3-1066	18 W	Jan 4, 2011
E-300	B0	2	1.3 GHz		2 × 512 KB	13×	1.25 - 1.35			488 MHz		DDR3-1333		Aug 22, 2011
E-350	B0		1.6 GHz			16×				492 MHz		DDR3-1066		Jan 4, 2011
E-450	C0	2	1.65 GHz		16.5×	HD 6320	80:8:4	508 MHz	600 MHz	DDR3-1333	Aug 22, 2011			
E1-1200			1.4 GHz		14×	HD 7310	80:8:4	500 MHz	N/A	DDR3-1066	Q1 2012			
E2-1800			1.7 GHz		17×	HD 7340	80:8:4	523 MHz	680 MHz	DDR3-1333				

"Ontario" (40 nm)

Model	Step.	CPU						GPU				Memory	TDP	Released
		Cores	Freq.	Turbo	L2 Cache	Multi ¹	V _{core}	Model	Config ²	Freq.	Turbo			
C-30	B0	1	1.2 GHz	N/A	512 KB	12×	1.25 - 1.35	HD 6250	80:8:4	276 MHz	N/A	DDR3-1066	9 W	Jan 4, 2011
C-50		2	1.0 GHz		2 × 512 KB	10×	1.05 - 1.35			276 MHz				
C-60	C0		1.33 GHz			10-13.3×		HD 6290	80:8:4	276 MHz	400 MHz			Aug 22, 2011

"Desna" (40nm)

Model	Step.	CPU						GPU				Memory	TDP	Released
		Cores	Freq.	Turbo	L2 Cache	Multi ¹	V _{core}	Model	Config ²	Freq.	Turbo			
Z-01	B0	2	1.0 GHz	N/A	2 × 512 KB	10×		HD 6250	80:8:4	276 MHz	N/A	DDR3-1066	5.9 W	June 1, 2011
Z-03													4.5 W	Q1 2012

2.2.2 Main features of the Bobcat core (4)

2.2.2.2 Main features of the Bobcat core affecting the power consumption [8]

Bobcat Core Overview

Advanced Micro-architecture

- Dual x86 Decode
- Advanced Branch Predictor
- Full OOO instruction execution
- Full OOO load/store engine
- High Performance Floating Point
- AMD64 64-bit ISA
- SSE1,2,3, SSSE3 ISA
- Secure Virtualization
- 32kb L1s, 512kb L2

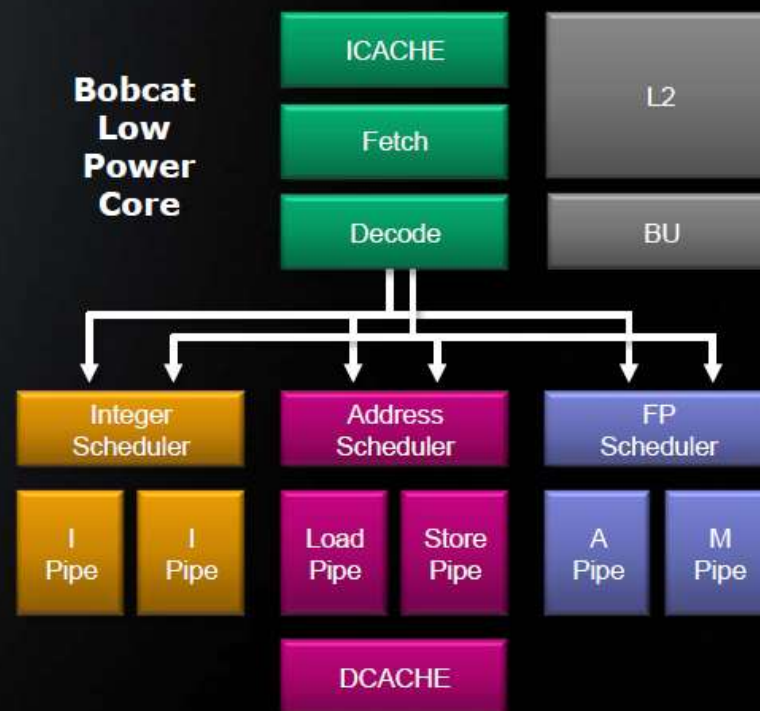
Low Power Design

- Power Optimized Execution
- Micro-architecture that minimizes data movement and unnecessary reads
- Clock gating, Power gating
- System Low Power States

Small Core

- Area efficient balance of high performance and low power

(Dual issue superscalar)



1) Power optimized microarchitecture [31]

- **Introducing physical register files instead of future files for register renaming**
 - While using physical register files for register renaming the physical register files keep both the architectural state and the result values of the execution that are waiting for writing back into the architectural registers in sequential order.
 - Such an implementation replaces data movements with pointer updates that results in power saving.
- **Pointer based implementation of queues**

This minimizes data movements versus traditional implementations of queues where data will be shifted for adding or removing data.

Remark

For an overview of register renaming see e.g. [62].

2.2.2 Main features of the Bobcat core (6)

2) Using effective power saving techniques related to clocking and powering the processor

Bobcat cores utilize

- Clock gating
- Power gating as well as
- Core CC6 and package PC6 states,

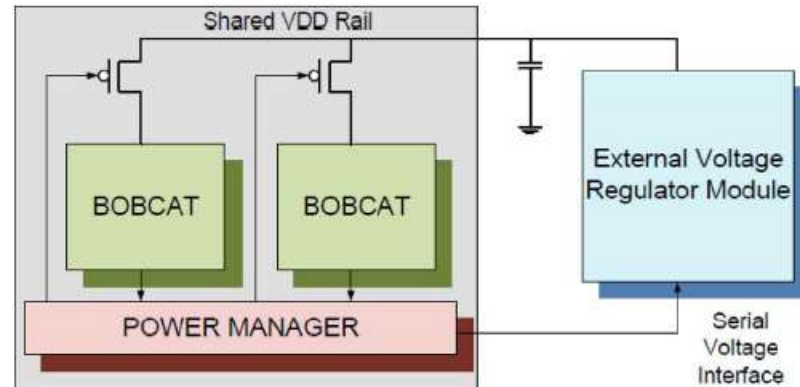
i.e. low power techniques used also in Llano or Bulldozer cores, and described in the related Section discussing the Llano lines.

Remarks

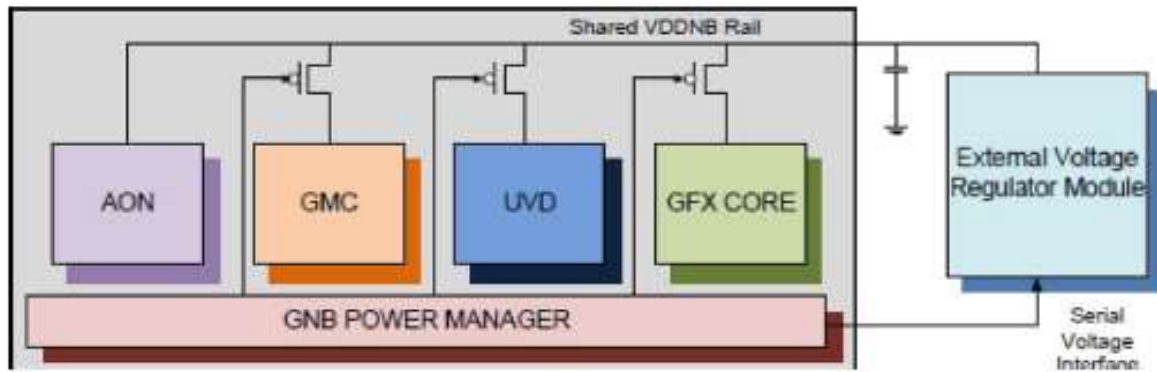
- 1) Data size-based clock gating is widely used in Bobcat cores for less than 64-bit operations, for this reason e.g. the upper and lower halves of all result buses and forwarding logic are clocked independently to allow clock gating of not needed circuitry [31].
- 2) Power gating is implemented differently in the Bobcat and Llano cores and Bulldozer modules. Whereas in the Llano cores and Bulldozer modules AMD power isolates VSS (ground), in the Bobcat cores VDD will be isolated as shown next [28].

2.2.2 Main features of the Bobcat core (7)

Power gating the Bobcat cores [28]



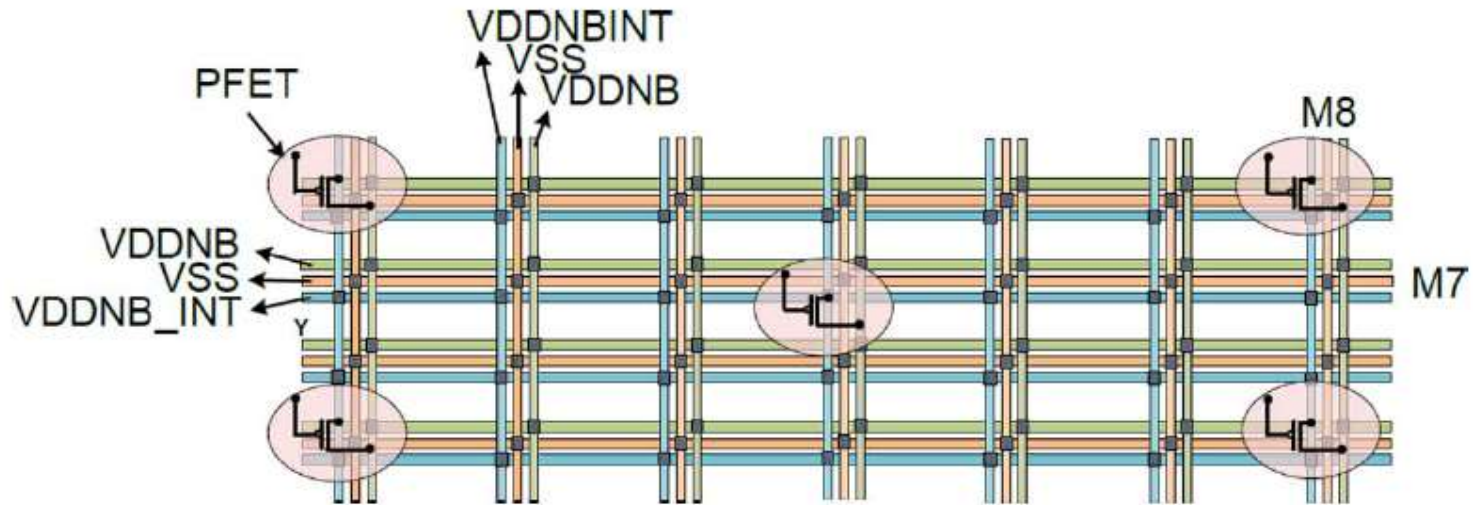
Power gating the NBB units [28]



- GFX:** Graphics Core
- GMC:** Graphics Memory Control
(if memory is in self-refresh)
- UVD:** Unified Video Decoder

2.2.2 Main features of the Bobcat core (8)

Power gating of VDDNB in Zacate's VDDNB power grid implementation [28]



VDDNB: Supply voltage of the North Bridge

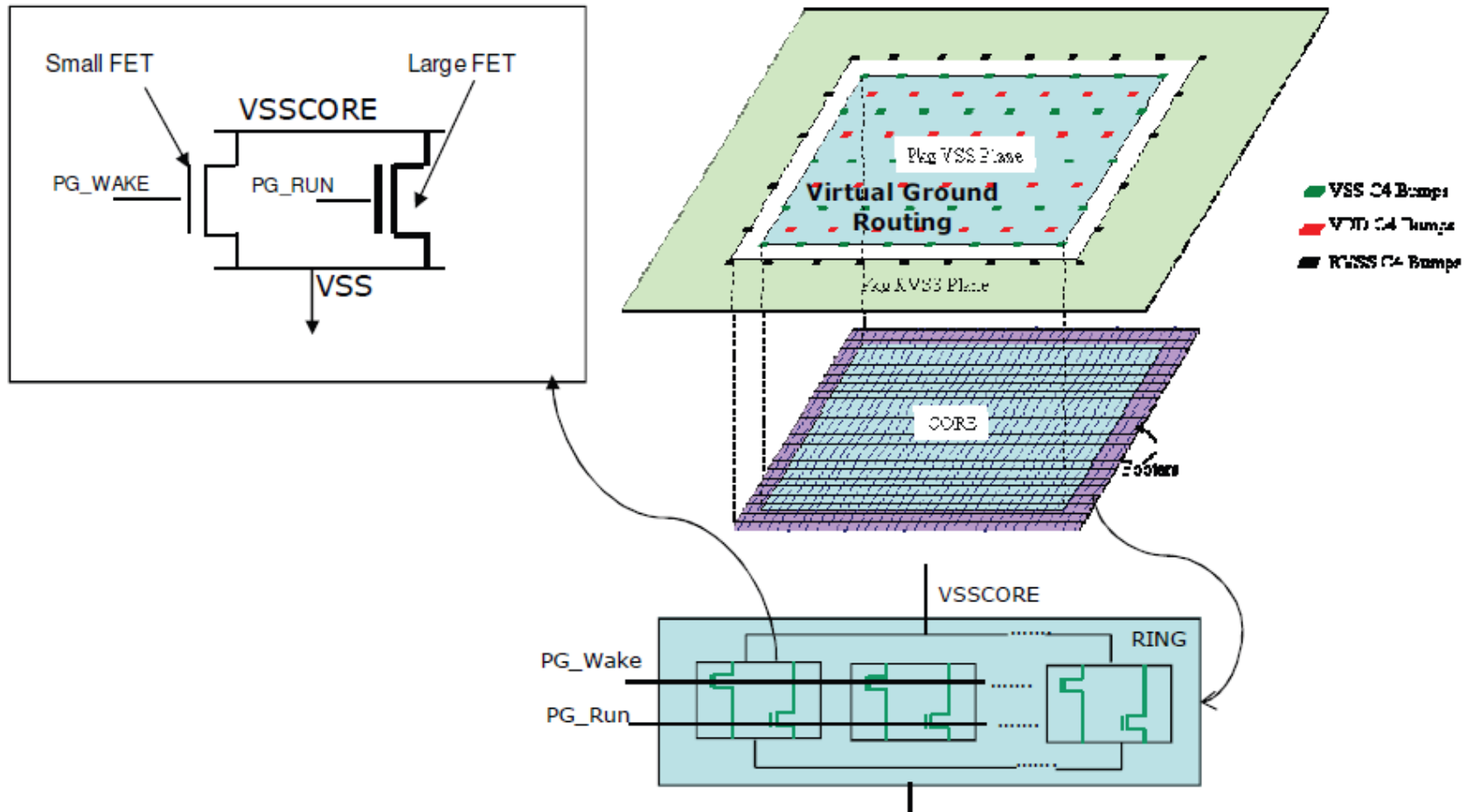
VDDNB_INT: Power gated supply voltage of the North Bridge

VSS: Ground

M7, M8: Metal layers

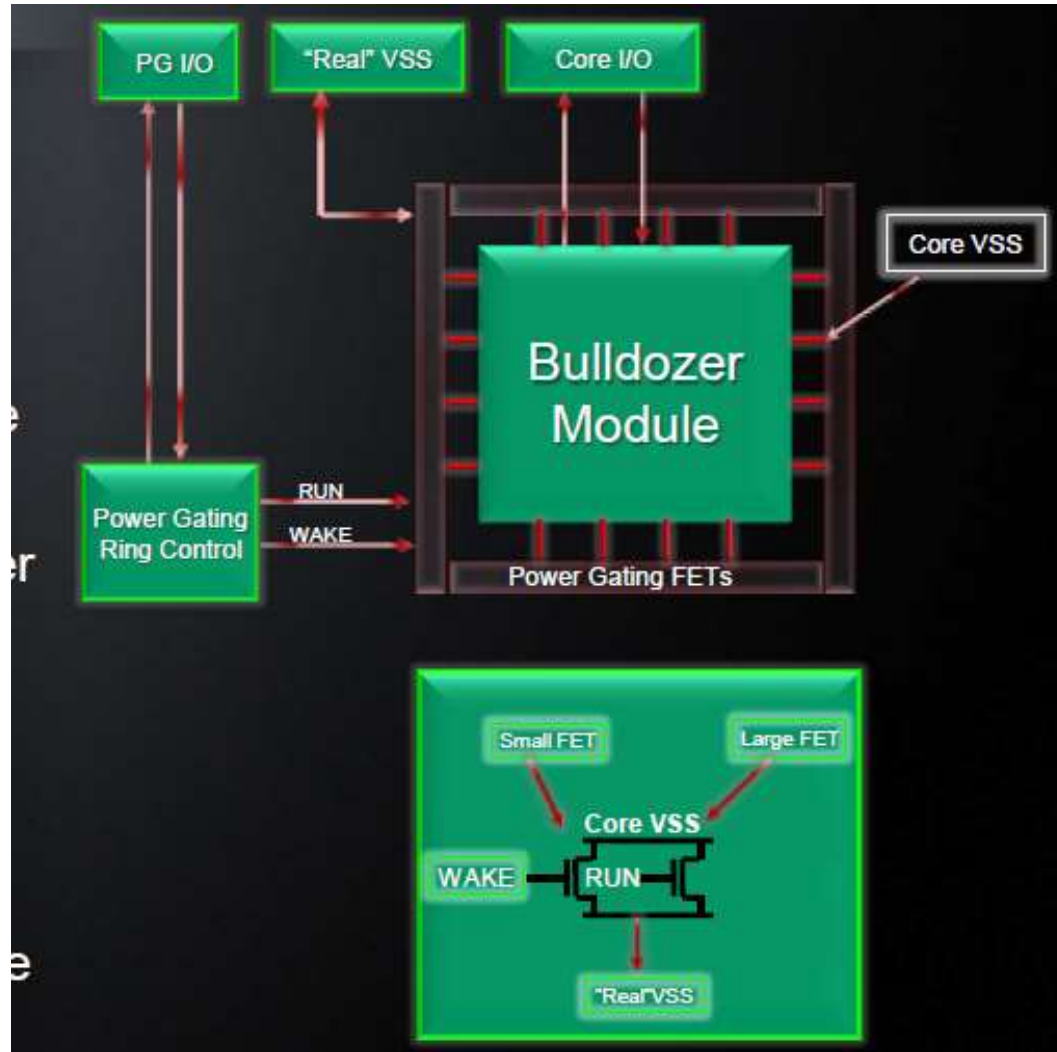
2.2.2 Main features of the Bobcat core (9)

Power gating of VSS in AMD's Llano cores [32]



2.2.2 Main features of the Bobcat core (10)

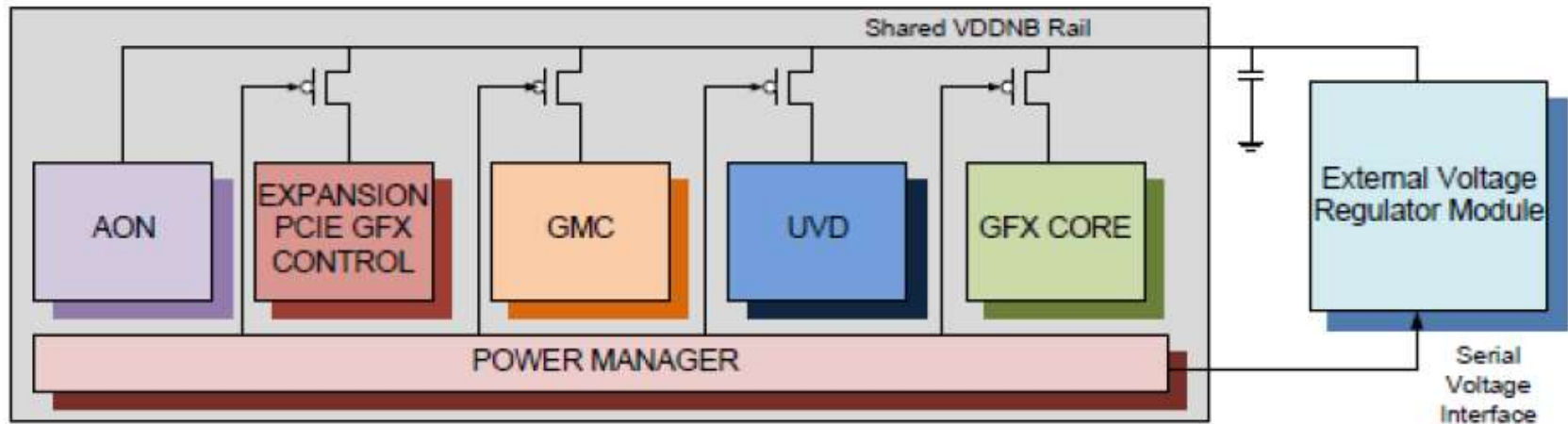
Power gating of VSS in AMD's Bulldozer modules [33]



2.2.2 Main features of the Bobcat core (11)

Remark

Nevertheless, in Llano's NB AMD seems to power-gate VDDNB rather than VSS [34]



- With
- GFX: Graphics Core
 - GMC: Graphics Memory Control
(when memory is in self-refresh)
 - UVD: Unified Video Decoder
 - PCIE GFX CONTROL: the x16 PCIe Graphics Expansion Controller
 - AON: Always on (not power gated circuitry)

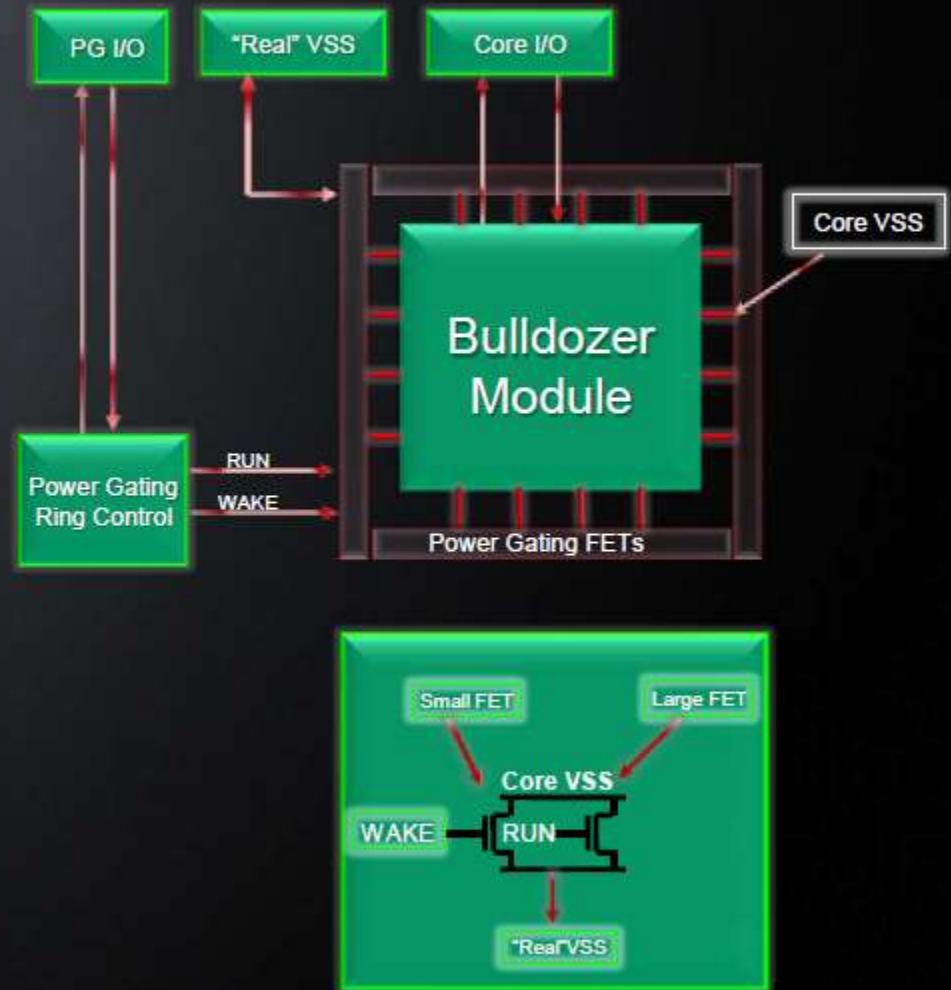
The **GFX** and **GMC** units are **dynamically** (hardware controlled) **power gated** whereas power gating of the **other units** is **static**, i.e. done under software (driver) control.

2.2.2 Main features of the Bobcat core (12)

Implementation of the Core C6 state with power gating in a Bulldozer module [33]

POWER MANAGEMENT | Core C6 State (CC6)

- Core C6: if a core isn't active, remove power
- Implemented in this physical design by a power gating ring that isolates the Core VSS for each Bulldozer module from the "Real" VSS
- CC6 entry: when both Bulldozer cores in the module are idle, flush caches and dump register state to CC6 save space, then gate Core VSS
- CC6 exit: ungate Core VSS, reload CC6 saved state, resume execution (ex: service interrupts, etc.)



2.2.2 Main features of the Bobcat core (13)

The Core C6 state (CC6 state)/Package C6 state (PC6 state) (simplified) [35]

Entering the CC6 state

1. OS requests entering into the CC6 state by issuing a specific I/O read or HLT instruction.
2. The processor enters the CC6 state if associated monitors allow this.

The process of entering the CC6 state

1. L1 and L2 caches are flushed to DRAM by hardware.
2. Internal core state is saved to DRAM by hardware.
3. The core clock ramps down to a low value..

Entering the power gating state

If a core entered the CC6 state and a transition to power gating is allowed the core becomes power gated by Vss removed.

Exiting the Core C6 state (CC6 state)

There is a set of events, such as interrupts, which cause a core to exit the CC6 state.

Entering the Package C6 state (PC6 state)

If all cores have entered the CC6 state and a transition to the PC6 state is enabled (by monitors), the processor enters the PC6 state.

Exciting from the Package C6 state (PC6 state)

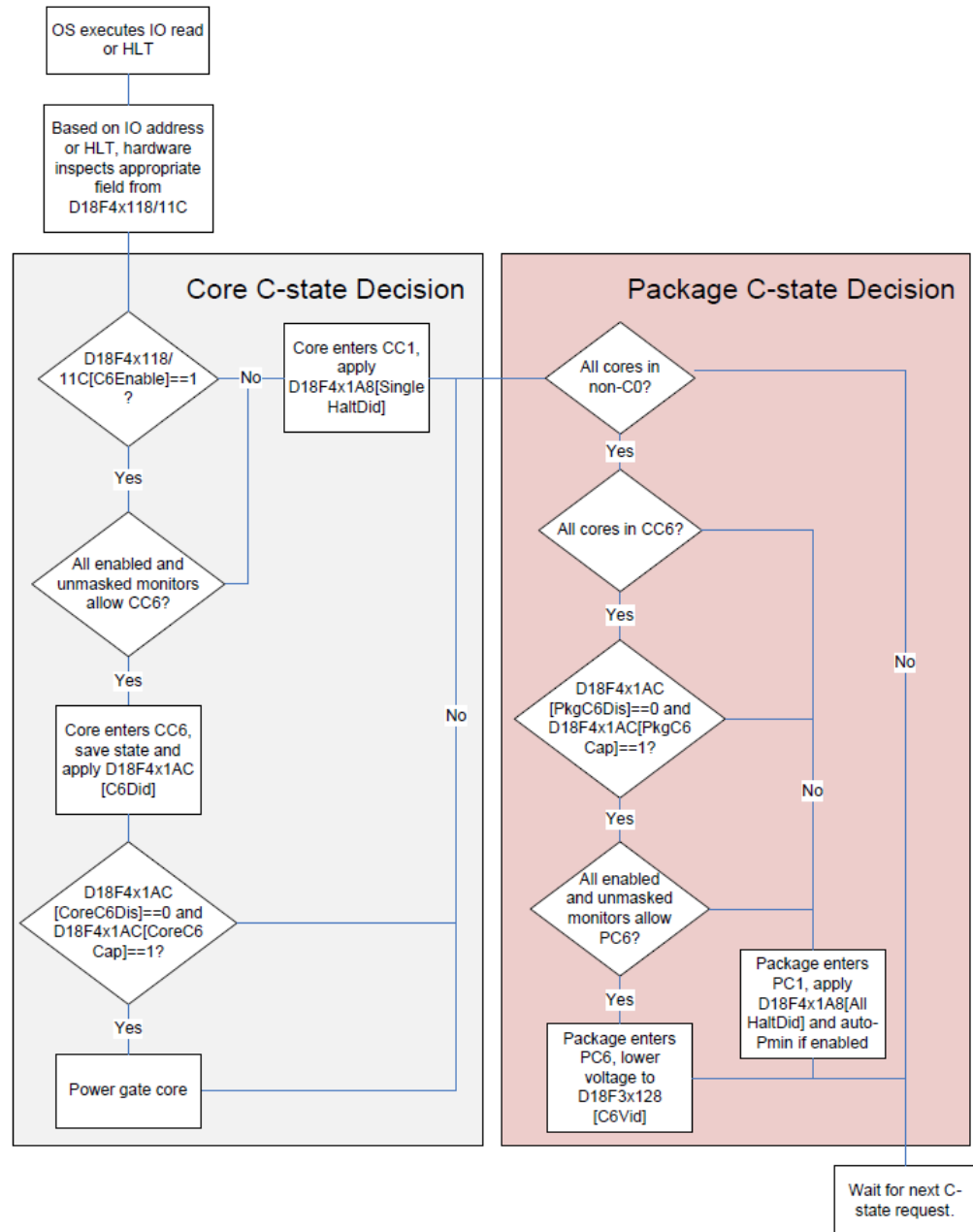
If one of the cores leaves the CC6 state the processor excites the PC6 state.

2.2.2 Main features of the Bobcat core (14)

Remark [35]

Flow diagram of entering

- the Core C6 (CC6) and
- the Package C6 (PC6) states



2.3 APU-lines of the Brazos platform

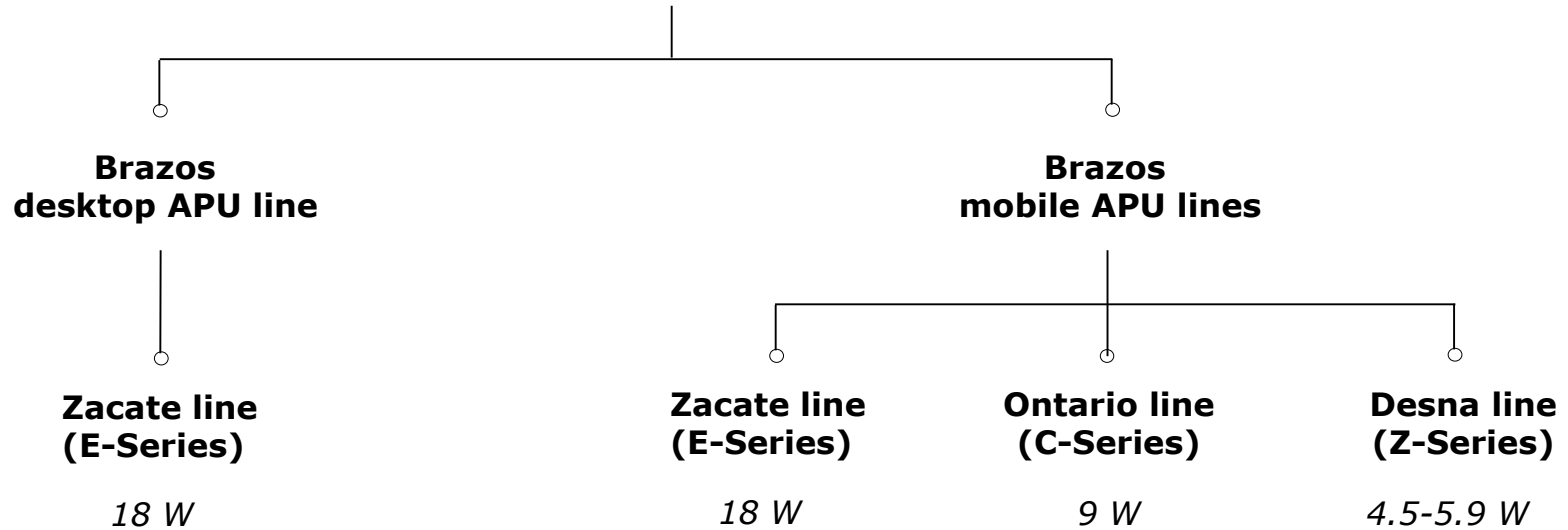
- 2.3.1 Overview of the Bobcat based APU lines of the Brazos platform
- 2.3.2 Mobile APU lines of the Brazos platform

2.3.1 Overview of the APU lines of the Brazos platform

2.3.1 Overview of the Bobcat based APU lines of the Brazos platform (1)

2.3.1 Overview of the APU lines of the Brazos platform

APU lines of the Brazos platform



No extra designs,
as desktops AMD markets
high-end models of the
Zacate mobile APU line
(No extra discussion is needed).

Direct X 11 capable graphics.

No Turbo Core on first introduced, Stepping B0 devices in 1/2011,

CPU and GPU Turbo Core introduced later on select dual core Stepping C0 Series E and C devices in 8/2011.

Socket: FT1 BGA.

2.3.1 Overview of the Bobcat based APU lines of the Brazos platform (2)

Target markets of Bobcat based APU lines of the Brazos platform [36]

Llano-based APU lines



- Mainstream notebooks
- All-in-ones
- Desktops
- Embedded

Bobcat-based APU lines of the Brazos platform



- Ultra-mobile and thin-and-light notebooks
- Small form factor desktops

Zacate line (18 W)

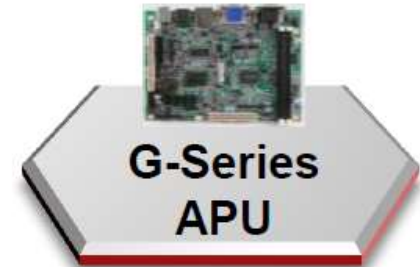


- Ultra-mobile notebooks
- Tablets

Ontario line (9 W)

Desna line (4.5/5.9 W)

Bobcat-based embedded APU lines



- Embedded

Zacate-based (18 W)

Ontario-based (9 W)

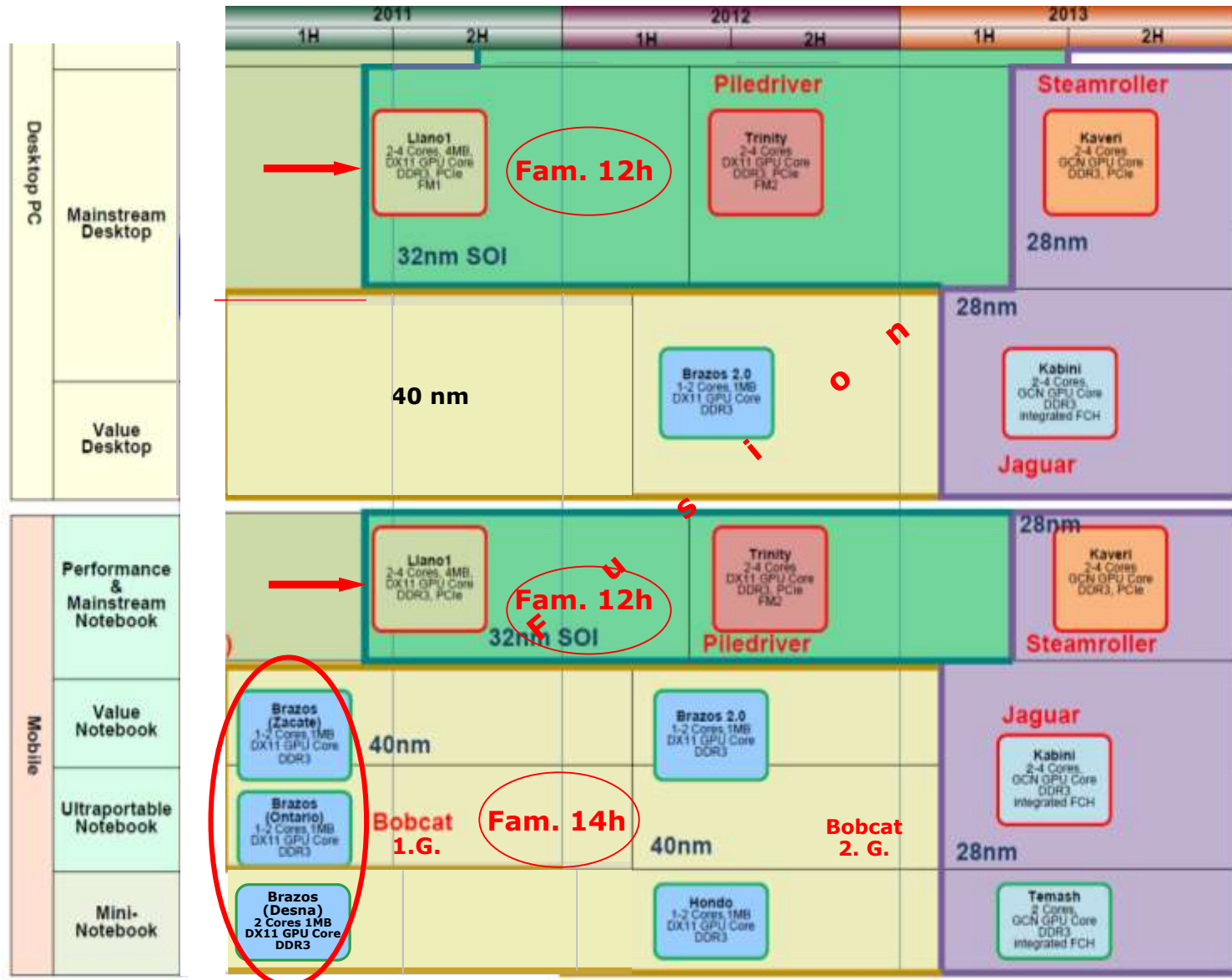
Desna-based (5.5/
6.4 W)

All days battery life

x86 cores and a Direct X 11 capable GPU on the same silicon

2.3.1 Overview of the Bobcat based APU lines of the Brazos platform (3)

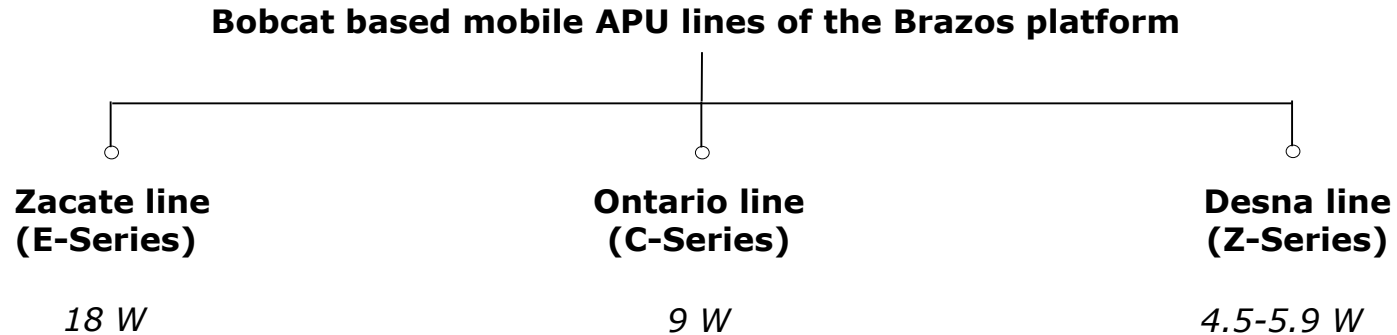
Positioning of the Bobcat-based mobile APU lines of the Brazos platform [14]



2.3.2 Mobile APU lines of the Brazos platform

2.3.2 Mobile APU lines of the Brazos platform (1)

2.3.2 Bobcat based mobile APU lines of the Brazos platform



Direct X 11 capable graphics.

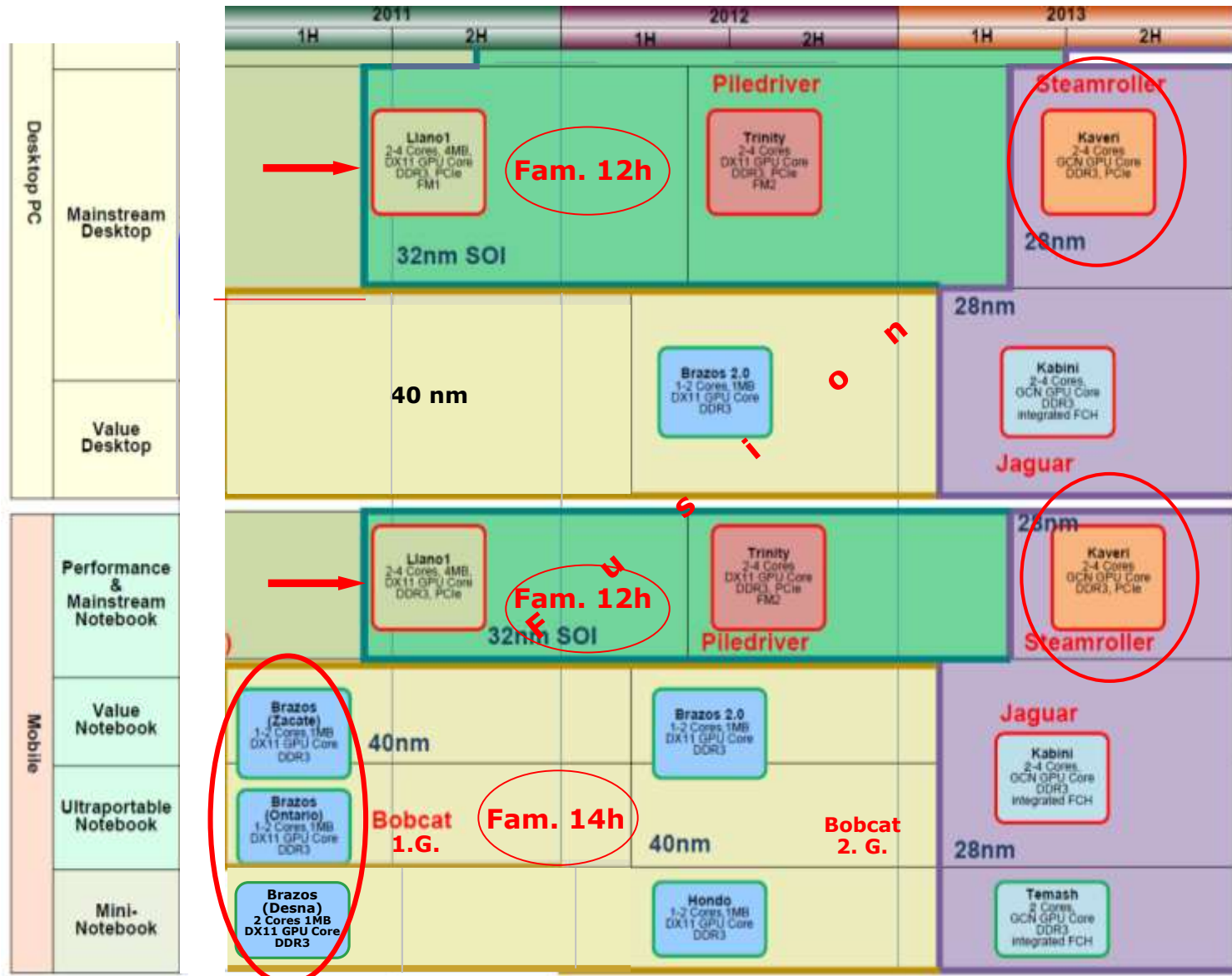
No Turbo Core on first, Stepping B0 devices in 1/2011,

CPU and GPU Turbo Core introduced later on select dual core Stepping C0 Series E and C devices in 8/2011.

Socket: FT1 BGA.

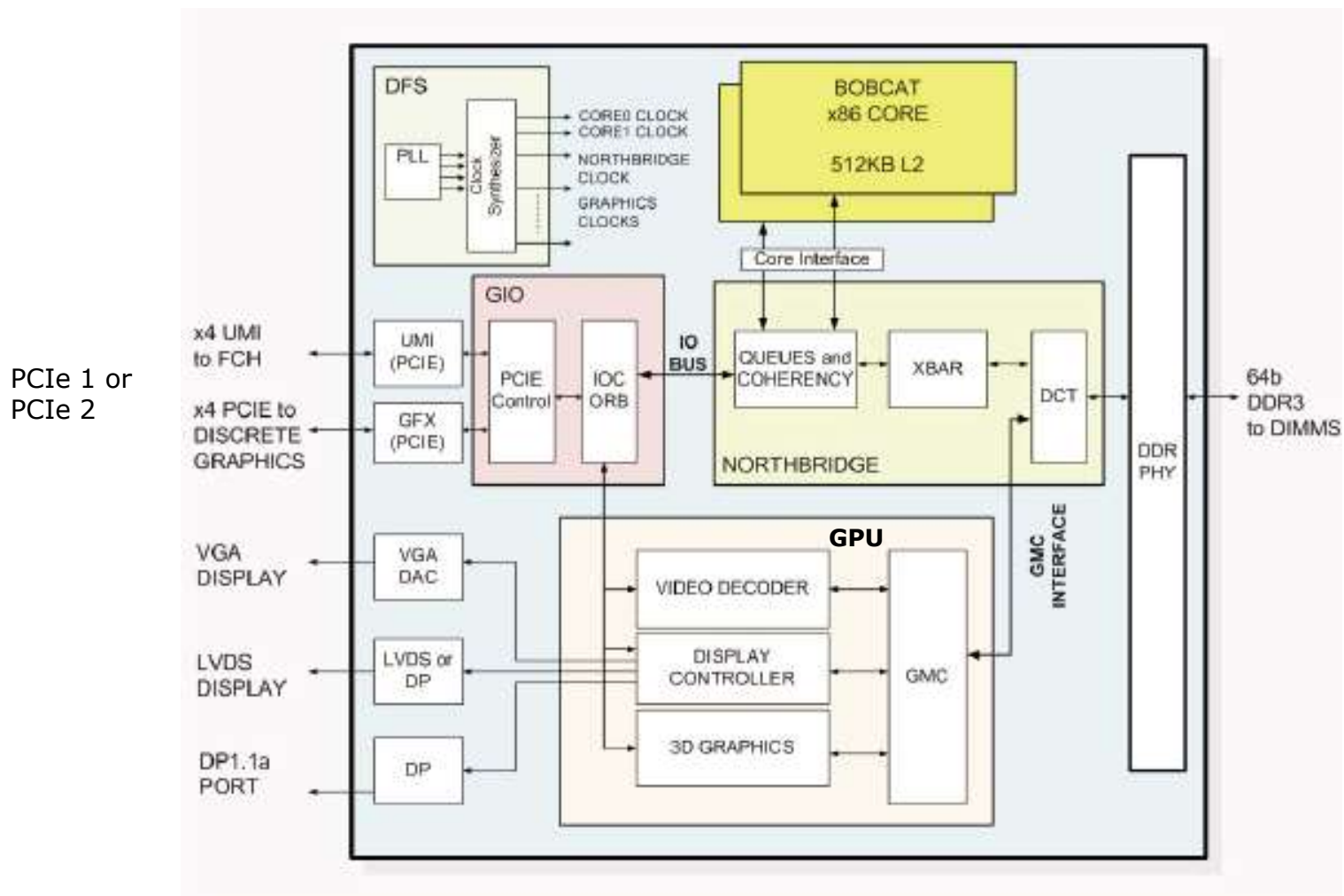
2.3.2 Mobile APU lines of the Brazos platform (2)

Positioning of the Mobile APU lines of the Brazos platform [based on 14]



2.3.2 Mobile APU lines of the Brazos platform (3)

The common block diagram of the Zacate, Ontario and Desna Fusion APUs [28]



PCIe 1 or
PCIe 2

GMC: Graphics Memory Controller
DP: Display port
DFS: Digital Frequency Synthesizer
UMI: Unified Media interface

FCH: Fusion Controller Hub
LVDS: Low Voltage Differential Signaling
VGA: Video Graphics Array

2.3.2 Mobile APU lines of the Brazos platform (4)

Remarks

- 1) AMD's Fusion architecture implements an **efficient form of the UMA architecture (Unified Memory Architecture)** in which a part of the system memory is used as the **graphics frame buffer** [28].
- 2) The Zacate, Ontario and Desna processors **are part of the Brazos mobile platform**, as already stated.

2.3.2 Mobile APU lines of the Brazos platform (5)

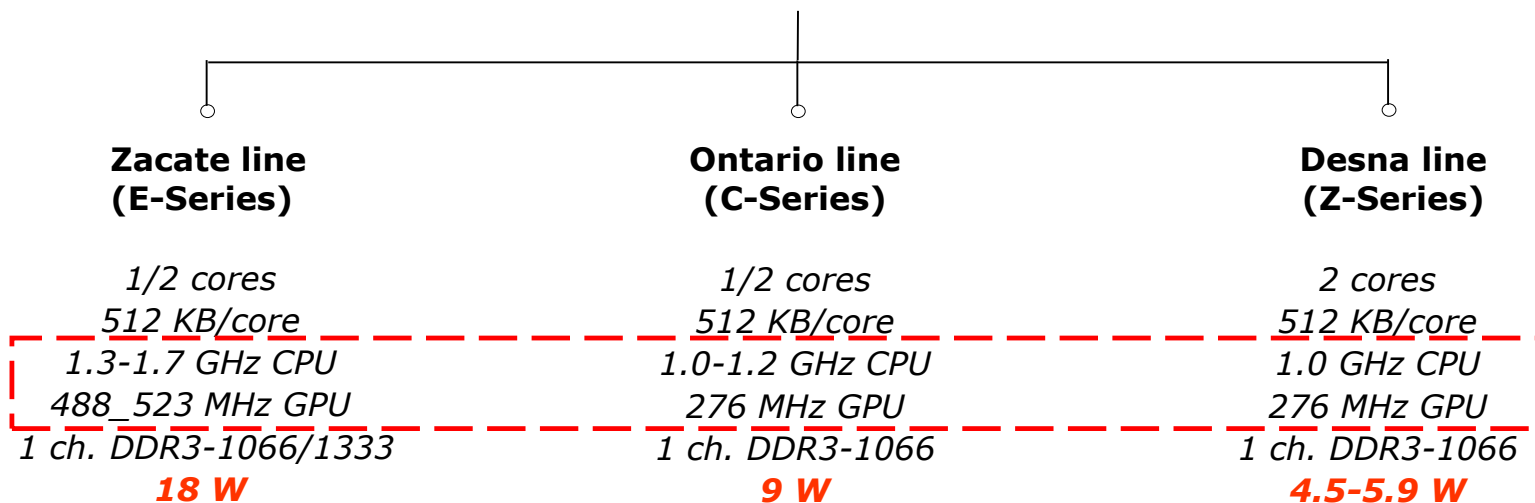
Microarchitecture of Mobile APUs of the Brazos platform

- Zacate, Ontario and Desna APUs have **basically the same microarchitecture**.
- The **main difference** between them is that they have **decreasing clock rates** (both CPU and GPU clock rates) and **accordingly decreasing power consumption** (18 W/9 W/~5 W), as shown below.

2.3.2 Mobile APU lines of the Brazos platform (6)

Key features of Mobile APU lines of the Brazos platform

Bobcat based mobile APU lines of the Brazos platform



Direct X 11 capable graphics.

No Turbo Core on first, Stepping B0 devices in 1/2011,

CPU and GPU Turbo Core introduced later on select dual core Stepping C0 Series E and C devices in 8/2011.

Socket: FT1 BGA.

2.3.2 Mobile APU lines of the Brazos platform (7)

Main features of mobile APU lines of the Brazos platform

		Core count	L2	GPU	fc (GPU) (MHz)	1 Ch. DDR3 (up to)	
M o b i l e s	Mainstream A-Series (Llano-based)						
	Essential	2C	2x512 KB	HD 6320	488-508	DDR3-1333	1/11 ↓ Zacate 40 nm, ~75 mm ² , ~450 mtrs 1.3-1.65 GHz 18 W, FT1 BGA E-4xx ----- E-2xx/E-3xx
	E-series (Zacate) (Bobcat-based)						
	Value	1C	512 KB	HD 6310	488-500	DDR3-1333	
	C-series Low power (Ontario) (Bobcat-based)	2C	2x512 KB	HD 6250 (C-30/C-50) HD 6290 (C-60)	276	DDR3-1066	1/11 ↓ Ontario 40 nm, ~75 mm ² , ~450 mtrs 1.0-1.2 GHz 9 W, FT1 BGA C-50/C60 ----- C-30
		1C	512 KB				
Ultra Low power Z-series (Desna) (Bobcat-based)	2C	2x512 KB	HD 6250	276	DDR3-1066	6/11 ↓ Desna 40 nm, ~75 mm ² , ~450 mtrs 1.0 GHz 5.9 W, FT1 BGA Z-0x	

Differences in the microarchitectures of the Bobcat-based Zacate, Ontario and Desna APUs-1

- a) A few Zacate and Ontario models (E-series and C-series) have only a single Bobcat core, while the other core is disabled on the die, as indicated in the next Figure.

2.3.2 Mobile APU lines of the Brazos platform (9)

Differences in the microarchitectures of the Bobcat-based Zacate, Ontario and Desna APUs-2

		Core count	L2	GPU	fc (GPU) (MHz)	1 Ch. DDR3 (up to)		
M o b i l e s	Mainstream	A-Series (Llano-based)						
	Essential	E-series (Zacate)	2C	2x512 KB	HD 6320	488-508	DDR3-1333	1/11 ↓ Zacate 40 nm, ~75 mm ² , ~450 mtrs 1.3-1.65 GHz 18 W, FT1 BGA E-4xx
	Value		1C	512 KB	HD 6310	488-500	DDR3-1333	E-2xx/E-3xx
	Low power	C-series (Ontario)	2C	2x512 KB	HD 6250 (C-30/C-50) HD 6290 (C-60)	276	DDR3-1066	1/11 ↓ Ontario 40 nm, ~75 mm ² , ~450 mtrs 1.0-1.2 GHz 9 W, FT1 BGA C-50/C60
			1C	512 KB				C-30
	Ultra Low power	Z-series (Desna)	2C	2x512 KB	HD 6250	276	DDR3-1066	6/11 ↓ Desna 40 nm, ~75 mm ² , ~450 mtrs 1.0 GHz 5.9 W, FT1 BGA Z-0x

Differences in the microarchitectures of the Bobcat-based Zacate, Ontario and Desna APUs-3

- b) Different models of the Zacate, Ontario and Desna lines include slightly different GPUs, nevertheless all have the same number of processing units (80), as shown below.

2.3.2 Mobile APU lines of the Brazos platform (11)

Use of different GPU cores in different mobile processors [29]

"Zacate" (40 nm)

Model	Step.	CPU						GPU				Memory	TDP	Released
		Cores	Freq.	Turbo	L2 Cache	Multi ¹	V _{core}	Model	Config ²	Freq.	Turbo			
E-240	B0	1	1.5 GHz	N/A	512 KB	15×	1.175 - 1.35	HD 6310	80:8:4	500 MHz	N/A	DDR3-1066	18 W	Jan 4, 2011
E-300	B0	2	1.3 GHz		2 × 512 KB	13×	1.25 - 1.35			488 MHz		DDR3-1333		Aug 22, 2011
E-350	B0		1.6 GHz			16×				492 MHz		DDR3-1066		Jan 4, 2011
E-450	C0	1.65 GHz	16.5×		HD 6320	80:8:4	508 MHz			600 MHz	DDR3-1333	Aug 22, 2011		
E1-1200		1.4 GHz	14×		HD 7310	80:8:4	500 MHz			N/A	DDR3-1066	Q1 2012		
E2-1800		1.7 GHz	17×		HD 7340	80:8:4	523 MHz			680 MHz	DDR3-1333			

"Ontario" (40 nm)

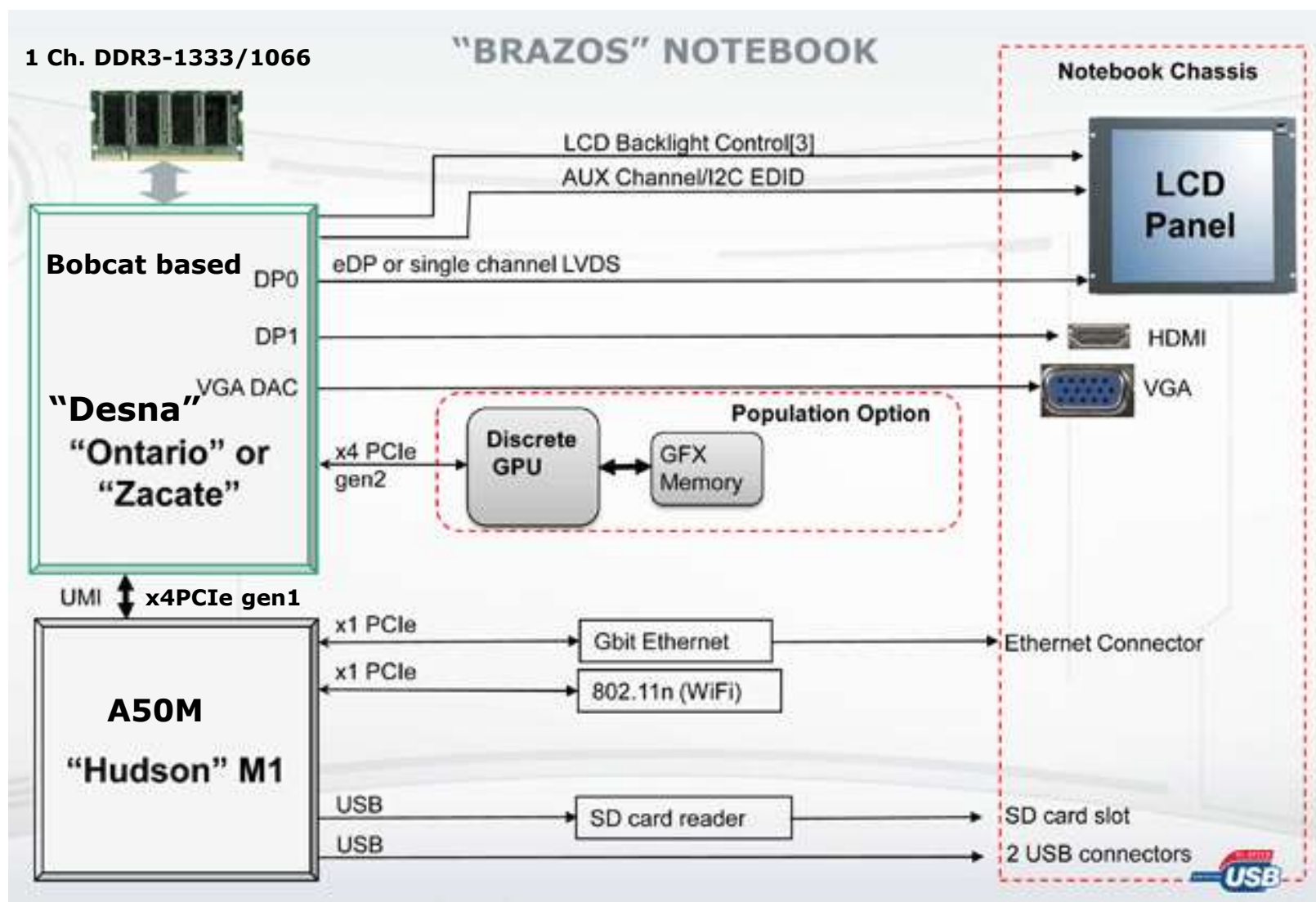
Model	Step.	CPU						GPU				Memory	TDP	Released
		Cores	Freq.	Turbo	L2 Cache	Multi ¹	V _{core}	Model	Config ²	Freq.	Turbo			
C-30	B0	1	1.2 GHz	N/A	512 KB	12×	1.25 - 1.35	HD 6250	80:8:4	276 MHz	N/A	DDR3-1066	9 W	Jan 4, 2011
C-50		2	1.0 GHz		2 × 512 KB	10×	1.05 - 1.35							400 MHz
C-60	C0		1.33 GHz				10-13.3×		HD 6290	80:8:4	276 MHz	400 MHz		

"Desna" (40nm)

Model	Step.	CPU						GPU				Memory	TDP	Released
		Cores	Freq.	Turbo	L2 Cache	Multi ¹	V _{core}	Model	Config ²	Freq.	Turbo			
Z-01	B0	2	1.0 GHz	N/A	2 × 512 KB	10×		HD 6250	80:8:4	276 MHz	N/A	DDR3-1066	5.9 W	June 1, 2011
Z-03													4.5 W	Q1 2012

2.3.2 Mobile APU lines of the Brazos platform (12)

The Brazos notebook platform [37]



2.3.2 Mobile APU lines of the Brazos platform (13)

Positioning the Hudson-M1 (A50M) Fusion Controller Hub (FCH) [38]

- All models support up to 4 channels of HD audio.
- A55T support up to 2 channels of HD audio.

Model	Codename	Platform	Fab (nm)	UMI	SATA	USB 3.0 + 2.0 + 1.1	RAID	Gb Ethernet MAC	33 MHz PCI	SD ¹	VGA DAC	TDP (W)	Features / Notes		
A55T	Hudson-M2T ^[N 1]	"Brazos" T		×2 Gen 1	1 × 3 Gbit/s AHCI 1.1	0+8+0	No	No		SDIO	No				
A50M	Hudson-M1 ^[N 1]	"Brazos"		×4 Gen 1 ^[M 1]	6 × 6 Gbit/s	0 + 14 + 2				No			~920mw idle		
A60M	Hudson-M2 ^[N 1]	"Sabine"	65	×4 Gen 1 +DP	AHCI 1.2		RAID 0,1	10/100/1000	No	Yes	Yes	4.7			
A68M	Hudson-M3L ^[N 1]	"Brazos" 2.0			2 × 6 Gbit/s AHCI 1.2	2+8+0					No		No	~750mw idle	
A70M	Hudson-M3 ^[N 1]	"Indus" "Comal" "Sabine"			6 × 6 Gbit/s AHCI 1.2	4 + 10 + 2					Yes		Yes	First native USB 3.0 controller ^[6]	
A45	Hudson-D1 ^[N 2]				6 × 3 Gbit/s AHCI 1.1	0 + 14 + 2					No		No	Up to 4 slots	No
A55	Hudson-D2 ^[N 2]		65	×4 Gen 2 +DP	6 × 6 Gbit/s AHCI 1.2	4 + 10 + 2	RAID 0,1,10	10/100/1000	Up to 3 slots	Yes	Yes	7.8	First native USB 3.0 controller ^[6]		
A75	Hudson-D3 ^[N 2]	"Lynx"												8 × 6 Gbit/s AHCI 1.2	RAID 0,1,5,10
A85X	Hudson-D4	"Virgo"												6 × 6 Gbit/s AHCI 1.2	0 + 14 + 2
A55E	Hudson-E1 ^[N 3]		65	×4 Gen 2	6 × 6 Gbit/s AHCI 1.2	0 + 14 + 2	RAID 0,1,5,10	10/100/1000	Up to 4 slots	No	No	5.9			

Codenames:

M: for notebook platform
D: for desktop platform
E: for embedded platform

UMI:

UMI ×4 Gen 1 is based on [PCIe 1.1](#) × 4 lanes, giving 1 GBps bandwidth
 UMI ×4 Gen 2 is based on [PCIe 2.0](#) × 4 lanes, giving 2 GBps bandwidth

2.3.2 Mobile APU lines of the Brazos platform (14)

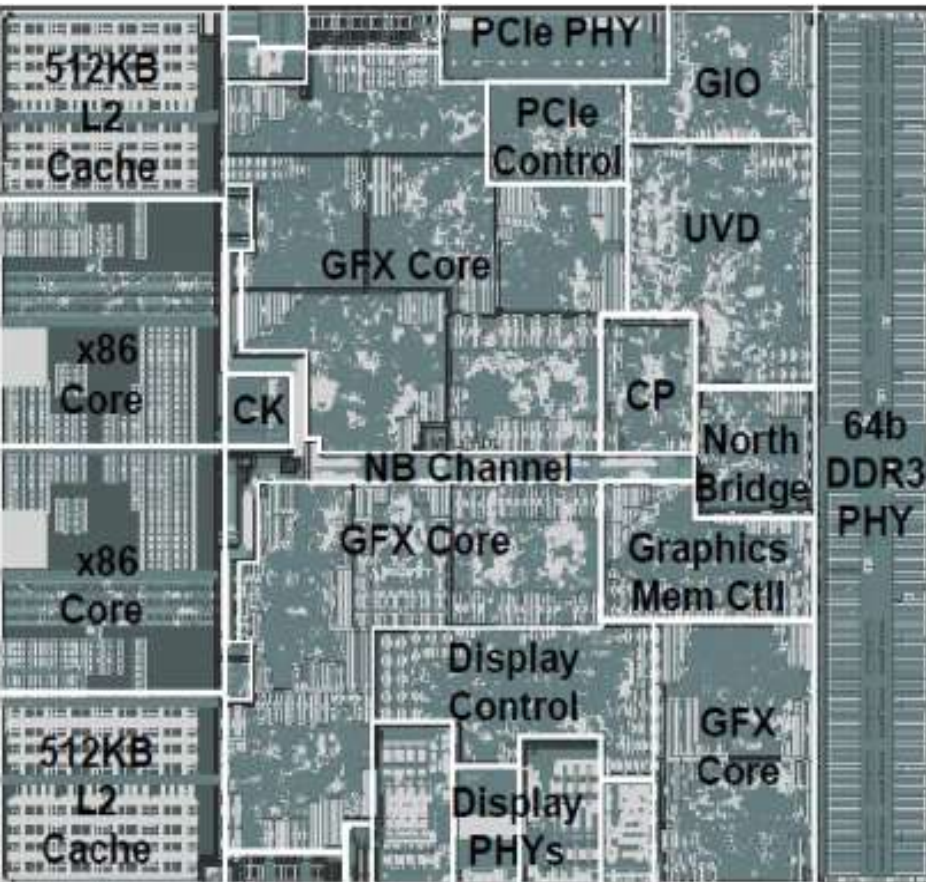
Die plots of the Zacate, Ontario and Desna APUs

All three APUs have **the same die plot**, as demonstrated below.

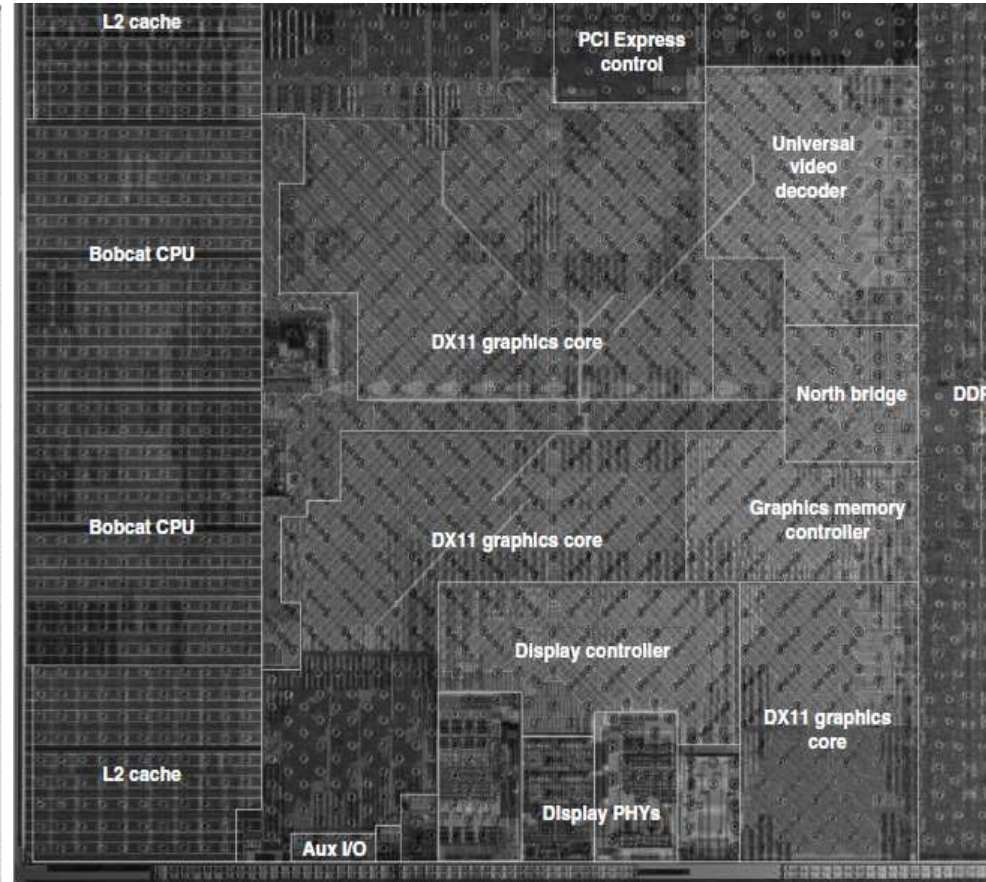
2.3.2 Mobile APU lines of the Brazos platform (15)

Die plots of the Zacate and Ontario processors [28], [31]

Zacate



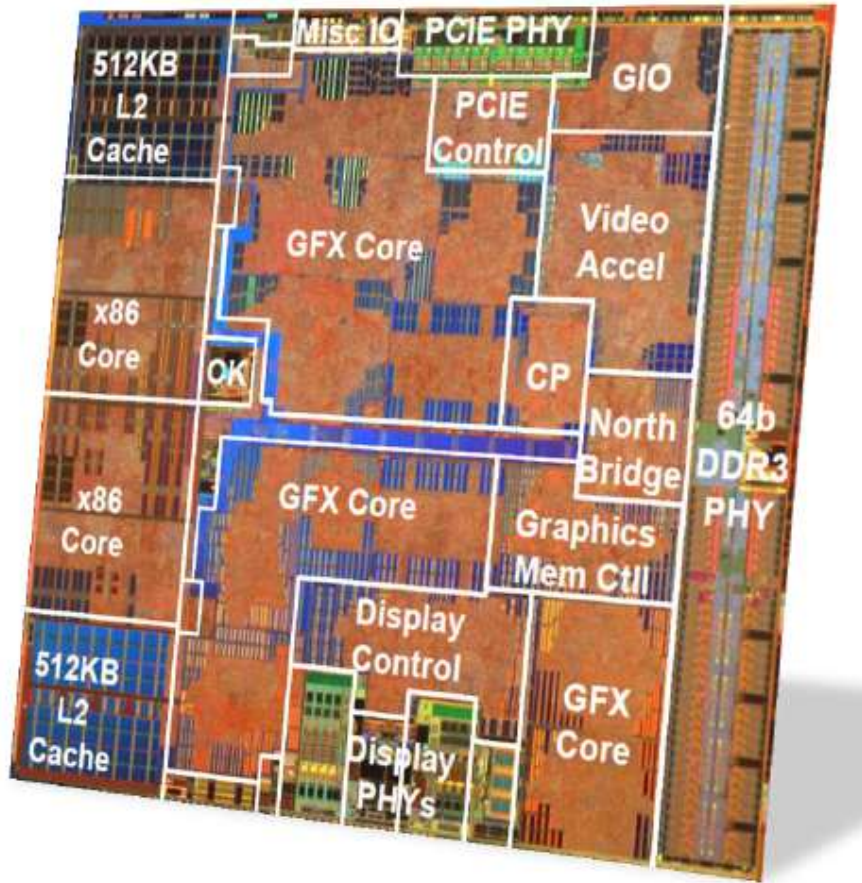
Ontario



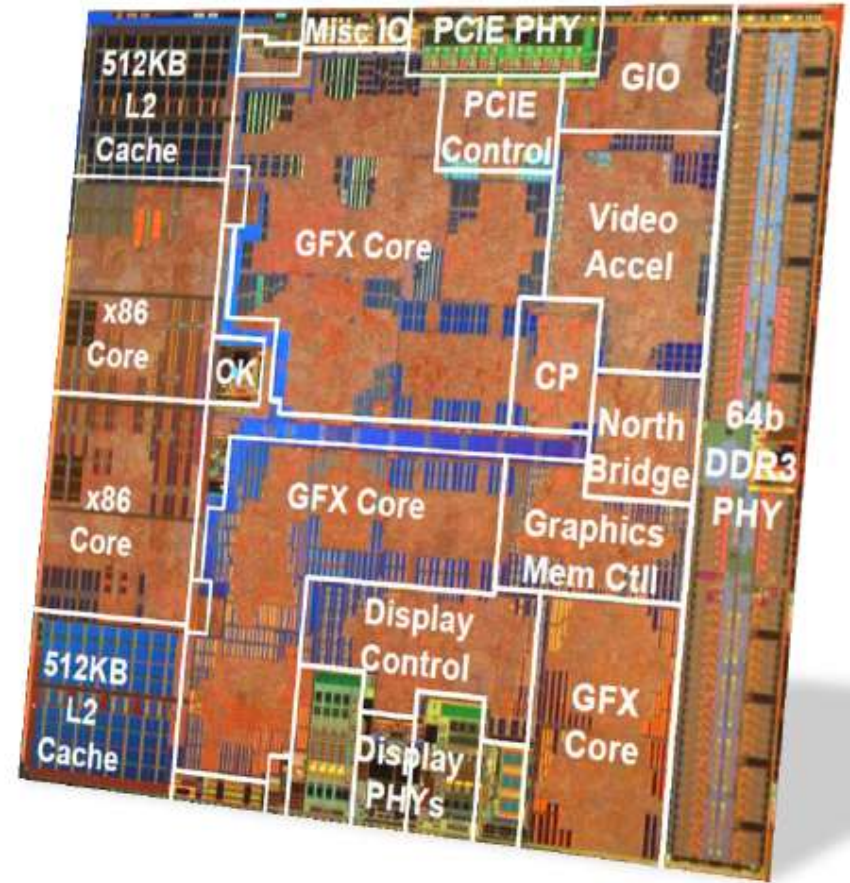
2.3.2 Mobile APU lines of the Brazos platform (16)

Die plots of the Zacate and Desna processors [36]

Zacate

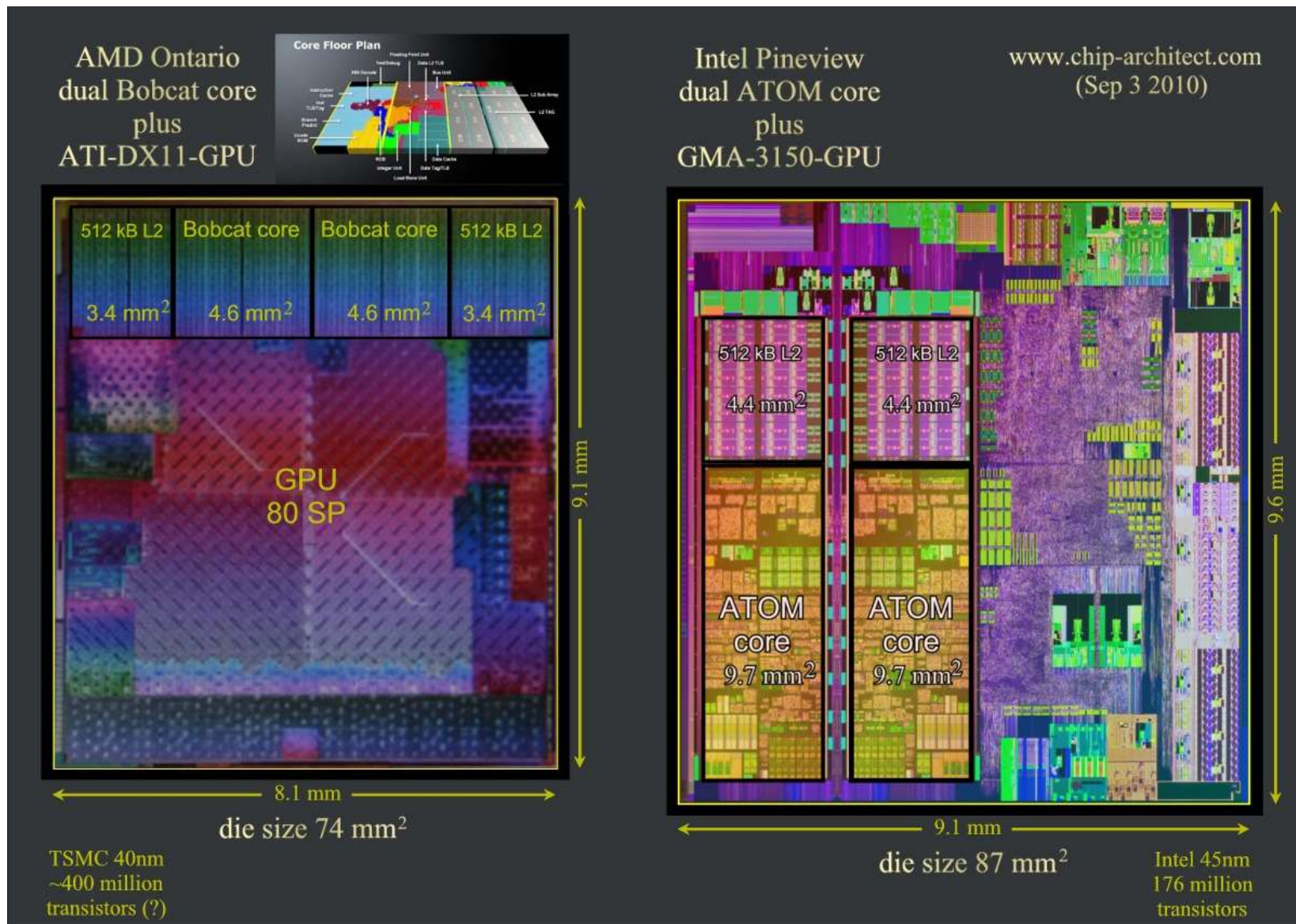


Desna



2.3.2 Mobile APU lines of the Brazos platform (17)

Contrasting the die plots of Ontario and Intel's Pineview dual core Atom processor [39]



2.3.2 Mobile APU lines of the Brazos platform (18)

OpenCL programming support for the Ontario and the Zacate lines

AMD's APP SDK 2.3 (1/2011) (formerly ATI Stream SDK) (provides OpenCL support for both lines .

New features of APP SDK 2.3 [40]

Improved OpenCL runtime performance:

- Improved kernel launch times.

- Improved PCIe transfer times.

- Enabled DRMDMA for the ATI Radeon 5000 Series and AMD Radeon 6800 GPUs that are specified in the [Supported Devices](#).

- Increased size of staging buffers.

- Enhanced Binary Image Format (BIF).

- Support for UVD video hardware component through OpenCL (Windows 7).

- Support for AMD E-Series and C-Series platforms (AMD Fusion APUs).

- Support for Northern Islands family of devices.

- Support for AMD Radeon™ HD 6310 and AMD Radeon™ 6250 devices.

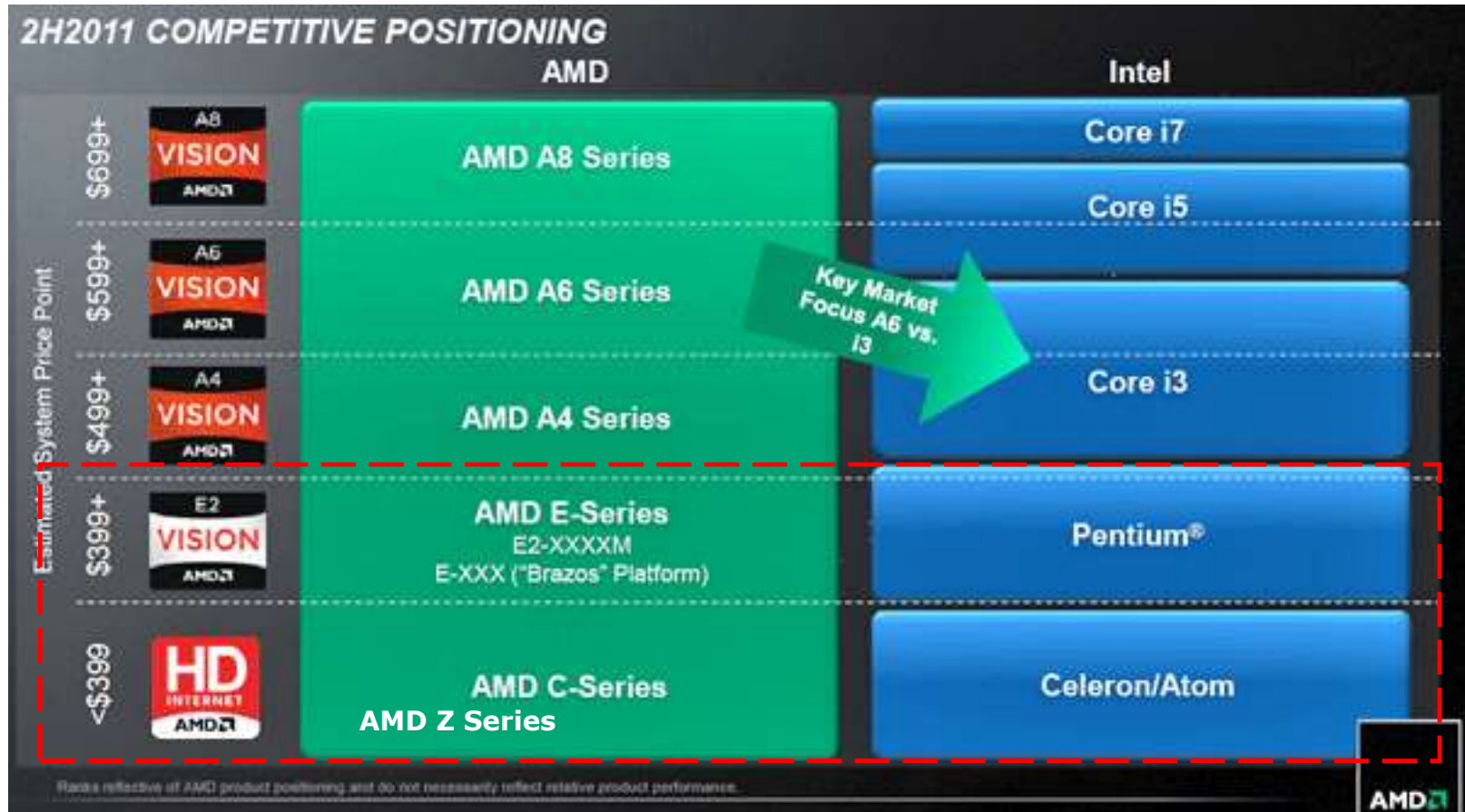
- Support for OpenCL math libraries: FFT and BLAS-3, available for download at [AMD Accelerated Parallel Processing Math Libraries](#).

- Preview feature: An optimization pragma for unrolling loops.

- Preview feature: Support for CPU/X86 image. This enables the support for Image formats, as described in the Khronos specification for OpenCL, to be run on the x86 CPU. It is enabled by the following environment variable in your application: CPU_IMAGE_SUPPORT.

2.3.2 Mobile APU lines of the Brazos platform (19)

Positioning of the Bobcat-based Brazos mobile lines vs. Intel's lines [41]



Remark

A-Series processors address the midrange and high-end market [41]

2.3.2 Mobile APU lines of the Brazos platform (20)

Main features of Bobcat-based ultra-portable mobile lines with a TDP of ~10-20W

Base arch./stepping	Intro	Ultra-portable mobile family	Series	Techn.	Core count (up to)	L2 (up to)	L3	GPU (APU)	Memory (up to)	TDP [W]	Socket
Family14h (00h-0fH) (Bobcat)	1/2011	Zacate (not SoC)	E Series	40 nm	2	512 KB/ core Private	-	Yes	DDR3L- 1333	18	FT1 (BGA)
	6/2012	Zacate (not SoC)	E1/E2 Models	40 nm	2	512 KB/ core Private	-	Yes	DDR3L- 1333	18	FT1 (BGA)
	1/2011	Ontario	C Series	40 nm	2	512 KB/ core private	-	Yes	DDR3- 1066	9	FT1 (BGA)
Family 16h (10H-1fH) (Jaguar)	5/2013	Kabini (SoC)	A Series	28 nm	4 cores with a shared L2 cache	2 MB shared	-	Yes	DDR3L- 1866	9/ 15	FT3
Family 16h (30H-3fH) (Puma+)	4/2014	Beema (SoC)	A Series	28 nm		2 MB shared	-	Yes	DDR3L- 1866	15	FT3b
	5/2015	Carrizo-L (SoC)	A Series	28 nm		2 MB shared	-	Yes	DDR3L- 1866	10/ 15	FP4
Family 17h (00H-0fH) (Zen)	10/2017	Raven Ridge (SoC)	Ryzen 7/5/3	14 nm	4-core CCX, private L2 and shared L3 cache(s)	½ MB/ core	1 MB/ core	Yes	DDR4- 2400	15	AM4

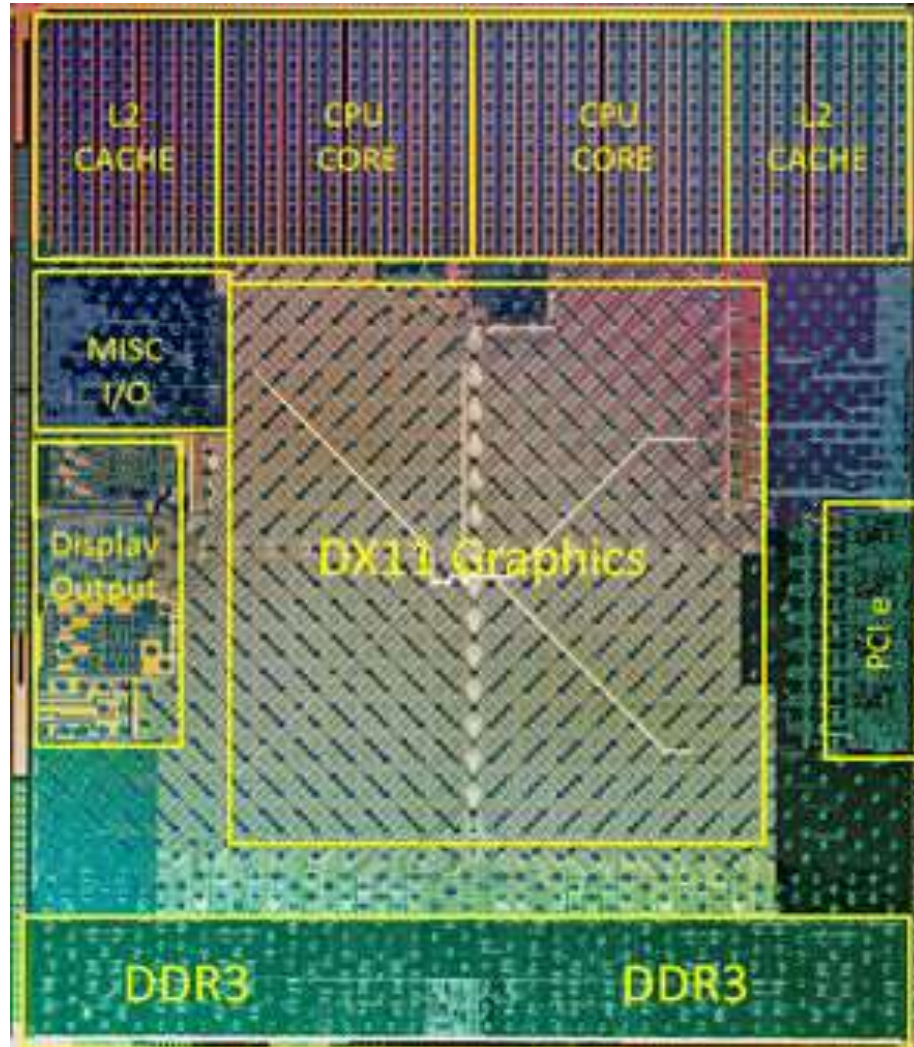
APU: Accelerated Processing Unit (CPU +GPU) CCX: Core Complex

²: 2*512 KB for Turion X2, 2*1 MB for Turion X2 Ultra

UMI: Universal Media Interface

2.3.2 Mobile APU lines of the Brazos platform (21)

Die plot of the Zacate APU [42]



2.3.2 Mobile APU lines of the Brazos platform (22)

"Zacate" (40nm)

[edit]

- All models support: *SSE, SSE2, SSE3, SSSE3, SSE4a, NX bit, AMD64, PowerNow!, AMD-V*
- Memory support: *DDR3 SDRAM, DDR3L SDRAM* (Single-channel, up to 1066 MHz)
- Config GPU are *Unified Shaders (Vertex shader/Geometry shader/Pixel shader) : Texture mapping unit : Render Output unit*

Model Number	CPU cores	Freq.	L2 Cache	Multi ¹	Voltage	Model GPU	Config GPU	GPU Freq.	UMI	TDP	Socket	Release Date
E-Series E _z -240	1	1.5 GHz	512 KB	18.75x	1.175 - 1.35	HD 6310	80:8:4	500MHz	2.5 GT/s	18 W	BGA-413	January 4, 2011
E-Series E _z -350	2	1.6 GHz	2x 512 KB	20x	1.25 - 1.35	HD 6310	80:8:4	500MHz	2.5 GT/s	18 W	BGA-413	January 4, 2011

Table: Main features of AMD's mainstream Zacate Fusion APU line [43]

"Ontario" (40nm)

[edit]

- All models support: *SSE, SSE2, SSE3, SSSE3, SSE4a, NX bit, AMD64, PowerNow!, AMD-V*
- Memory support: *DDR3 SDRAM, DDR3L SDRAM* (Single-channel, up to 1066 MHz)
- Config GPU are *Unified Shaders (Vertex shader/Geometry shader/Pixel shader) : Texture mapping unit : Render Output unit*

Model Number	CPU cores	Freq.	L2 Cache	Multi ¹	Voltage	Model GPU	Config GPU	GPU Freq.	UMI	TDP	Socket	Release Date
C-Series C _z -30	1	1.2 GHz	512 KB	15x	1.25 - 1.35	HD 6250	80:8:4	280MHz	2.5 GT/s	9 W	BGA-413	January 4, 2011
C-Series C _z -50	2	1.0 GHz	2x 512 KB	12.5x	1.05 - 1.35	HD 6250	80:8:4	280MHz	2.5 GT/s	9 W	BGA-413	January 4, 2011

Table: Main features of AMD's low power Ontario Fusion APU line [43]

2.4 Bobcat-based APU lines of the Brazos 2.0 platform

2.4 APU lines of the Brazos 2.0 platform (1)

APU lines of the Brazos 2.0 platform

Introduced in 6/2012

Brazos 2.0 APU line

Zacate APUs

E2-1800

E1-1200

18 W

DX 11 support

OpenCL 1.1 support

GPU Turbo mode available on the E2-1800 model.

The [same models are used both in value desktops and value notebooks](#) (termed also as extra portable notebooks).

Contrasting the Brazos 2.0 and Brazos platforms

a) Contrasting the Brazos 2.0 APUs and the previous Brazos APUs [44].

Neither of the E2-1800 and the E1-1200 CPU cores are **new designs but only minor upgrades** of the previous Brazos E-450 and E-300 CPUs, as detailed in the subsequent Remark.

2.4 APU lines of the Brazos 2.0 platform (3)

Remark

Differences of the Brazos 2.0 APUs from the previous Brazos APUs

- The **CPUs** of the Brazos 2.0 APUs are **minor upgrades** of the previous Brazos line, as follows:
The E2-1800 is an upgrade of the previous Brazos E-450 whereas the E2-1200 is an upgrade of the E-300.

The improvement is restricted to a few % clock speed increase, as indicated in the Table below.

- The **GPUs** associated with the Brazos 2.0 APUs are **rebranded GPUs of the HD 6xxx line**, as follows:

The HD 7310 is a rebranded HD 6310 whereas the HD 7340 is a rebranded HD 6320, both with a slight clock speed increase, as shown below.

	Brazos 2.0		Brazos	
	E2-1800	E2-1200	E-450	E-300
fc of the CPU	1.7 GHz	1.4 GHz	1.65 GHz	1.3 GHz
GPU type	HD 7310	HD 7340	HD 6310	HD 6320
Basic fc of the GPU	523 MHz	500 MHz	508 MHz	488 MHz
Turbo fc of the GPU	680 MHz	--	600 MHz	--

2.4 APU lines of the Brazos 2.0 platform (4)

b) Contrasting the FCHs of the Brazos 2.0 platform with those of the previous Brazos platform [45].

	Notebook		Desktop	
	A50M	A68M	A45	A68
2011 Branding	A50M	A68M	A45	A68
Target Platform	"Brazos"	"Brazos 2.0"	"Brazos"	"Brazos 2.0"
PCI Express Support (CF)	Y	1x4	Y	1x4
Clock Gen	N	Y	N	Y
SATA	6 x 6Gb/s	2 x 6Gb/s	6 x 3Gb/s	3 x 6Gb/s
HD Audio	Up to 4-codecs	Up to 4-codecs	Up to 4-codecs	Up to 4-codecs
PCIe GPPs	4 x1 Gen 2	4 x1 Gen 2	4 x1 Gen 2	4 x1 Gen 2
Unified Media Interface (UMI)	x4 Gen 1	x4 Gen 2	x4 Gen 2	x4 Gen 2
USB 3.0 + 2.0 + 1.1 Ports	0 + 14 + 2	2 + 8 + 0	0 + 14 + 2	2 + 8 + 0
APU Fan Control	Y	Y	Y	Y
SD Controller	N	Y	N	Y
33MHz PCI	N	N	Up to 4 slots	Up to 3 slots

As indicated, the major differences are additional PCIe 2.0 x4 and USB 3.0 support in Brazos 2.0 FCHs.

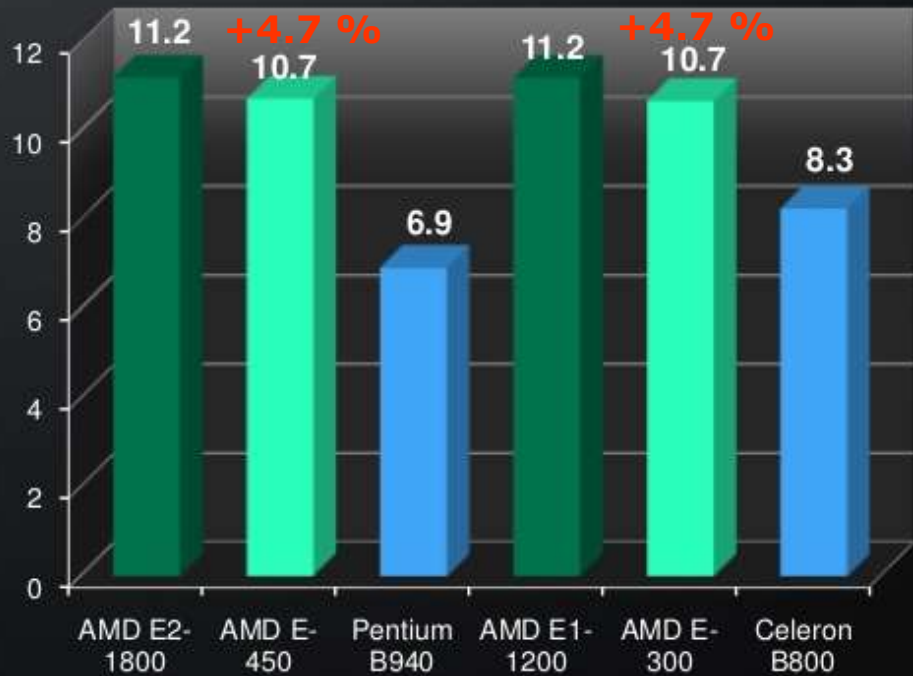
2.4 APU lines of the Brazos 2.0 platform (5)

Battery life comparison of Brazos, Brazos 2.0 and Intel's Atom models [45]

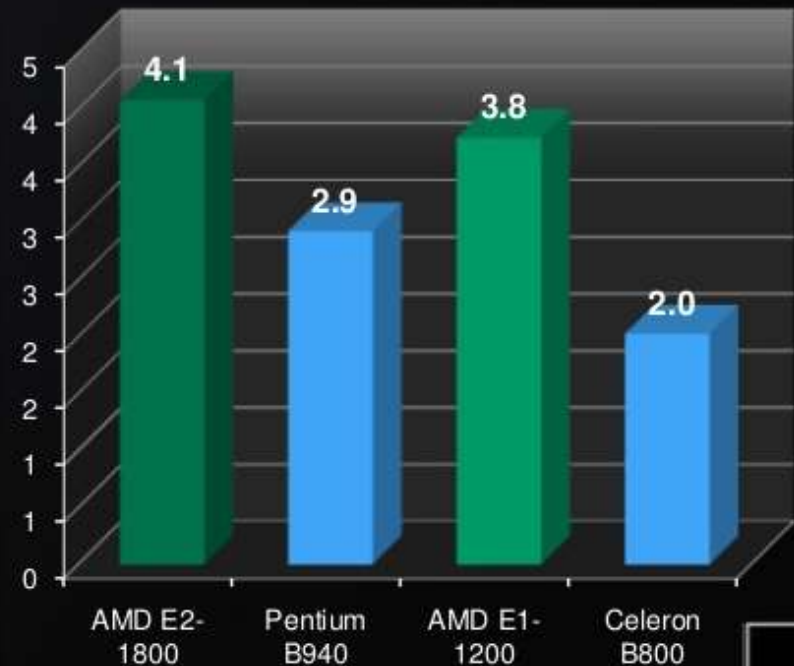
*Exceptional mobility with
up to 11+ hours of battery life*

*Up to 90 minutes more Flash gaming
time over the competition**

Hours Windows Idle



Hours of Flash Gaming



* See footnotes

2.4 APU lines of the Brazos 2.0 platform (6)

Main features of Mobile APU models of the Brazos 2.0 platform [45]

2012 AMD E-Series APU for Essential Notebooks and Desktops								
APU Model	AMD Radeon™ Brand	TDP	CPU Cores	CPU Clock (Max/Base)	AMD Radeon™ Cores	GPU Clock (Max/Base)	L2 Cache	Max DDR3
E2-1800	HD 7340	18W	2	1.7GHz	80	680MHz/ 523MHz	1MB	DDR3-1333 DDR3L1066 DDR3U-1066
E1-1200	HD 7310	18W	2	1.4GHz	80	500MHz	1MB	DDR3-1066 DDR3L-1066 DDR3U-1066

2.4 APU lines of the Brazos 2.0 platform (7)

The Brazos 2.0 platform [45]

“Zacate” APUs

•Dual Core CPU

- 40nm “Bobcat” core – 1 MB L2, 64-bit FPU
- 18W TDP
- Complete ISA support
- SSE1-3 and virtualization

•Graphics Core

- 80 Radeon™ Cores
- New AMD Radeon™ HD 7000 Series GPU
- DirectX® 11 capable
- OpenCL™ 1.1 enabled

•Improved graphics boost

•AMD VISION Engine

•3rd generation Unified Video Decoder

•DDR3 1066-1333, 2 DIMMs

•FT1 BGA package (same as current Brazos)

Display and I/O

•Two dedicated digital display interfaces

- Configurable as HDMI, DVI, and/or Display Port
- Also supports single link LVDS for internal panels

•VGA

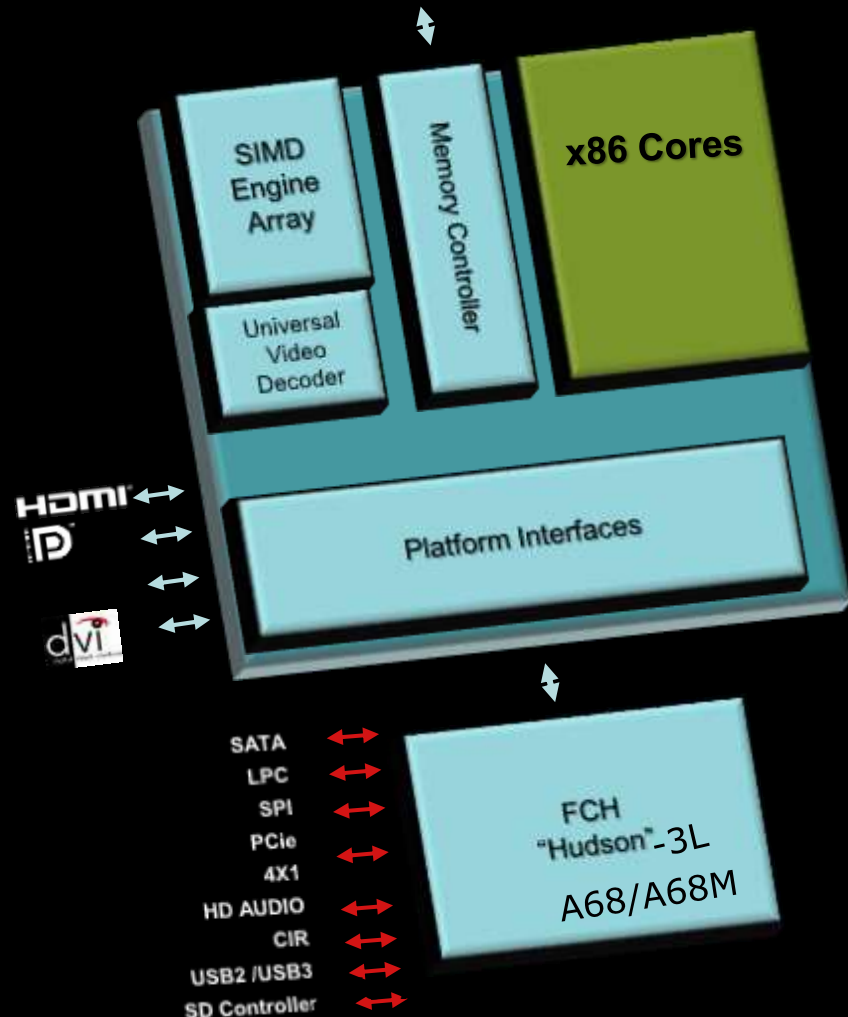
•8 PCIe Gen 2

•“Hudson-3L” FCH

- USB 3.0 Support (2 ports) / USB 2.0 (8 ports)

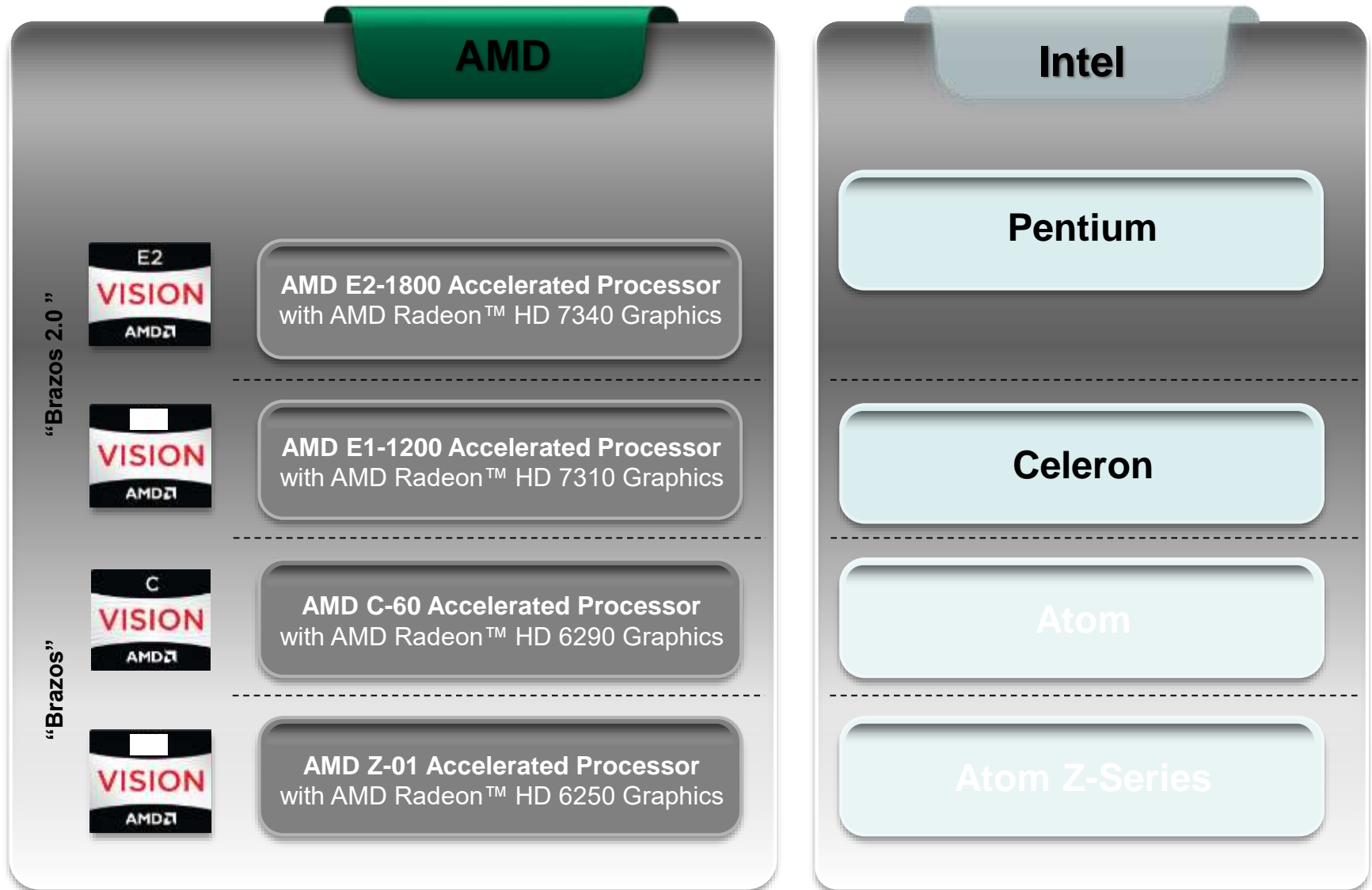
FCH

- Desktops: A68
- Mobiles: A68M



2.4 APU lines of the Brazos 2.0 platform (8)

Positioning the Brazos 2.0 APU models [45]



2.5 APU lines of the Embedded G-Series platform

Embedded G-Series

- Introduced in 1/2011
- Typical use: In TV Set Top Boxes
- They are basically Zacate, Ontario or Desna designs, as shown below.

2.5 APU lines of the Embedded G-Series platform (2)

Main features of the embedded GPU lines [29]

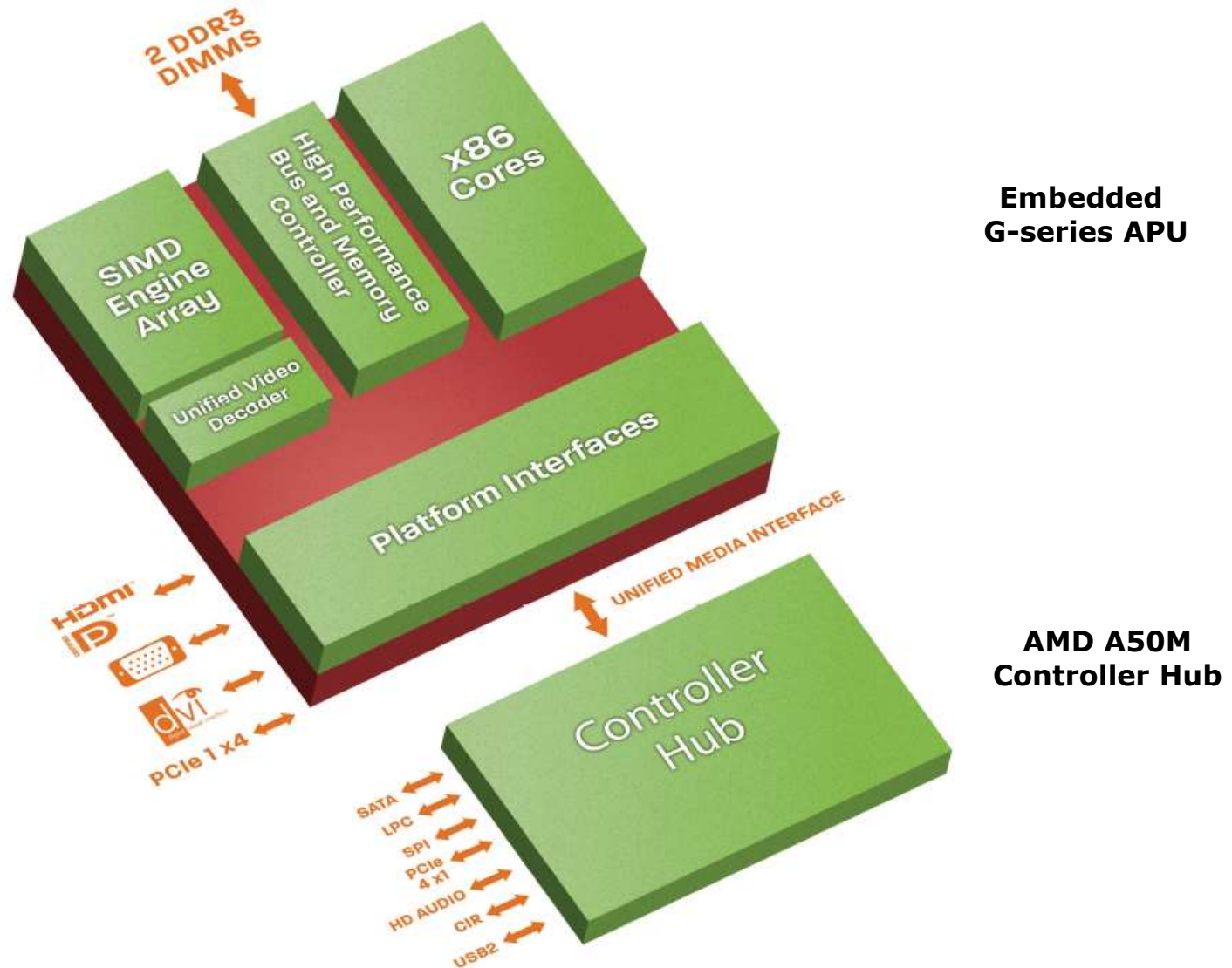
		Core count	L2	fc CPU	GPU Direct X11	fc GPU			
E m b e d d e d	G-series with GPU	18 W	2C	2x512 KB	1.4-1.65 GHz	HD 6310	500/520 MHz	^{1/11} Zacate 40 nm, Up to DDR3-1333 FTI BGA T48N ----- T56N T52R (1C disabled)	
			1C	512 KB					HD 6320
		9 W	2C	2x512 KB	1.0-1.2 GHz	HD 6250	280 MHz		^{1/11} Ontario T40N ----- T44R
			1C	512 KB		HD 6290			
		6.4/5.5 W	2C	2x512 KB	1.0 GHz	HD 6250	280 MHz		^{6/11} Desna T40E ----- T40R (1 C disabled)
			1C	512 KB					
	G-Series without GPU	18 W	2C	2x512 KB	1.4 GHz	—	—	^{3/11} Zacate T48 L ----- T30 L (GPU disabled)	
			1C	512 KB					
5 W	1C	512 KB	0.8-1.0 GHz	—	—	^{3/11} Desna T24 L (1C disabled) (GPU disabled)			

Graphics support of the G-Series [46]

- Direct X 11 with Shader Model 5
- Open CL 1.1
- Open GL 3.2.2.1

2.5 APU lines of the Embedded G-Series platform (4)

System architecture of a Bobcat-based embedded GPU lines [47]



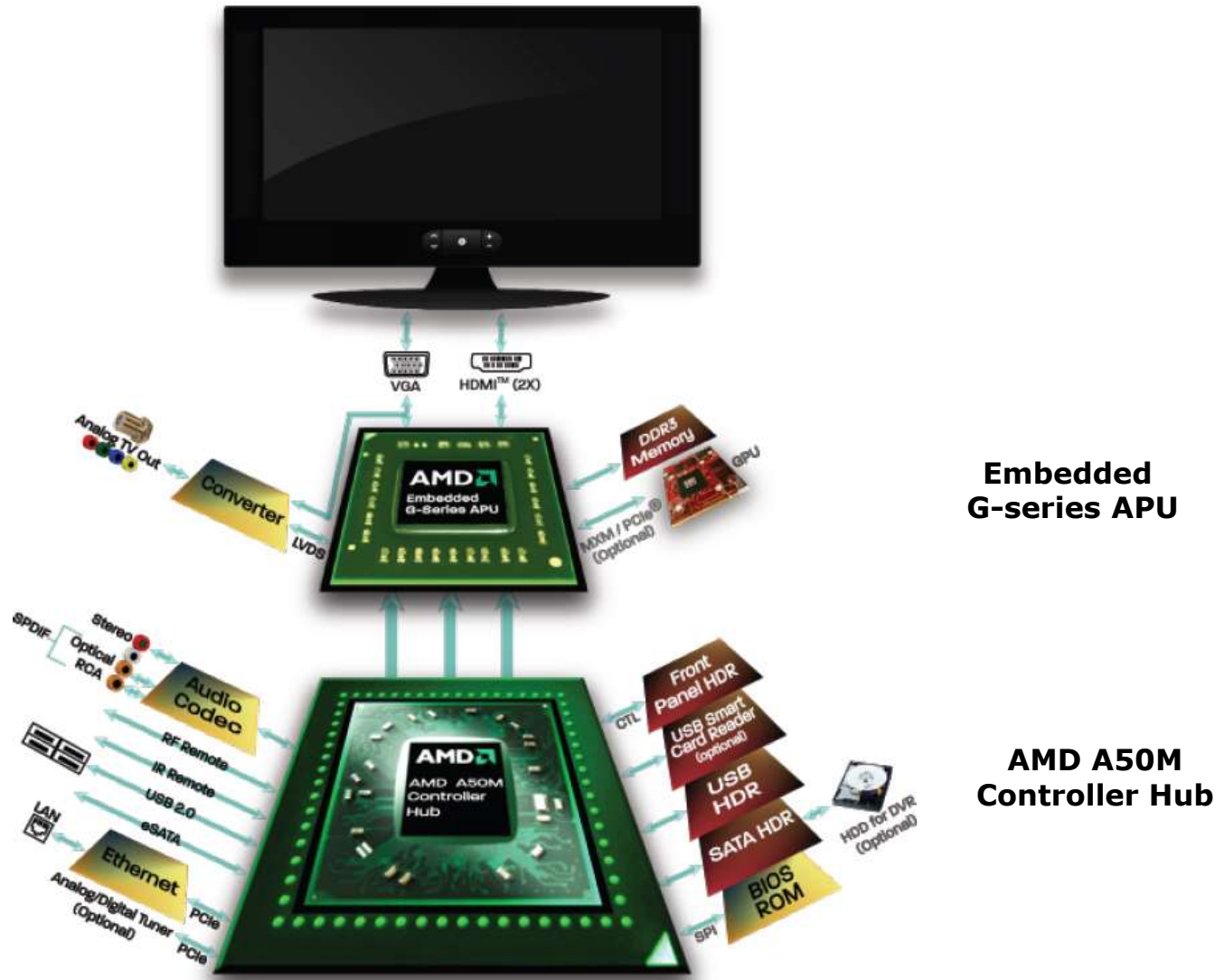
2.5 APU lines of the Embedded G-Series platform (5)

Main features of the Controller Hubs of the lines of the Embedded G-Series platform [47]

Model	PCI Express®	PCI	Gigabit Ethernet MAC	RAID	SATA	USB	Additional Interfaces/Features
A55E	4x1 or 1x4 PCIe® Generation 2 UMI connection to APU	33MHz with support for 4 masters	Yes	0/1/5/10 support with FIS-based switching	6x 6Gb/s ports	14x v2.0 ports	SPI, LPC, SMBus, CIR, HD audio, up to 102 GPIO, Fan control, Integrated Clock Generation, pin compatible for A50M and A55E
A50M	4x1 or 1x4	No	No	No			

2.5 APU lines of the Embedded G-Series platform (6)

Use of a Bobcat-based embedded APU in a TV set top box [48]



3. Family 16h Models 00h-0Fh (Jaguar-based) APU lines

- 3.1 Overview of the Jaguar-based APU lines
- 3.2 The Jaguar core
- 3.3 Jaguar-based APU lines

3.1 Overview of the Jaguar-based APU lines

3.1 Overview of the Jaguar-based APU lines (1)

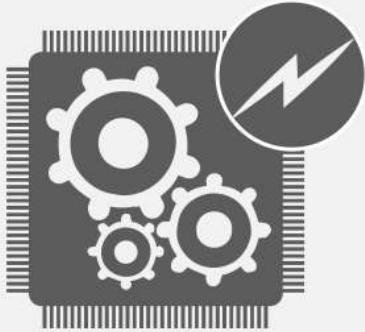
3.1 Overview of the Jaguar-based APU lines -1

- **Jaguar-based APUs** are AMD's second low power oriented product series that were announced at the Hot Chips 2012 in 8/2012 and introduced in 5/2013.
They focus on the **mobile market**, especially on ultra-light notebooks and tablets but include also a line of **micro servers**, released in 5/2013 as well.
- Jaguar-based products follow AMD's successful Bobcat-based product lines of the Brazos platform that are typically used in ultra-light notebooks and tablets.
- Jaguar-based APUs **compete with Intel's Atom line of processors, and also with ARM designs**, as ARM's processor design were used in most smartphones and tablets, e.g. in Apple's iPad, Google's Galaxy Nexus 7 and Amazon's Kindle Fire [49].
- They are **part of AMD's new market strategy that emphasizes the mobile market segment in AMD's overall market policy**.
- Jaguar-based APU products include basically **up to four Jaguar cores and a GPU** with similar capabilities than a low-end discrete graphics card.
- **28 nm** technology, **~ 110 mm² die size** (compared to 75 mm² of Bobcat-based APUs + 28 mm² for the associated FCH) [50] and 1178 mtrs (vs. 450 mtrs for Bobcat-based APUs) [51].

3.1 Overview of the Jaguar-based APU lines (2)

Design goals of the Jaguar-based APU lines [26]

IMPROVE ON "Bobcat": PERFORMANCE IN A GIVEN POWER ENVELOPE



- ▶ More IPC
- ▶ Better Frequency at given Voltage
- ▶ Improved power efficiency thru clock gating and unit redesign

UPDATE THE ISA/FEATURE SET



- ▶ "Jaguar"added:
 - ▶ SSE4.1, SSE4.2
 - ▶ AES, CLMUL
 - ▶ MOVBE
 - ▶ AVX, XSAVE/XSAVEOPT
 - ▶ F16C, BMI1
- ▶ 40 bit physical address capable
- ▶ Improved virtualization

INCREASE PROCESS PORTABILITY



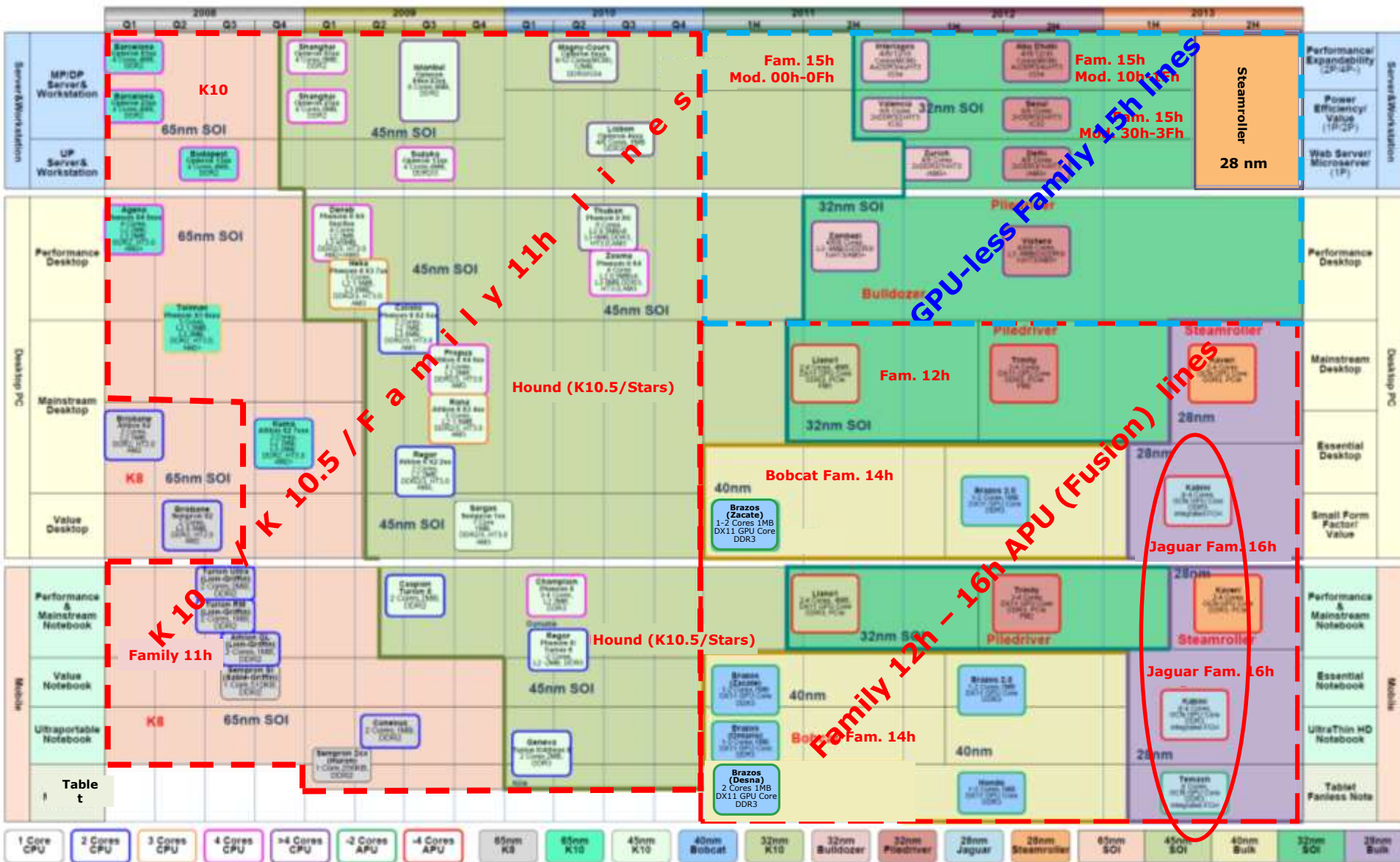
3.1 Overview of the Jaguar-based APU lines (3)

Remark

Process portability means the ability of different manufacturers to take the Jaguar design and fabricate it [52].

3.1 Overview of the Jaguar-based APU lines (4)

Positioning the Jaguar-based APU lines (The Kyoto micro server line not shown)[based on 14]



3.1 Overview of the Jaguar-based APU lines (5)

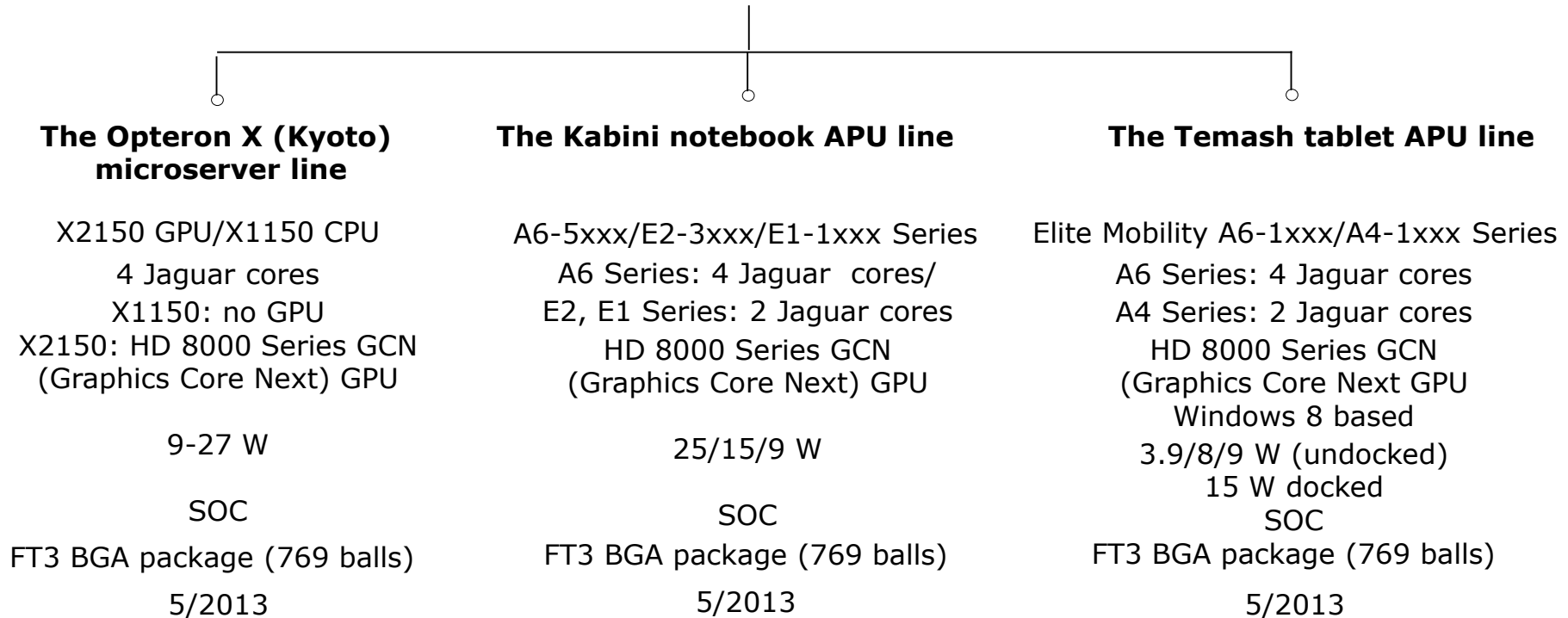
Brand names of AMD's Jaguar-based processor lines

	Launched in	2011	2012	2013	2014	2015
		Family 14h (00h-0Fh) (Bobcat)	Family 14h (00h-0Fh) (Bobcat)	Family 16h (00h-0Fh) (Jaguar)	Family 16h (30h-3Fh) (Puma+)	Family 16h (30h-3Fh) (Puma+)
Servers	4P servers					
	2P servers					
	1P servers					
	(85-140 W)					
Desktops	High perf. (~95-125 W)					
	Mainstream (~65-100 W)					
	Entry level (~30-60 W)					
Notebooks	High performance/ mainstream/entry (~30-60 W)			Kabini A6		
	Ultra portable (~10-15 W)	Zacate E-Series Ontario C-Series	Zacate E1/E2	Kabini A/E-Series	Beema A/E-Series	Carrizo-L A/L-Series
	Tablet (~5 W)	Desna Z-Series		Temash A Series	Mullins A Series/E1	

3.1 Overview of the Jaguar-based APU lines (6)

Overview of the Jaguar-based APU lines

Jaguar-based APU lines



3.1 Overview of the Jaguar-based APU lines (7)

Overview of Jaguar cores in game consoles [52], [53]

- Sony's **PS4 (Playstation 4)** (the previous PS3 incorporated a Sony/Toshiba/IBM Cell processor and an Nvidia graphics chip, the GeForce 7000)
- Microsoft's **Xbox One** (the previous Xbox 360 incorporated a triple core IBM PowerPC-based processor and an AMD GPU)
- Nintendo **Wii U** (the previous Wii incorporated a single-core IBM PowerPC-based processor and an ATI GPU).

Design goals of the Jaguar core [3]

"JAGUAR" DESIGN GOALS

- Improve on "Bobcat": performance in a given power envelope
 - More IPC
 - Better Frequency at given Voltage
 - Improve power efficiency thru clock gating and unit redesign
- Update the ISA/Feature Set



3.1 Overview of the Jaguar-based APU lines (9)

Manually power optimized design of the Jaguar core [4]

- The Jaguar core uses the 28 nm process technology and has a small area of 3.1 mm².
- The core design was manually optimized by using Calypto's PowerPro power simulation tool.
- This tool analysis pre synthesis design and provides hints for improving clock gating.
- The design team made a number of design iteration cycles, each requiring a number of weeks, to reduce the number of active (not gated) flip-flops in the design.

3.1 Overview of the Jaguar-based APU lines (10)

Example: Reducing the number of active (not gated) flops during cpu-halt in the design iteration process

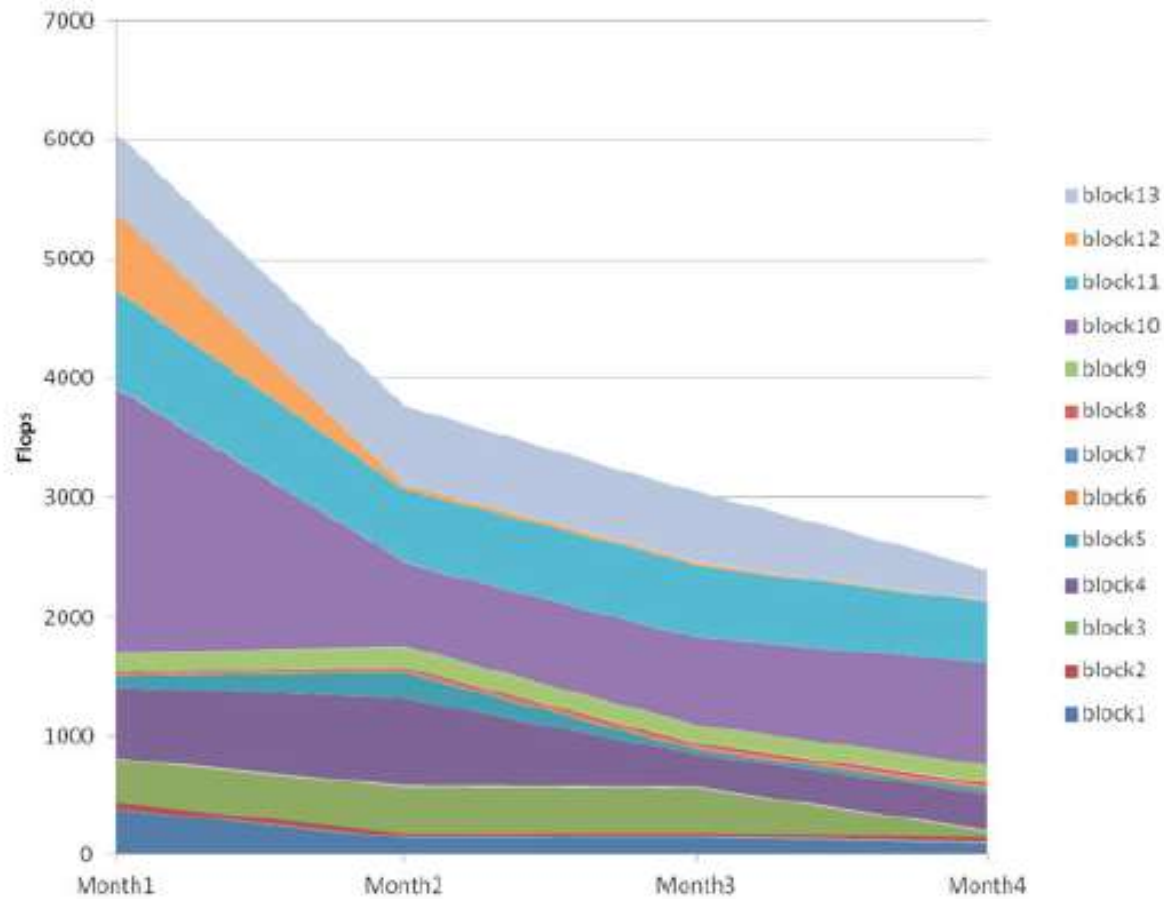


Figure: Average clocked flops during cpu-halt [4]

Results of the manually optimized design of the Jaguar core

One of the circuit designers summarized **the results of the design efforts** as follows:

“As design goals included increasing the frequency and instructions per clock cycle (IPC) in this generation of the core, designers worked on timing and minimizing the gates between flops. The goal at the start of the project was to lower typical application power by 10%. Ultimately, **using a design methodology that included deployment of PowerPro® from Calypto®**, AMD was able to **lower the typical power by approximately 20% while increasing frequency at the given voltage by over 10%”** [4].

3.1 Overview of the Jaguar-based APU lines (12)

IPC improvements and power gating efficiency of the Jaguar core vs. the Bobcat core [4]

	Bobcat x86 IPC	Jaguar x86 IPC	Bobcat Core % Flops Active	Jaguar Core % Flops Active
Halt	0.00	0.00	8.2	1.2
AppTyp	0.95	1.10	10.3	7.7
Bobcat Virus	1.74	1.78	15.4	12.9
Jaguar Virus	0.81	1.86	14.3	15.0

Table: Comparison of IPC and clock-gating improvements [4]

Remark

IPC improvements were achieved also by manually optimizing the design for timing by using Monte Carlo simulation tools.

3.2 The Jaguar core

- 3.2.1 The microarchitecture of the Jaguar core
- 3.2.2 Main features of the Jaguar core

3.2.1 The microarchitecture of the Jaguar core

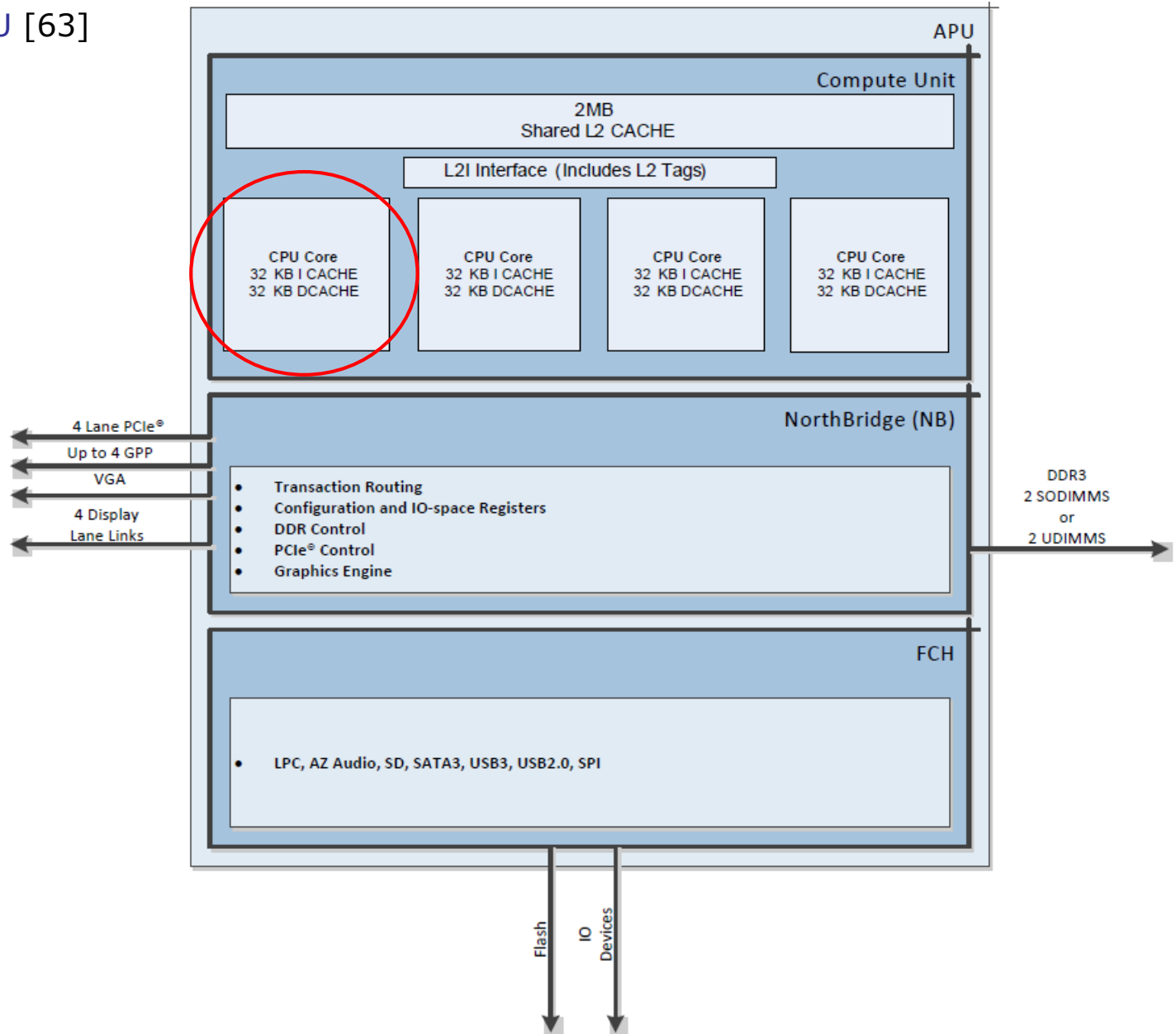
3.2.1 The microarchitecture of the Jaguar core (1)

3.2.1 The microarchitecture of the Jaguar core

The **Jaguar cores** are the key parts of the Compute Unit (x86 “engine”) of the APU, as indicated in the next slide.

3.2.1 The microarchitecture of the Jaguar core (2)

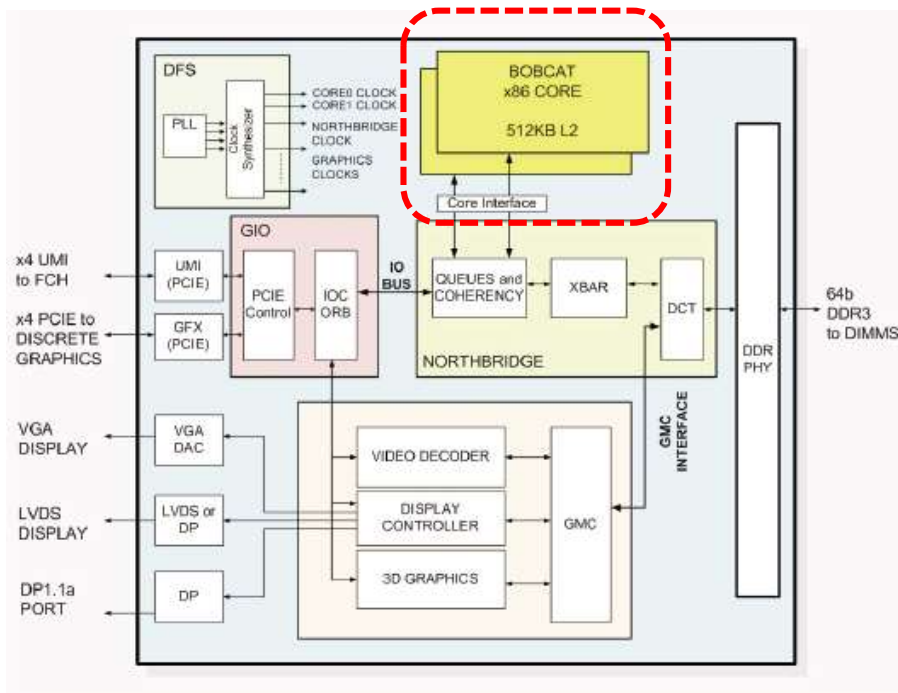
Block diagram of a Jaguar based APU [63]



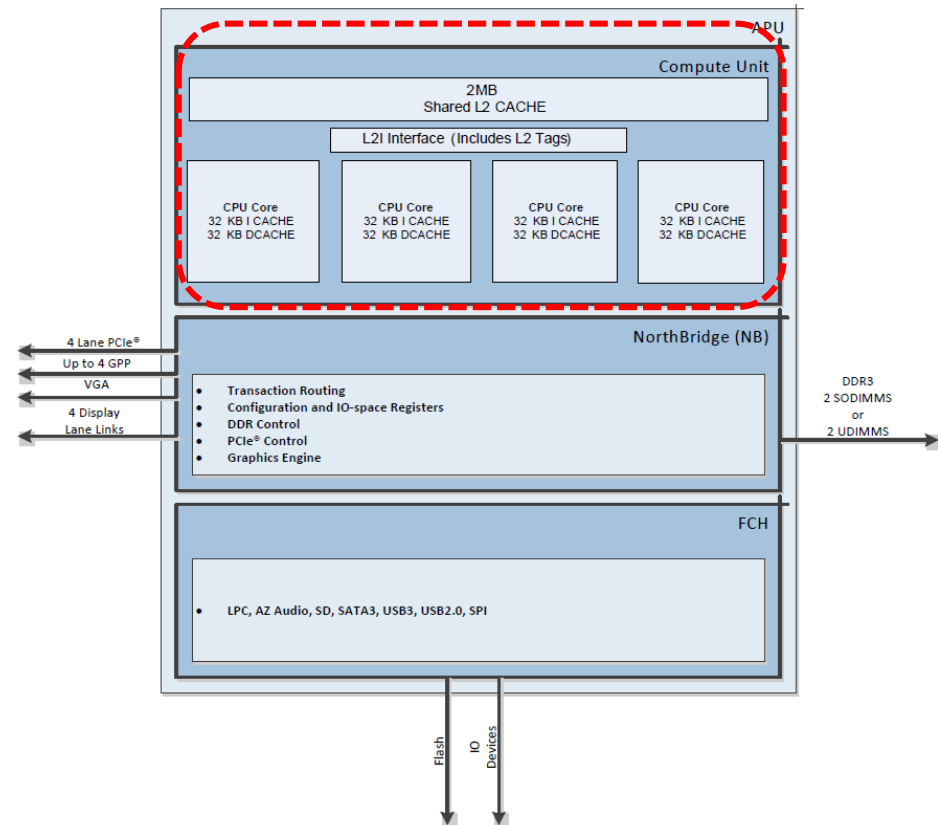
3.2.1 The microarchitecture of the Jaguar core (2b)

Key difference in the layout of the core complex in Bobcat and Jaguar based APUs [35], [64]

Bobcat based APU



Jaguar-based APU



Note that **Jaguar**-based APUs are based on **up to 4 cores** with a **shared (2 MB) L2 cache** whereas **Bobcat**-based APUs are based on **up to 2 cores** with **private 512 KB L2 caches**.

3.2.1 The microarchitecture of the Jaguar core (2c)

Block diagram of the Compute Unit (CU) of the Jaguar core [3]

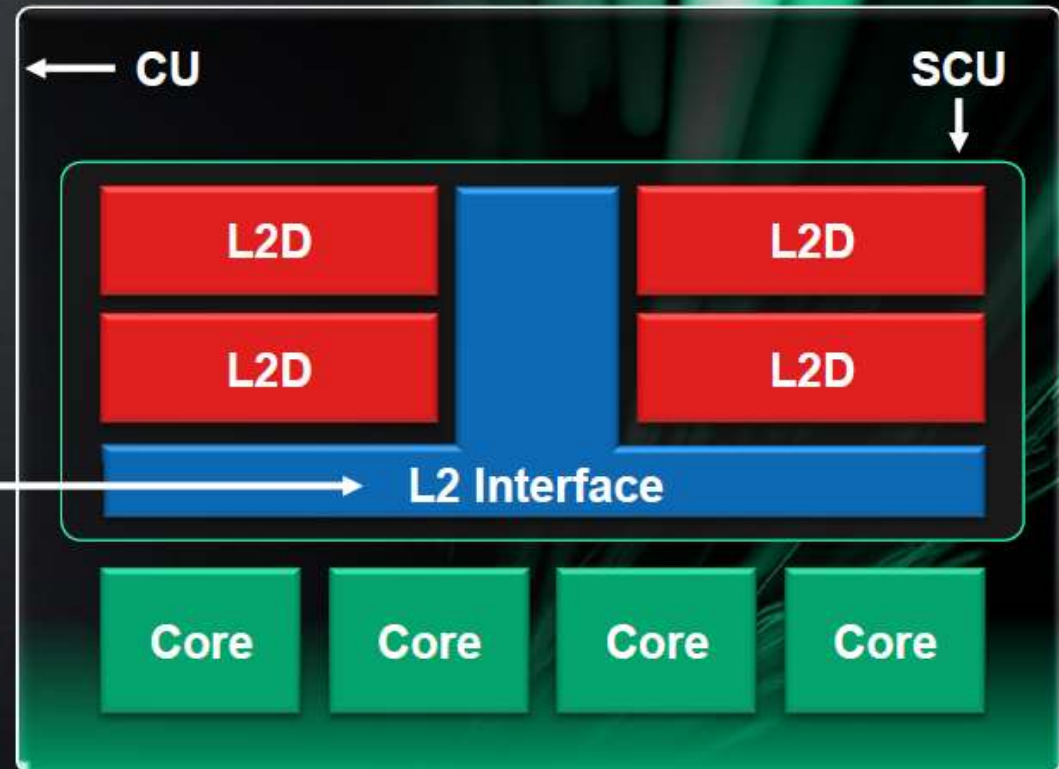
"JAGUAR" COMPUTE UNIT (CU)

- 4 Independent "Jaguar" cores
- Shared Cache Unit (SCU)
 - 4 L2 Data Banks (total 2MB)
 - L2 Interface Tile

To/from NB

The L2 databanks run at half-clock to save power and are clocked only when required [6].

The L2 interface runs at full speed.



Major ISA changes vs. the Bobcat core [63]

- Physical address extended to 40 bits (from 36 bits)
- Instruction set extensions
 - AVX
 - AES
 - SSE4.1, SSE4.2

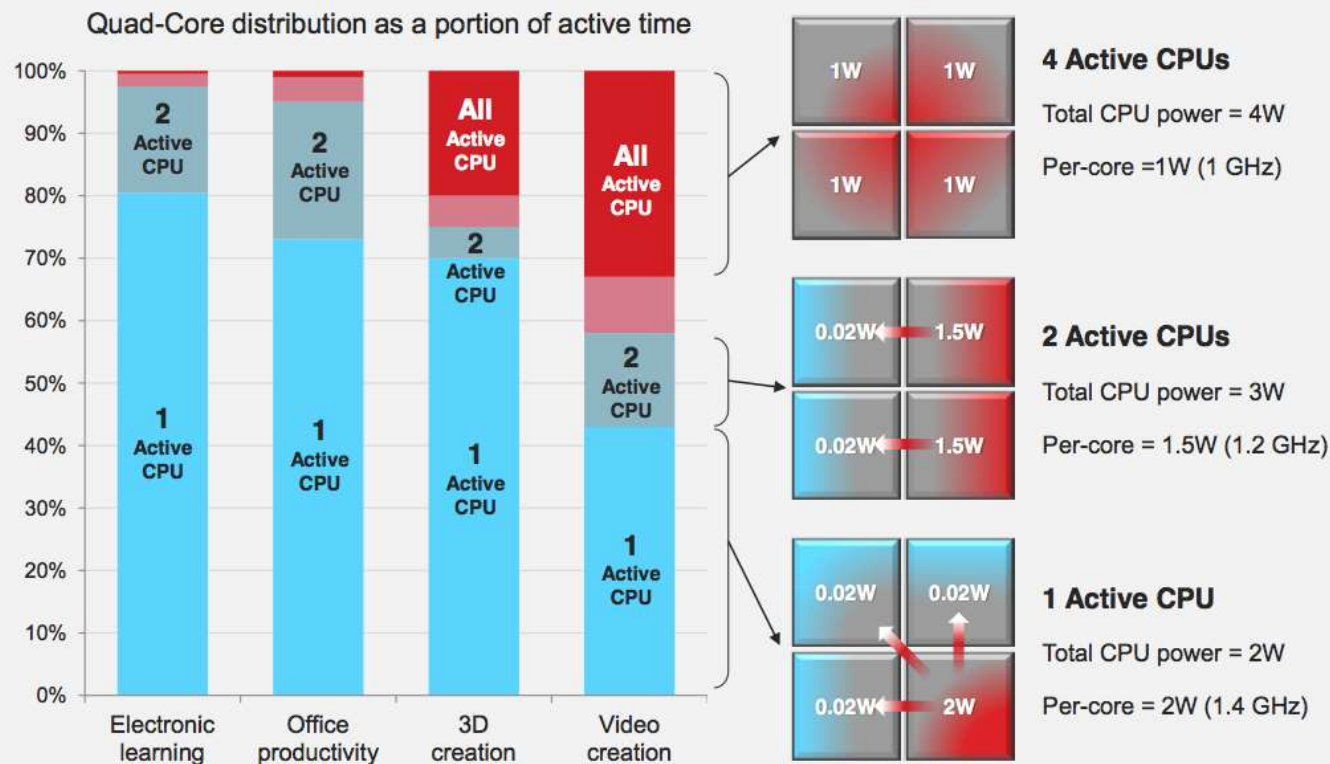
3.2.1 The microarchitecture of the Jaguar core (3)

Power consumption vs. quad-core utilization while running different applications [26]

QUAD-CORE UTILIZATION

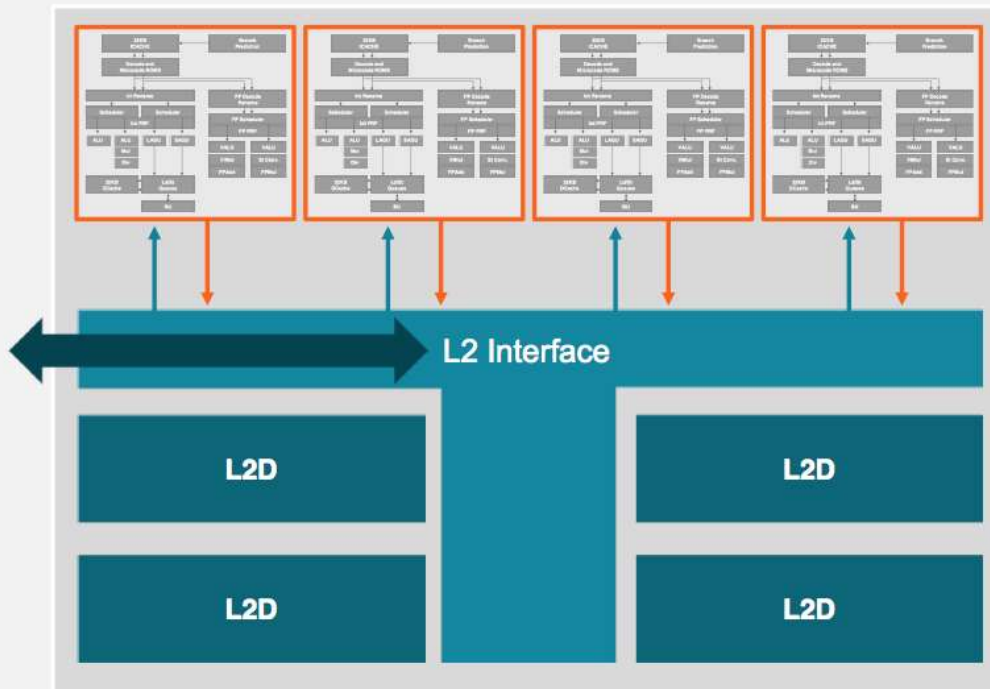


- ▶ If not all cores are being used, the unused power becomes available to the remaining cores
- ▶ Idle cores behave as thermal sinks to the active cores
- ▶ Power Density Multiplier (PDM) is applied to the TDP Limit of the active CPUs, based on the topology of the Idle CPUs and the ambient temperature
- ▶ Increases the CPU Thermal Headroom and lower thread count performance



3.2.1 The microarchitecture of the Jaguar core (4)

The shared L2 cache of Jaguar [26]

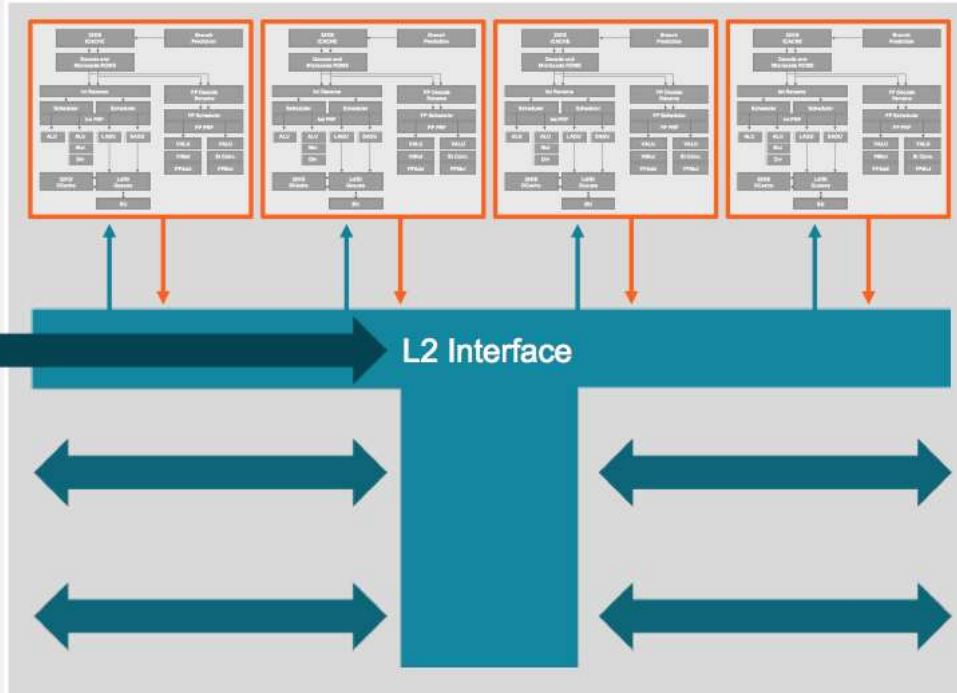


Shared Cache is major design addition in "Jaguar"

- ▶ Supports 4 cores
- ▶ Total shared 2MB, 16-way
 - ▶ Supported by 4 L2D banks of 512KB each
- ▶ L2 cache is inclusive – allows using L2 tags as probe filter
 - ▶ Any line in a Core L1 instruction or data cache must be in the L2

3.2.1 The microarchitecture of the Jaguar core (5)

The L2 cache interface of Jaguar [26]



- ▶ All connections routed thru L2 interface
- ▶ L2 tags reside in interface block
 - ▶ Divided into 4 banks
 - ▶ L2D bank lookup only after L2 tag hit
- ▶ L2 Interface block runs at core clock
 - ▶ L2D's run at half clock for power, only clocked when required
- ▶ New L2 stream prefetcher per core
 - ▶ Allows improved bandwidths & IPC
- ▶ Up to a total of 24 paired read + write transactions in flight
- ▶ 16 additional L2 snoop queue entries
 - ▶ Allows for handling coherent probes at high bandwidth

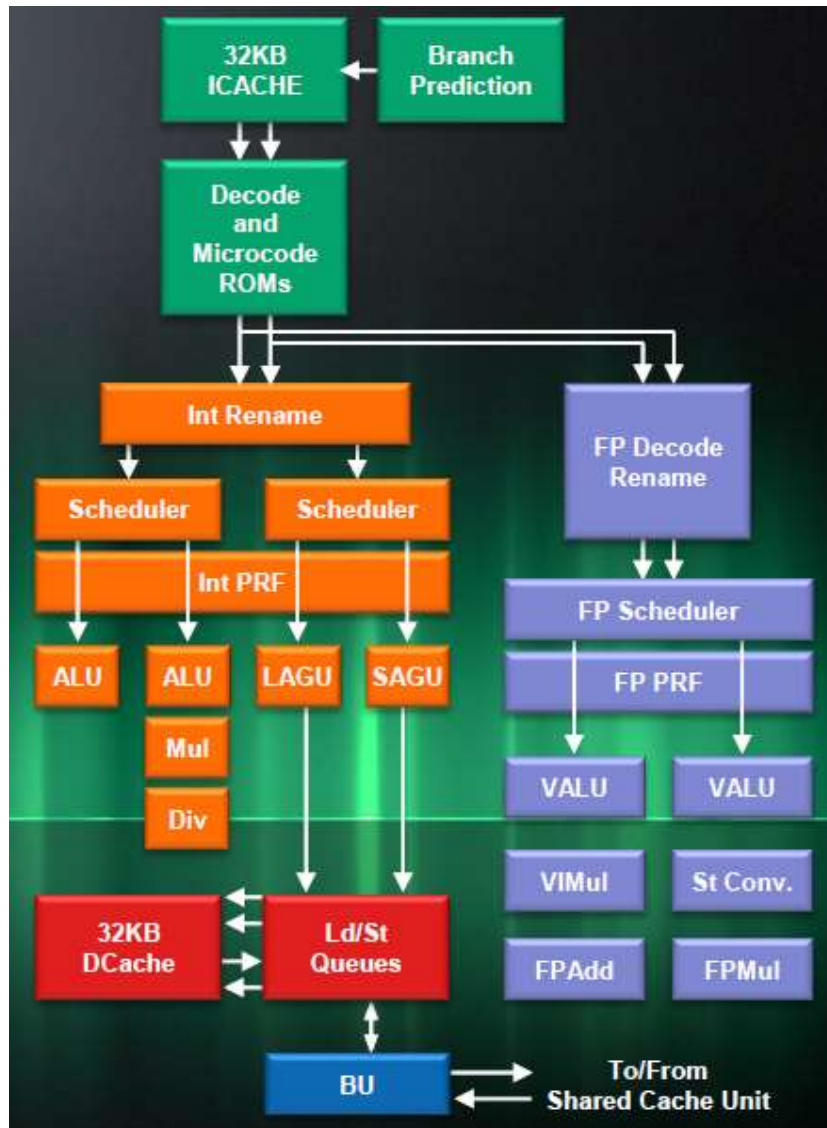
3.2.1 The microarchitecture of the Jaguar core (6)

Expected benefit of the shared L2 cache

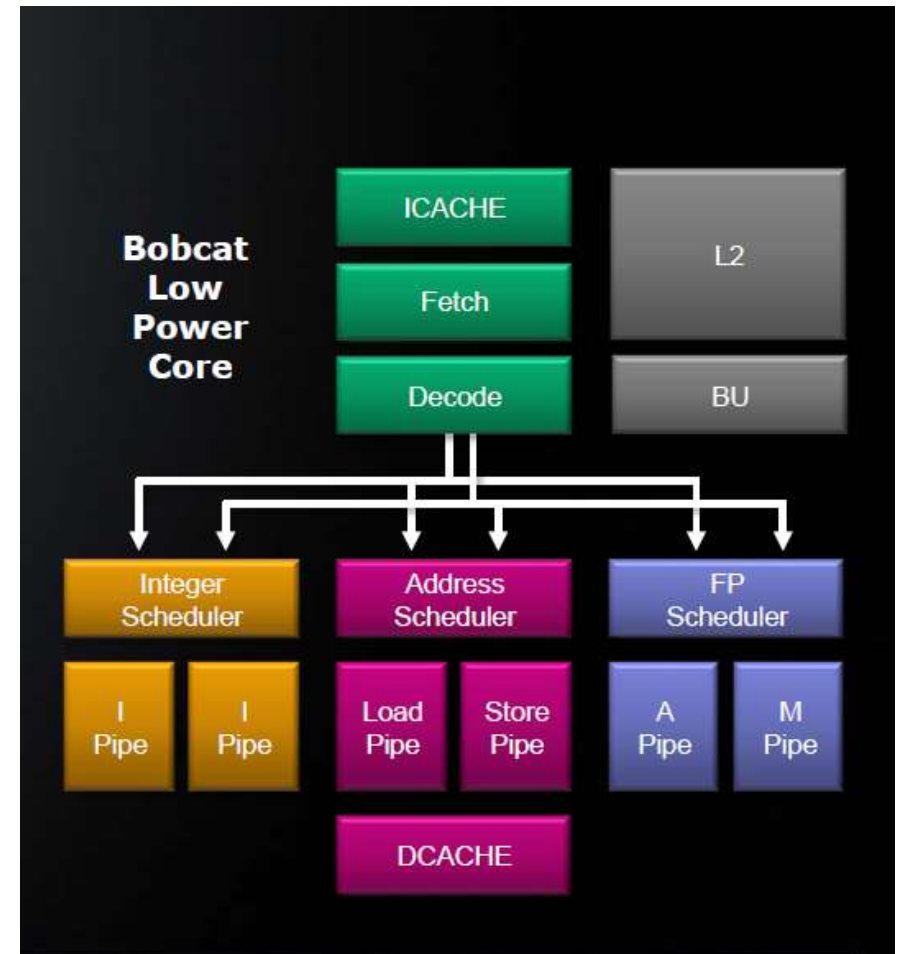
- The shared cache consists of **four 512 KB data banks** that are connected to the four cores via an L2 interface unit.
- The **L2 interface unit runs at full speed** whereas the **data banks at half speed** to save power.
- The **data banks are only clocked when required**.
- The shared design provides **more L2 cache space** for any core in a single threaded program and thus **reduces the rate of cache misses but needs a new L2 data prefetcher per core** [7].

3.2.1 The microarchitecture of the Jaguar core (7)

Comparing the microarchitecture of the Bobcat and Jaguar cores



Jaguar core [3]



Bobcat core [8]

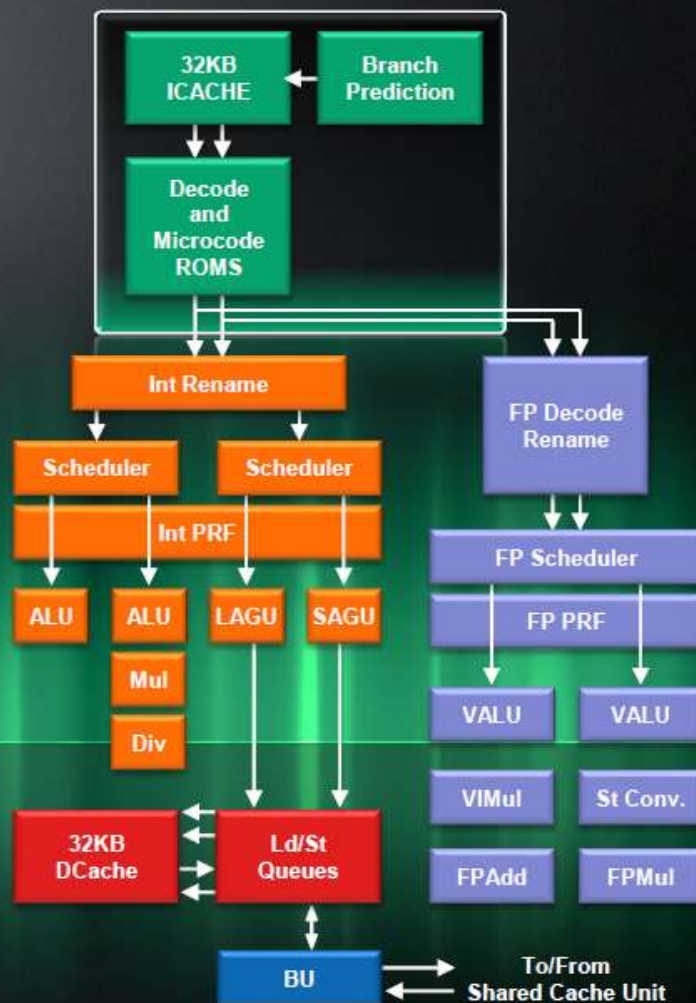
3.2.1 The microarchitecture of the Jaguar core (8)

The front-end part of the microarchitecture of the Jaguar core [3]

"JAGUAR" CORE Frontend

Like "Bobcat":

- IC: 32KB, 2way
- Itlb: 512 4KB pages
- Layered branch predictor w/ state of the art conditional predictor
- 32B fetch
- 2-instruction decode



"Jaguar" Enhancements:

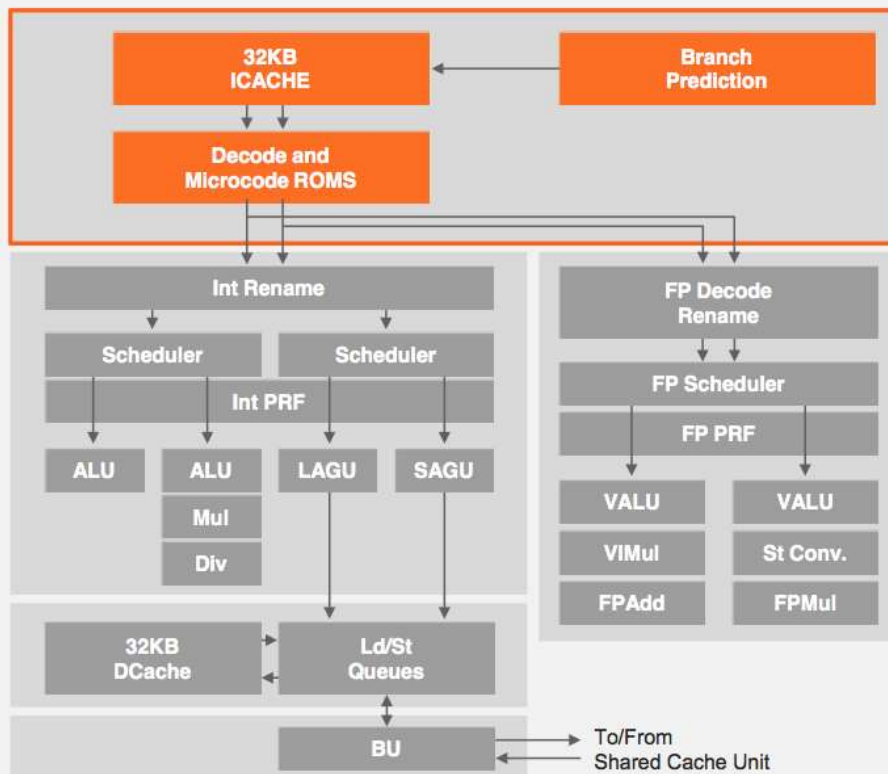
- 4x32B IC loop buffer for power
- Improved IC prefetcher for IPC
- Grew IB for improved fetch/decode decoupling
- Added decode stage for frequency

3.2.1 The microarchitecture of the Jaguar core (9)

Comparing the front-end parts of Jaguar and Bobcat [26]

LIKE "Bobcat":

- ▶ IC: 32KB, 2way
- ▶ Itlb: 512 4KB pages
- ▶ Layered branch predictor w/ state of the art conditional predictor
- ▶ 32B fetch
- ▶ 2-instruction decode



"Jaguar" ENHANCEMENTS:

- ▶ 4x32B IC loop buffer for power
- ▶ Improved IC prefetcher for IPC
- ▶ Grew IB for improved fetch/decode decoupling
- ▶ Added decode stage for frequency

3.2.1 The microarchitecture of the Jaguar core (10)

Loop buffer [7], [26]

- One front-end improvement is the addition of a 4 element (4x 32 byte) loop buffer.
- Whenever a loop is detected instructions are fetched from the loop buffer rather than from the L1 cache.

Nevertheless, it is not a trace cache, like the one used in Intel's Pentium 4.

With the loop buffer the fetch/decode unit will not be shut down during subsequent iterations of the loop.

Using the loop buffer saves power but does not increase performance.

Remark

Using loop buffers to improve IPC or reduce power consumption of instruction fetching is not a new idea.

Different implementations were already used e.g. in Cray computers or in the Pentium M or Nehalem processors.

There are also numerous patents concerning loop buffers, see e.g. the US patent application 11/272,718 with a large number of references.

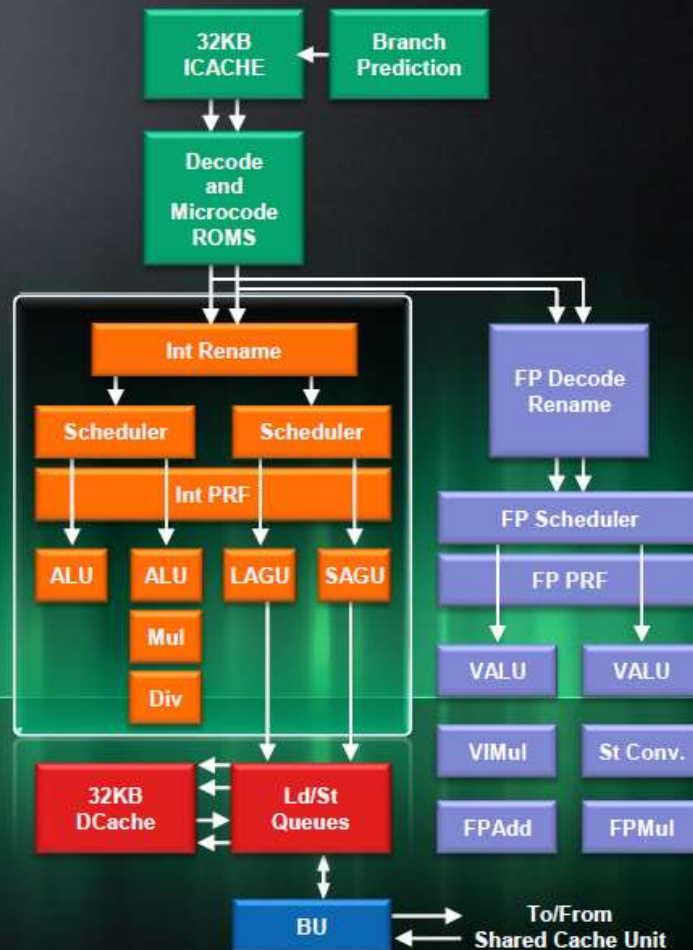
3.2.1 The microarchitecture of the Jaguar core (11)

Integer execution in the Jaguar core [3]

"JAGUAR" CORE Integer Execution

Like "Bobcat":
Schedulers can issue

- 2 ALU
- 1 LD AGU
- 1 ST AGU



"Jaguar" Enhancements:

- New hardware divider (leveraged from Llano)
- New/improved cops: CRC32/SSE4.2, BMI1, POPCNT, LZCNT
- More OOO resources
Larger schedulers, ROB

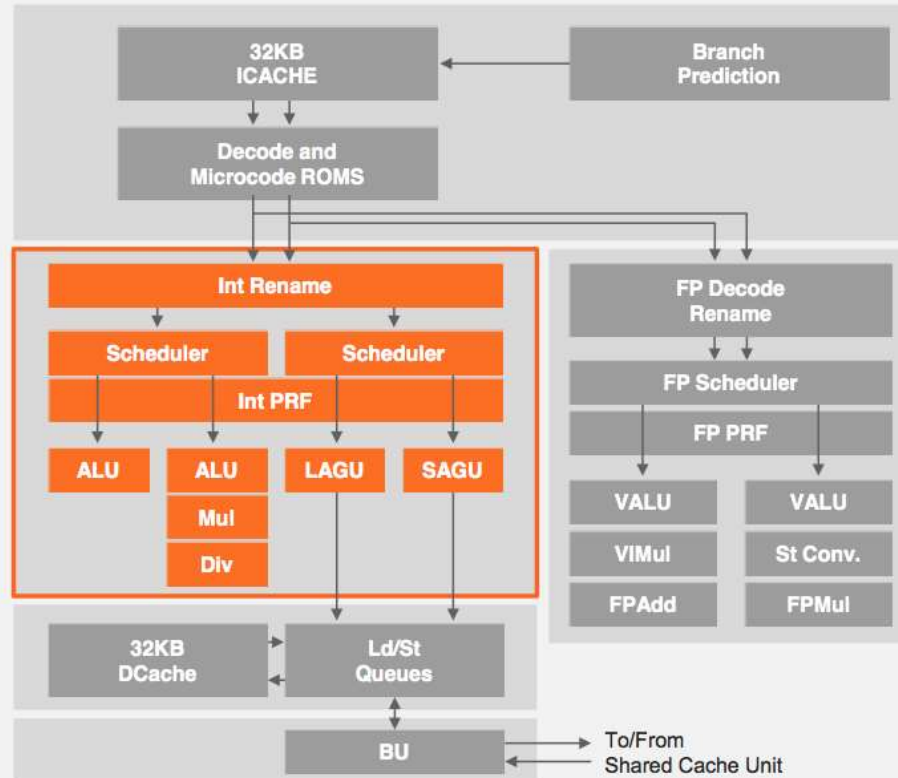
cops: Complex operations

3.2.1 The microarchitecture of the Jaguar core (12)

Comparing the integer execution units of Jaguar and Bobcat [26]

LIKE "Bobcat":

- ▶ Schedulers can issue
 - ▶ 2 ALU
 - ▶ 1 LD AGU
 - ▶ 1 ST AGU



"Jaguar"

ENHANCEMENTS:

- ▶ New hardware divider (leveraged from Llano)
- ▶ New/improved cops: CRC32/SSE4.2, BMI1, POPCNT, LZCNT
- ▶ More OOO resources
- ▶ Larger schedulers, ROB

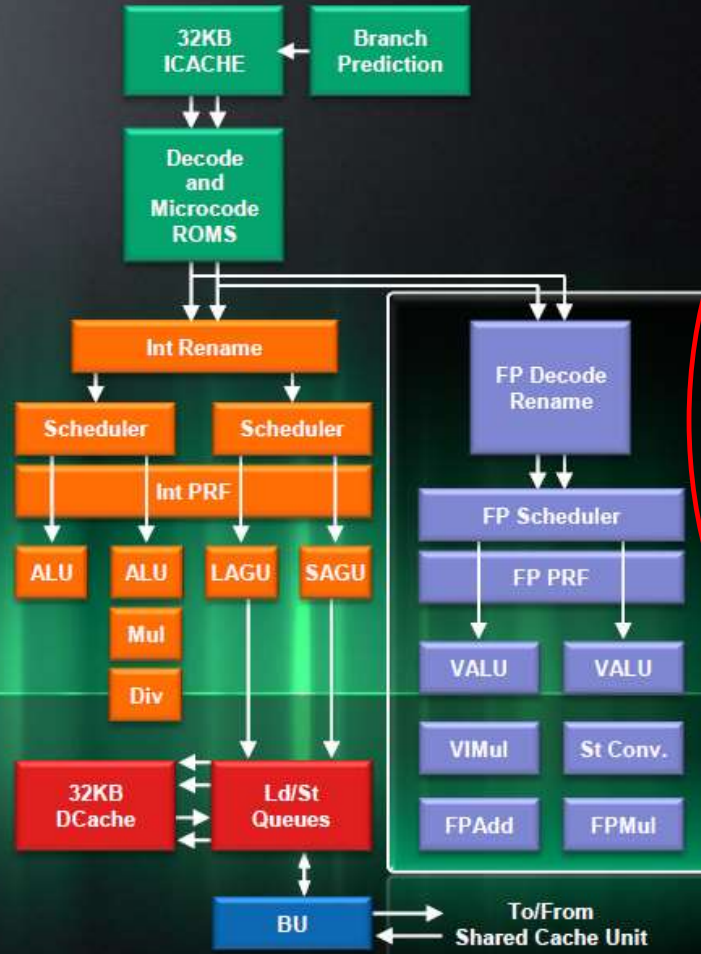
3.2.1 The microarchitecture of the Jaguar core (13)

FP execution in the Jaguar core [3]

"JAGUAR" CORE Floating Point Unit

Like "Bobcat":

- 2 wide FP decode
- OOO scheduler
- 2 execution pipes



"Jaguar" Enhancements:

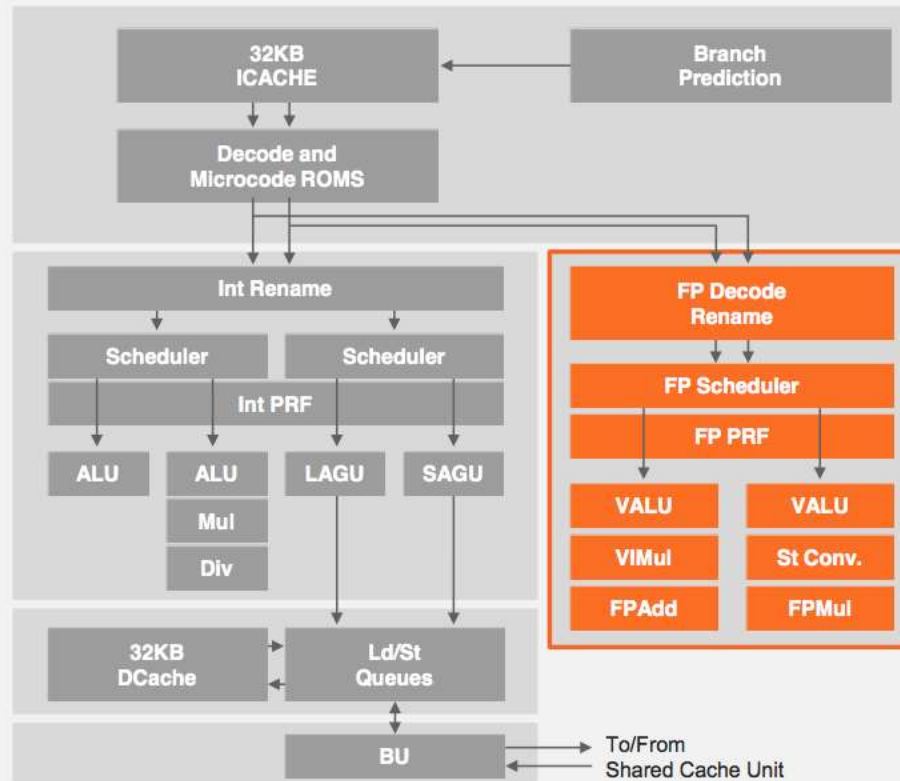
- 128b native hardware
 - 4 SP muls + 4 SP adds
 - 1 DP mul + 2 DP adds
- ISA: many new COPs
 - 256b AVX supported by double pumping 128b hardware
- New Zero Optimizations
- Second FPRF stage for frequency

3.2.1 The microarchitecture of the Jaguar core (14)

Comparing the floating point units of Jaguar and Bobcat [26]

LIKE "Bobcat":

- ▶ 2 wide FP decode
- ▶ OOO scheduler
- ▶ 2 execution pipes



"Jaguar" ENHANCEMENTS:

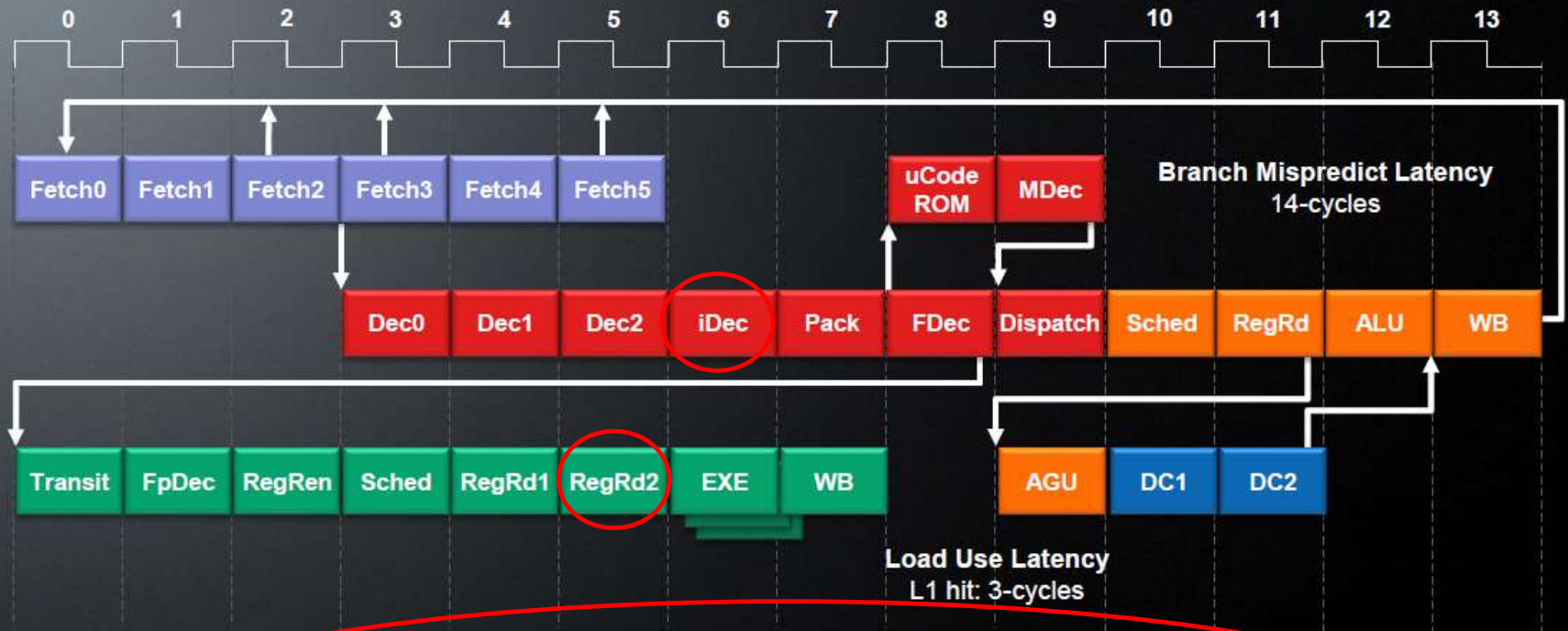
- ▶ 128b native hardware
 - ▶ 4 SP muls + 4 SP adds
 - ▶ 1 DP mul + 2 DP adds
- ▶ ISA: many new COPs
 - ▶ 256b AVX supported by double pumping 128b hardware
- ▶ New Zero Optimizations
- ▶ Second FPRF stage for frequency

3.2.1 The microarchitecture of the Jaguar core (15)

The core pipeline of Jaguar [3]

Two added stages (additional decode stage (iDec) and FP Reg. read stage (RegRd2)) to raise fc.

"JAGUAR" CORE PIPELINE

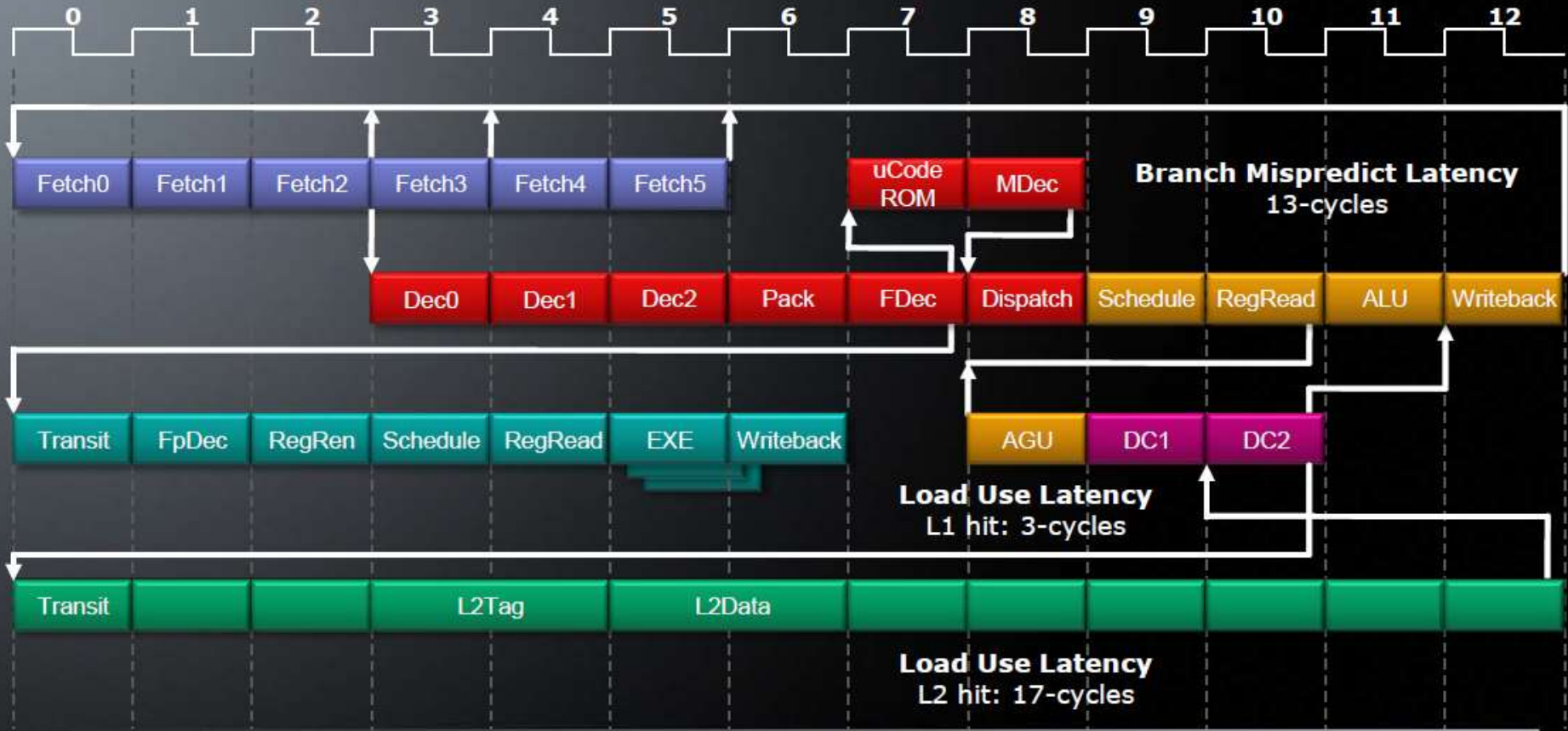


Microarchitectural Frequency improvement over "Bobcat": >10%
One additional cycle branch mispredict latency vs. "Bobcat"

3.2.1 The microarchitecture of the Jaguar core (16)

The core pipeline of Bobcat as comparison [8]

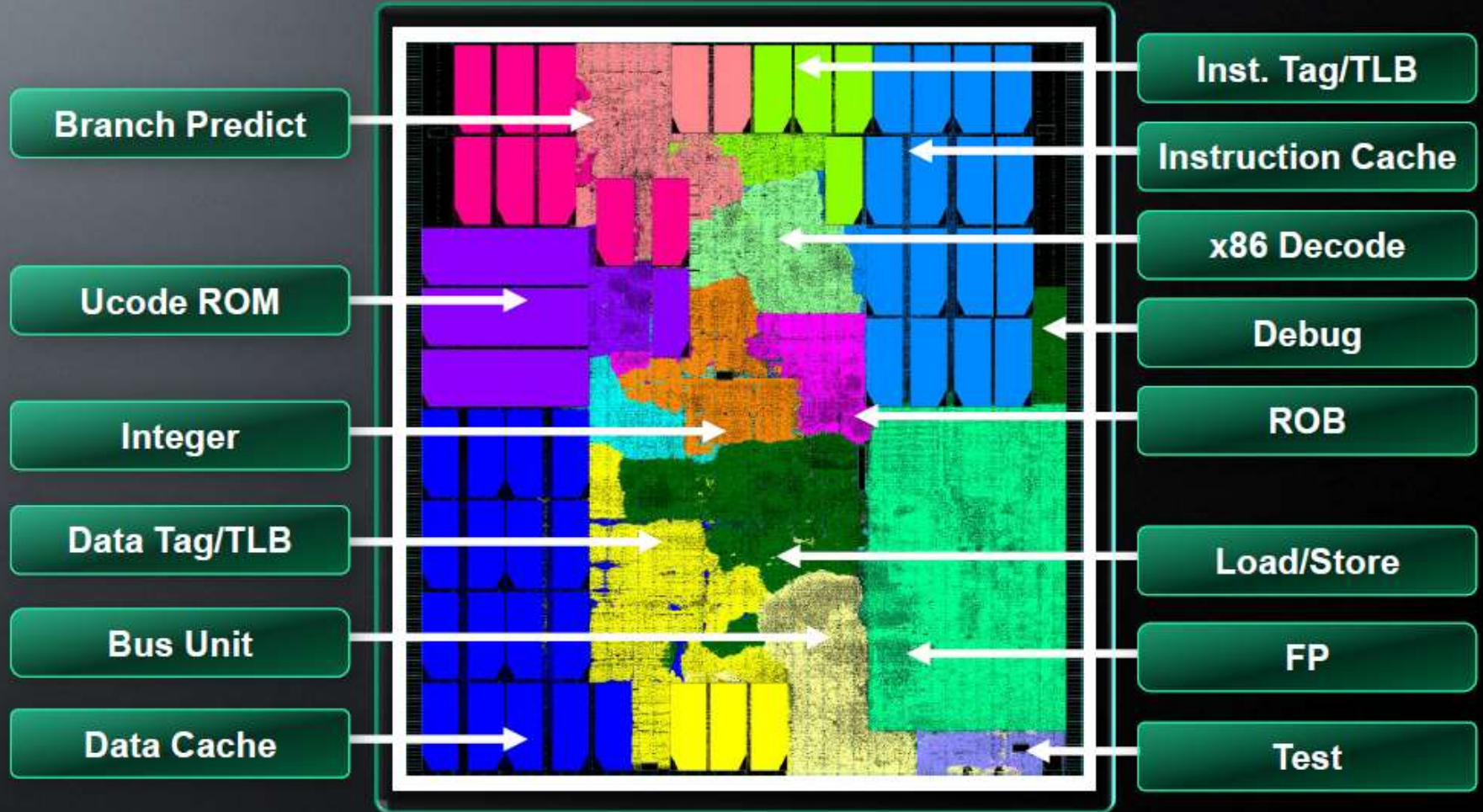
Bobcat Pipeline



3.2.1 The microarchitecture of the Jaguar core (17)

The core floor plan of Jaguar [3]

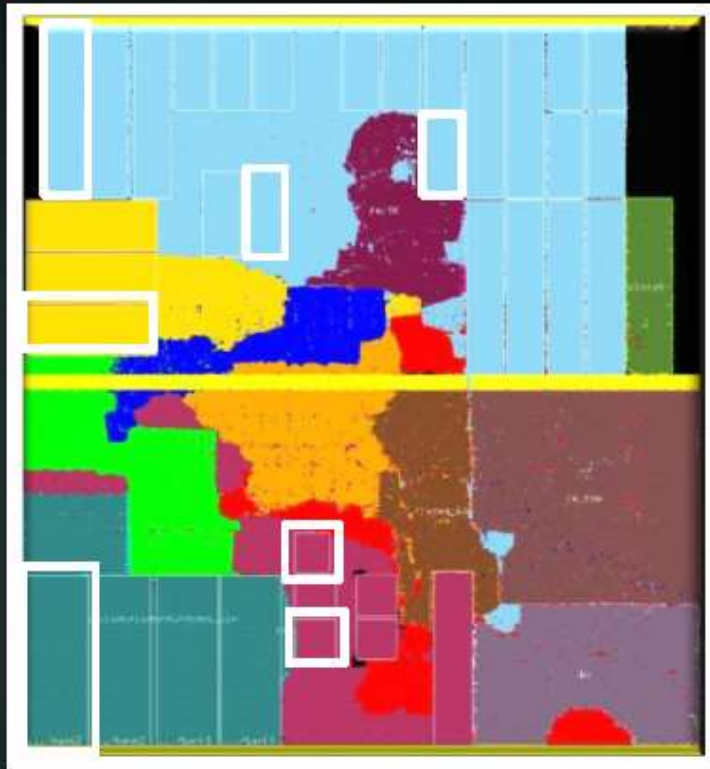
"JAGUAR" CORE FLOOR PLAN



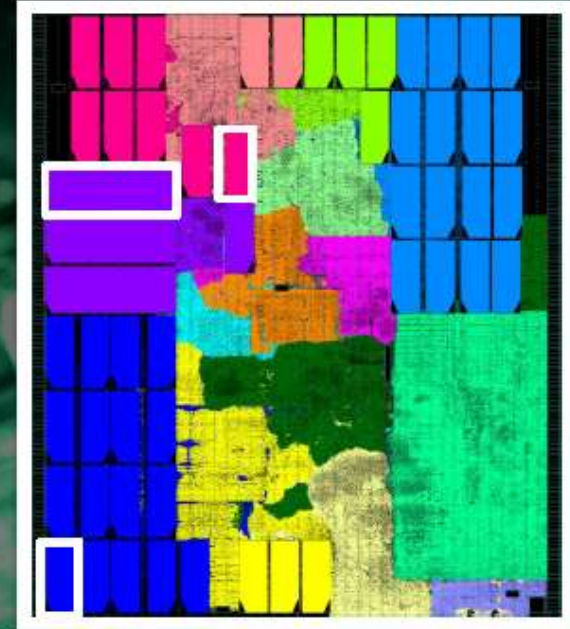
3.2.1 The microarchitecture of the Jaguar core (18)

Contrasting the core floor plans of Bobcat and Jaguar [3]

CORE FLOOR PLAN COMPARISON



“Bobcat” core in 40nm = 4.9 mm²
7 core macros, 2 L2 macros,
3 clock macros



“Jaguar” core in 28nm = 3.1 mm²
3 core macros, 1 L2 macro,
1 clock macro

3.2.2 Main features of the Jaguar core

3.2.2 Main features of the Jaguar core (1)

3.2.2 Main features of the Jaguar core compared with the Bobcat core [9]

Feature	"Bobcat"	"Jaguar"	User Benefit
Core Frequency	1.4 GHz/1.7 GHz	>10%	Improved CPU performance
Instructions per clock	"90% of mainstream"	>15%	Improved CPU performance
Core Count	2	4	More performance for highly threaded apps
L2 Cache	512KB per core	2MB Shared	More performance for less threaded apps
Power efficiency	Core C6 power gating	Enhanced core C6 power gating	Better battery life
Instruction Sets	AMD64, SSE1-SSE3, SSSE3, SSE4a	Bobcat + SSE4.1, 4.2, AES/CLMUL, MOVBE, AVX, F16C, BMI1	Improved performance/power when applications use newer instructions
Physical address capability	36-bit	40-bit	Memory capacity scale-up
Out of Order (OOO) Execution	Yes	Yes	More performance than In-Order designs
Machine Width	2-wide	2-wide	Power efficient design point
Floating Point Unit	64-bit data path	128-bit data path	Better media experience

3.2.2 Main features of the Jaguar core (2)

Expected benefit of the shared L2 cache [7]

- In the previous design each Bobcat core has a 512KB private L2 cache, clocked at ½ CPU speed.
- With Jaguar, AMD has opted to attach a single shared (up to 2 MB) L2 cache to the CPUs (providing still 512 KB per core).
- This cache pool is connected via an L2 interface unit, running at full processor speed, while the L2 cache itself still runs at 50% core clock.

3.2.2 Main features of the Jaguar core (3)

The Core C6 state (CC6 state)/Package C6 state (PC6 state) of Jaguar (simplified) [54]

Entering the CC6 state

1. OS requests entering into the CC6 state by issuing a specific I/O read or HLT instruction.
2. The processor enters the CC6 state if associated monitors allow this.

The process of entering the CC6 state and power gating

Due to using a shared L2 cache the process of entering the CC6 state has changed, as follows:

1. Internal core state is saved to the L1 cache or to DRAM depending to internal settings.
2. L1 cache is flushed to the shared L2 cache by microcode.
3. Power is removed from the core and the Core PLL is powered down.

Exiting the Core C6 state (CC6 state)

There is a set of events, such as interrupts, which cause a core to exit the CC6 state.

Entering the Package C6 state (PC6 state)

- If all cores entered the CC6 state and a transition to the PC6 state is enabled (by monitors), the processor enters the PC6 state.
- The last core entering the CC6 state let flush L2 to DRAM by microcode.
- In the PC6 state VDD can be reduced to a non-operational voltage that does not retain core state but allows to reduce static and dynamic dissipation.

Exciting from the Package C6 state (PC6 state)

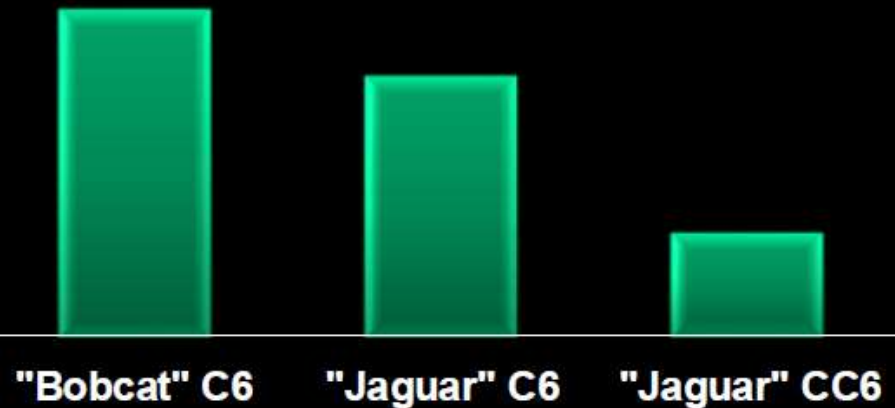
If one of the cores leaves the CC6 state the processor excites the PC6 state.

Improved C6/CC6 latencies of the Jaguar APU [3]

"JAGUAR" C6

- Any Core can independently go into CC6 power gating
 - Optimized microcode routines and hardware allow for fast CC6 entry/exit
 - Shared L2 leaves more cache for the remaining active cores (IPC)
- Last core in the compute unit to be power gated flushes shared L2 in preparation for full C6. Hardware engines added to improve L2 flush times.

Relative C6 Latencies Under Normalized Conditions



3.3 Jaguar-based APU lines

- 3.3.1 Overview of the Jaguar-based APU lines
- 3.3.2 The Kyoto Opteron X microserver line
- 3.3.3 The Kabini notebook APU line
- 3.3.4 The Temash tablet APU line

3.3.1 Overview of the Jaguar-based APU lines

3.3.1 Overview of the Jaguar-based APU lines (1)

3.3.1 Overview of the Jaguar-based APU lines

Jaguar-based APU lines

```
graph TD; Root[Jaguar-based APU lines] --- Branch1[ ]; Root --- Branch2[ ]; Root --- Branch3[ ]; Branch1 --- Opteron[The Opteron X (Kyoto) microserver line]; Branch2 --- Kabini[The Kabini notebook APU line]; Branch3 --- Temash[The Temash tablet APU line];
```

The Opteron X (Kyoto) microserver line

X2150 GPU/X1150 CPU

4 Jaguar cores

X1150: no GPU

X2150: HD 8000 Series GCN
(Graphics Core Next) GPU

9-27 W

SOC

FT3 BGA package (769 balls)

5/2013

First quad-core and second microserver line at all (following Intel's dual-core Atom S1200 series) for web and cloud applications.

The Kabini notebook APU line

A6-5xxx/E2-3xxx/E1-1xxx Series

A6 Series: 4 Jaguar cores/

E2, E1 Series: 2 Jaguar cores

HD 8000 Series GCN
(Graphics Core Next) GPU

25/15/9 W

SOC

FT3 BGA package (769 balls)

5/2013

First quad-core x86 SoC for entry-level and small-form factor touch notebooks [55].

The Temash tablet APU line

Elite Mobility A6-1xxx/A4-1xxx Series

A6 Series: 4 Jaguar cores

A4 Series: 2 Jaguar cores

HD 8000 Series GCN
(Graphics Core Next GPU

Windows 8 based

3.9/8/9 W (undocked)

15 W docked

SOC

FT3 BGA package (769 balls)

5/2013

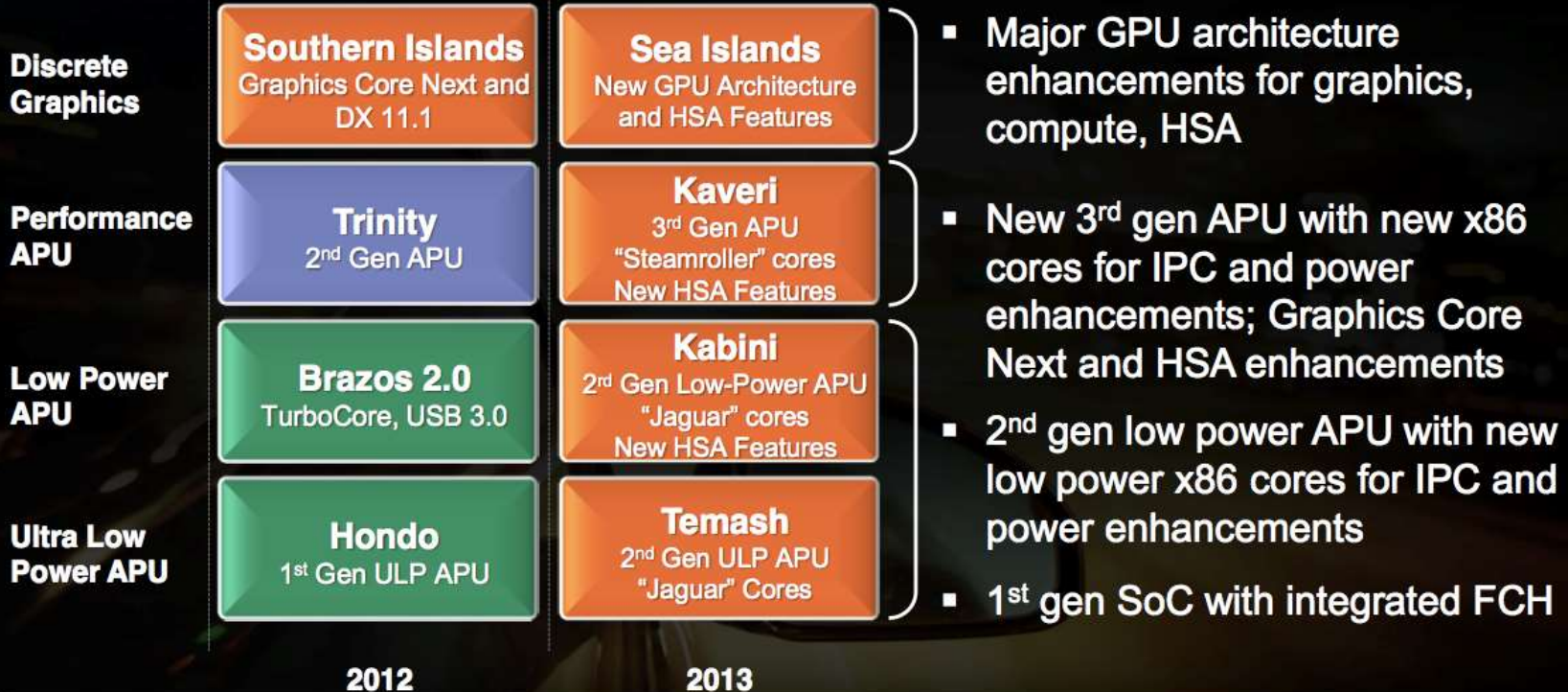
First 28nm, quad-core x86 SoC APU designed for touch small form-factor notebooks, tablets, and hybrids 13-inches and below [55].

3.3.1 Overview of the Jaguar-based APU lines (2)

The Kabini notebook and Temash tablet processors on AMD's roadmap for 2013 [65]

CLIENT AND GRAPHICS ROADMAP

40nm 32nm 28nm



INDUSTRY-LEADING GRAPHICS, COMPUTE IP RAPIDLY LEVERAGED IN LOW POWER PLATFORMS VIA APUs



3.3.2 The Opteron X (Kyoto) microserver line

3.3.2 Opteron X (Kyoto) microserver line (1)

3.3.2 Opteron X (Kyoto) microserver line

Jaguar-based APU lines

The Opteron X (Kyoto) microserver line

X2150 GPU/X1150 CPU

4 Jaguar cores

X1150: no GPU

X2150: HD 8000 Series GCN
(Graphics Core Next) GPU

9-27 W

SOC

FT3 BGA package (769 balls)

5/2013

The Kabini notebook APU line

A6-5xxx/E2-3xxx/E1-1xxx Series

A6 Series: 4 Jaguar cores/

E2, E1 Series: 2 Jaguar cores

HD 8000 Series GCN
(Graphics Core Next) GPU

25/15/9 W

SOC

FT3 BGA package (769 balls)

5/2013

The Temash tablet APU line

Elite Mobility A6-1xxx/A4-1xxx Series

A6 Series: 4 Jaguar cores

A4 Series: 2 Jaguar cores

HD 8000 Series GCN
(Graphics Core Next GPU

Windows 8 based

3.9/8/9 W (undocked)

15 W docked

SOC

FT3 BGA package (769 balls)

5/2013

3.3.2 Opteron X (Kyoto) microserver line (2)

Key features of the Opteron X (Kyoto) X models [56]

AMD Kyoto Offerings						
	CPU Cores	CPU Configurable Frequency	GPU Cores	GPU Configurable Frequency	TDP Range	1Ku Pricing
Opteron X1150	4	Up to 2.0GHz	-	-	9 - 17W	\$64
Opteron X2150	4	Up to 1.9GHz	128	266 - 600MHz	11 - 22W	\$99

Socket: FT3 BGA

3.3.2 Opteron X (Kyoto) microserver line (3)

Comparing key features of the AMD's Opteron X and Intel's Atom S1200 lines [56]

AMD OPTERON™ X-SERIES OUTPERFORMS INTEL® ATOM™ S1200 SERIES ACROSS ALL KEY PERFORMANCE METRICS

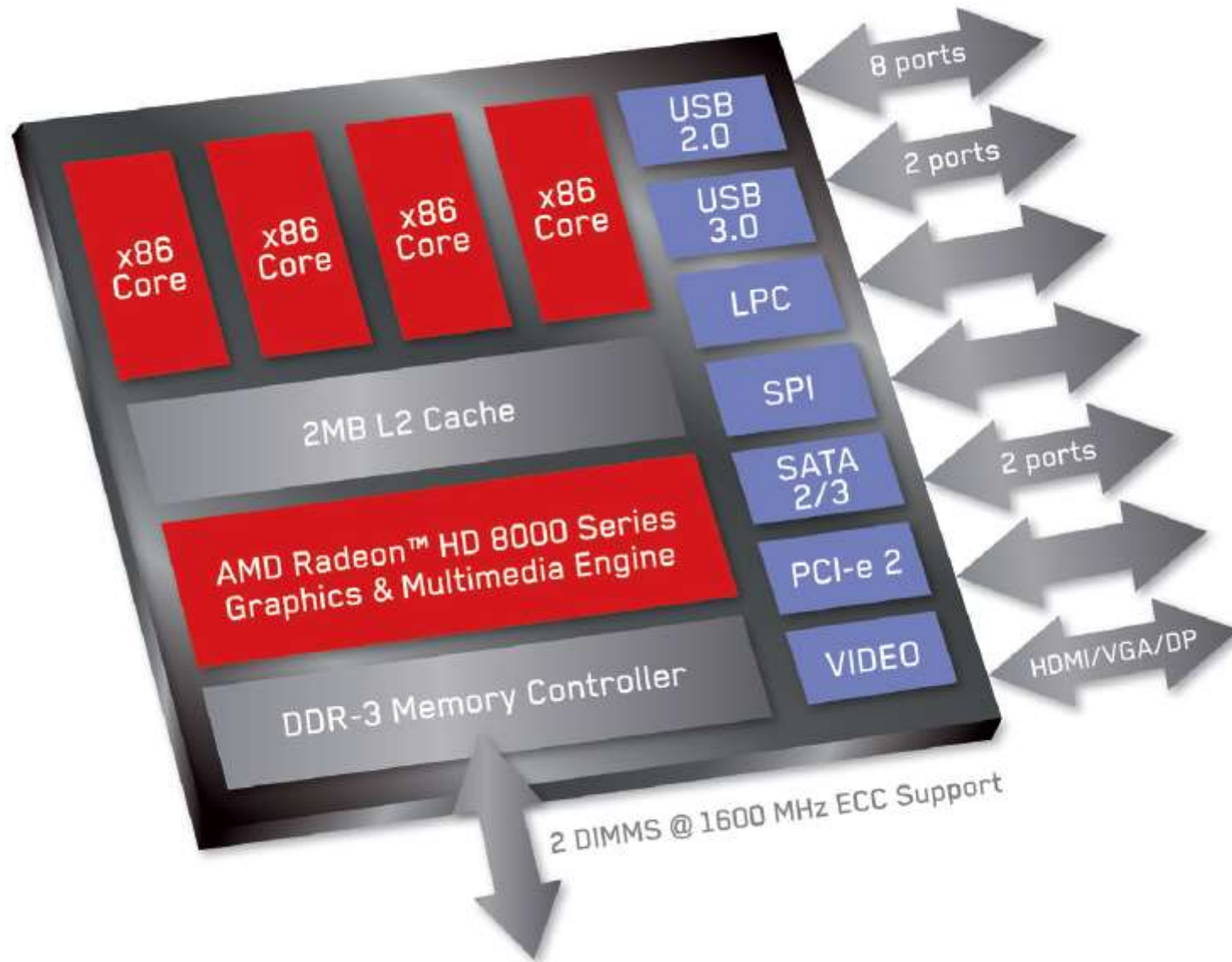


	AMD Opteron X-Series	Intel Atom S1200 Series	AMD ADVANTAGE
x86 CPU Cores	4	2	2X
x86 CPU Threads	4	4	
GPU Cores*	128 AMD Radeon™ 8000 Cores	None	AMD Only
Max. DRAM per Socket	32 GB**	8 GB	4X
Max. DRAM Speed	DDR3-1600	DDR3-1333	1.2X
L2 Cache	2 MB	1 MB	2X
Throughput Performance (est.) ²	28.9 @ 2 GHz (CPU)	13.0 @ 2GHz	2.2X
Single Thread Performance (est.) ²	10.0 @ 2 GHz (CPU)	5.2 @ 2 GHz	1.9X
Integrated SATA Ports	Yes	No	AMD Only

* X-Series APU only; **Based on the capability of the Kyoto memory controller and expected 16GB DIMM availability.

3.3.2 Opteron X (Kyoto) microserver line (4)

Block diagram of the Opteron X2150 APU [57]



3.3.2 Opteron X (Kyoto) microserver line (5)

Overview of the Opteron-X (Kyoto) series processors [58]

Compute

- ▶ 4 "Jaguar" 64-bit x86 cores
- ▶ 128 AMD Radeon™ HD 8000 cores (x2150 APU only)
 - Video decode offload
 - Video compression offload

Memory

- ▶ 64-bit DDR3 w/ECC
- ▶ SODIMM & UDIMM
- ▶ Up to 1600 GT/s
- ▶ Up to 2 DIMMs

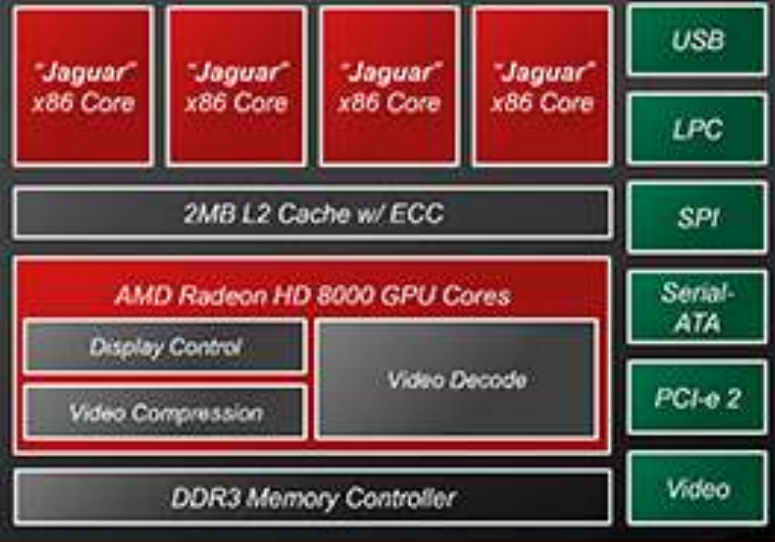
Integrated I/O

- ▶ PCI-e® Gen 2
- ▶ USB 2.0 / 3.0
- ▶ Video
- ▶ Serial-ATA 2.x / 3.x
- ▶ 8 lanes
- ▶ 8 ports / 2 ports
- ▶ DisplayPort, VGA, HDMI®
- ▶ 2 ports

X2150 APU - as low as **11W**

X1150 CPU - as low as **9W**

BGA
Package
(24.5 x 24.5)

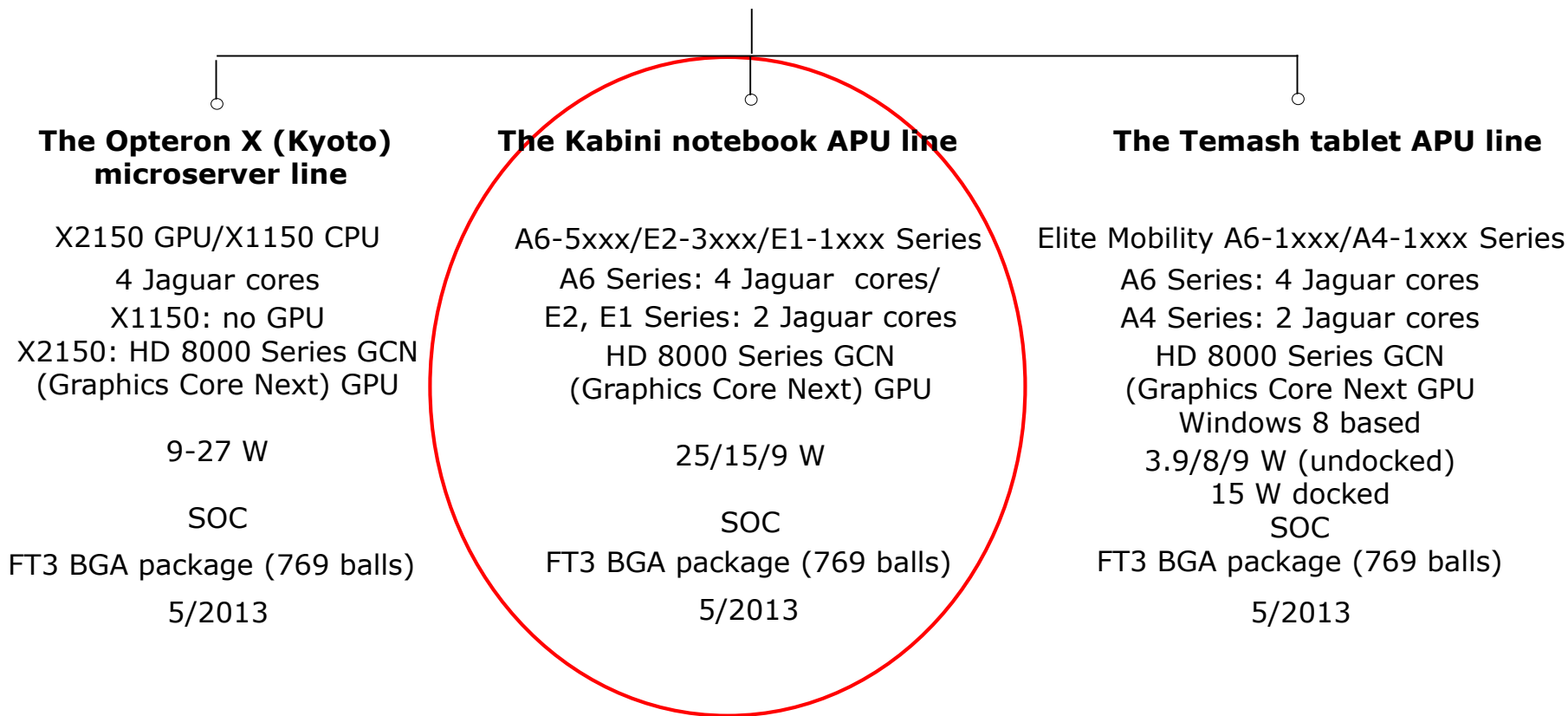


3.3.3 The Kabini notebook APU line

3.3.3 The Kabini notebook APU line (1)

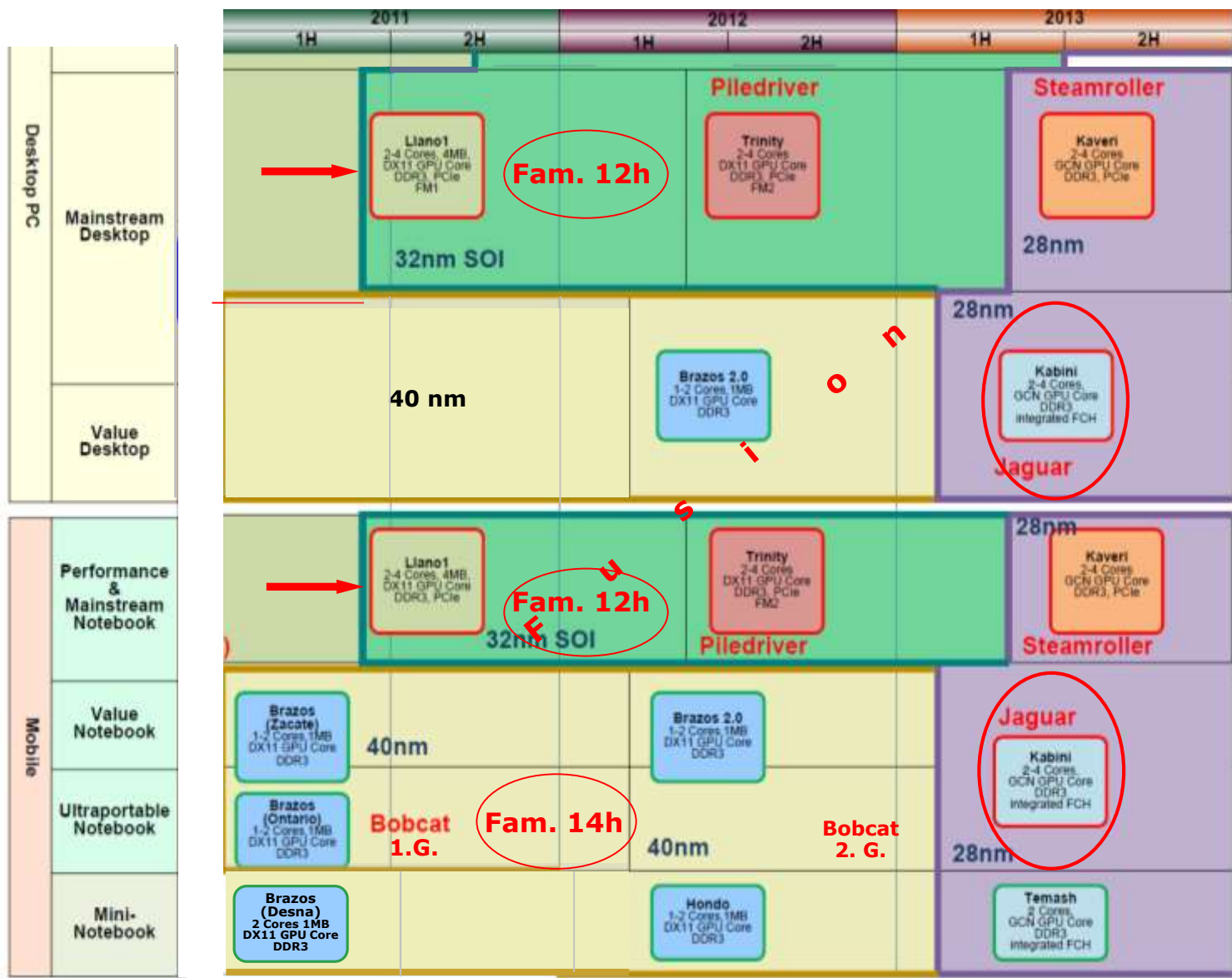
3.3.3 The Kabini notebook line

Jaguar-based APU lines



3.3.3 The Kabini notebook APU line (2)

3.3.3 Positioning the Kabini notebook APU line -1 [based on 14]



3.3.3 The Kabini notebook APU line (3)

Positioning the Kabini notebook APU line -2 [2]

AMD 2013 Client Roadmap

Performance	AMD 2 nd Generation A-Series APU codename "Trinity"	AMD 2 nd Generation A-Series APUs codename "Richland" Desktop, Standard notebook (35W) and Low Voltage (17-25W) 2-4 "Piledriver" CPU cores 2 nd Generation DirectX®11 GPU	"Kaveri" 3 rd Gen A-Series APUs 2-4 "Steamroller" CPU Cores Graphics Core Next (GCN) GPU HSA Application Support
Mainstream			
Low-Power Essential	AMD C-Series and E-Series APUs codename "Brazos 2.0" Low Voltage (9-18W) 2 "Bobcat" CPU Cores DirectX®11 capable GPU		"Kabini" A-Series and E-Series APUs Complete SoC Low Voltage (9-15W) 2-4 "Jaguar" CPU cores Graphics Core Next (GCN) GPU
Ultra-Low Power Tablet/Fanless	AMD Z-Series APU codename "Hondo" 1-2 "Bobcat" CPU Cores, Ultra Low Voltage (4.5W), DirectX®11 capable GPU		"Temash" A-Series Elite Mobility APUs Ultra Low Voltage; Complete SoC; 2-4 "Jaguar" CPU Cores Graphics Core Next (GCN) GPU

AMD roadmaps are subject to change without notice

40nm 32nm 28nm



January 7, 2013

3.3.3 The Kabini notebook APU line (4)

Main features of Kabini notebook APU models [59]

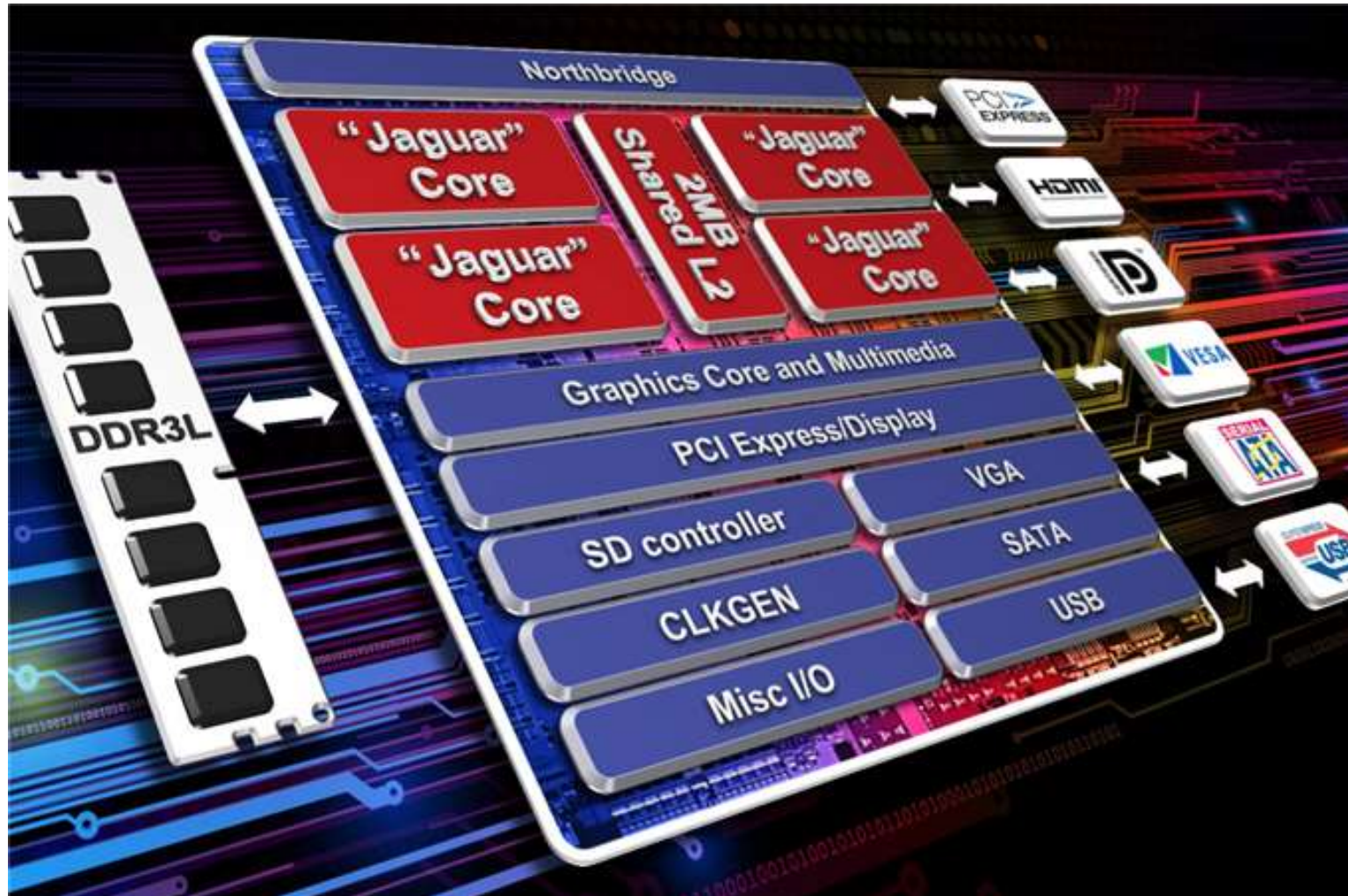


2013 AMD MAINSTREAM APU SPECS

Model	Radeon™ Brand	TDP	CPU Cores	CPU Clock Speed (Max/Base)	L2 Cache	Radeon™ Cores ¹	GPU Clock Speed (Max/Base)	MAX DDR3 Speed
AMD A-Series APUs								
A6-5200	HD 8400	25W	4	2.0GHz	2MB L2	128	600MHz	DDR3L-1600
A4-5000	HD 8330	15W	4	1.5GHz	2MB L2	128	500MHz	DDR3L-1600
AMD E-Series APUs								
E2-3000	HD 8280	15W	2	1.65GHz	1MB L2	128	450MHz	DDR3L-1600
E1-2500	HD 8240	15W	2	1.4GHz	1MB L2	128	400MHz	DDR3L-1333
E1-2100	HD 8210	9W	2	1.0GHz	1MB L2	128	300MHz	DDR3L-1333

3.3.3 The Kabini notebook APU line (5)

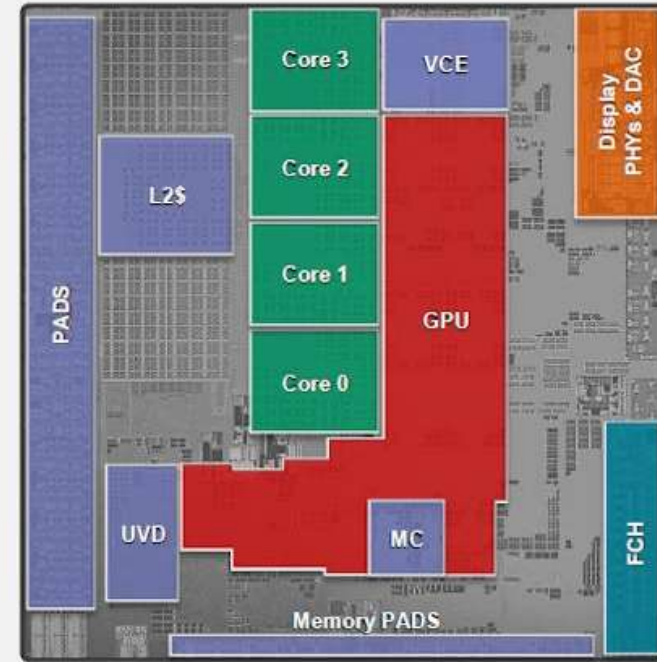
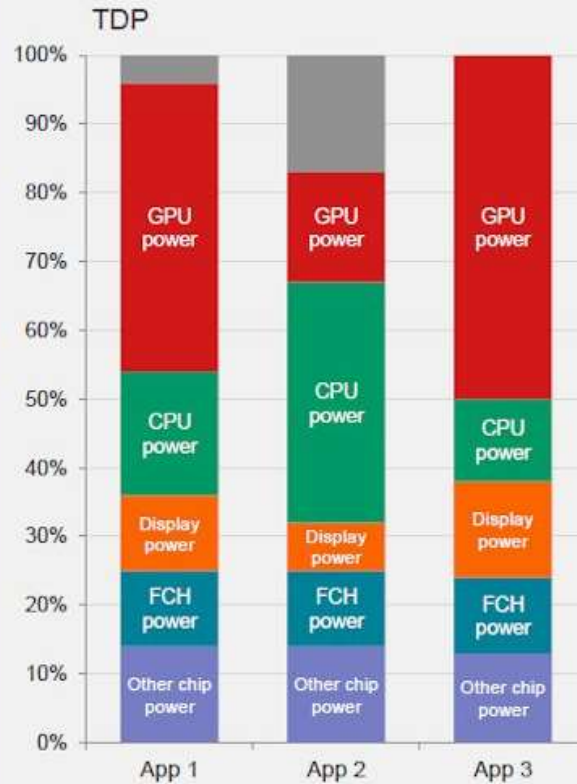
Block diagram of the Kabini notebook APU [26]



3.3.3 The Kabini notebook APU line (6)

Chip level power distribution [60]

- ▶ Power consumption (and hence performance) is set by the cooling capabilities of the platform
- ▶ Power varies a lot by workload
- ▶ We measure and manage the power of each component on the chip to generate the best performance/Watt

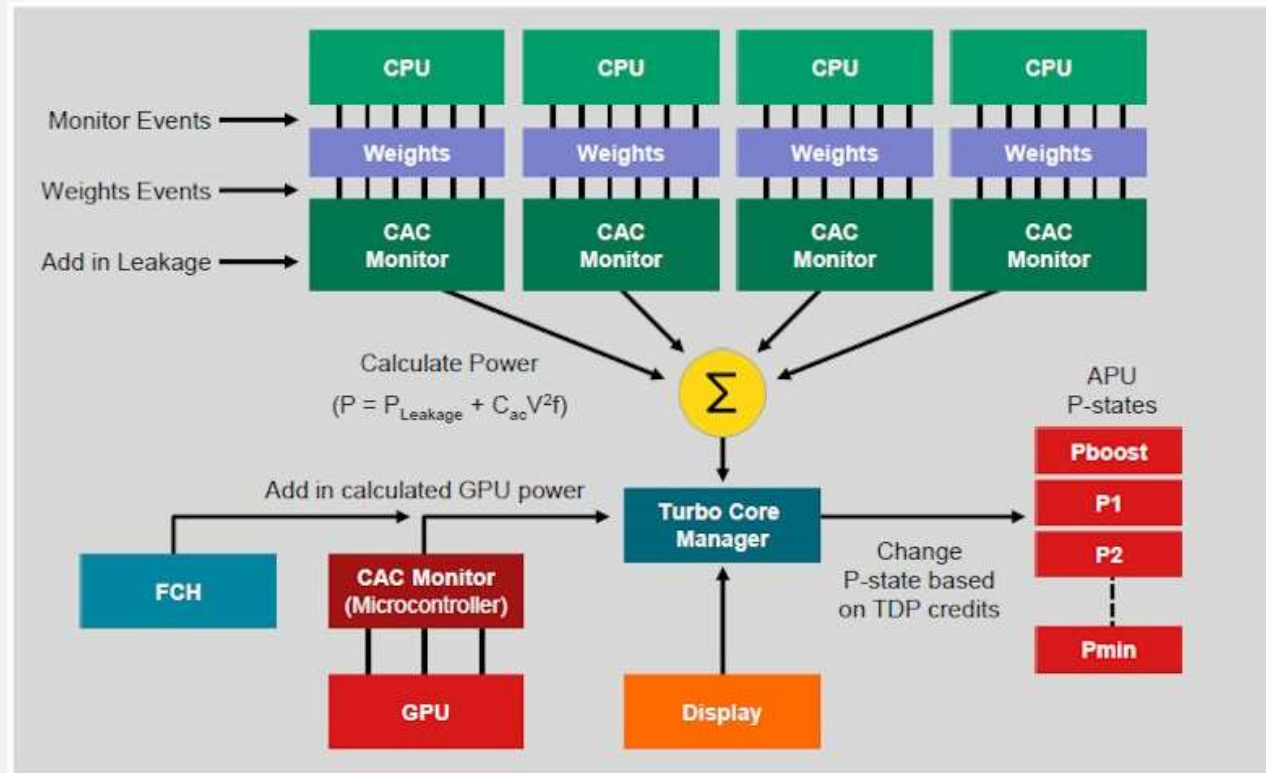


FCH: Fusion Controller Hub

3.3.3 The Kabini notebook APU line (7)

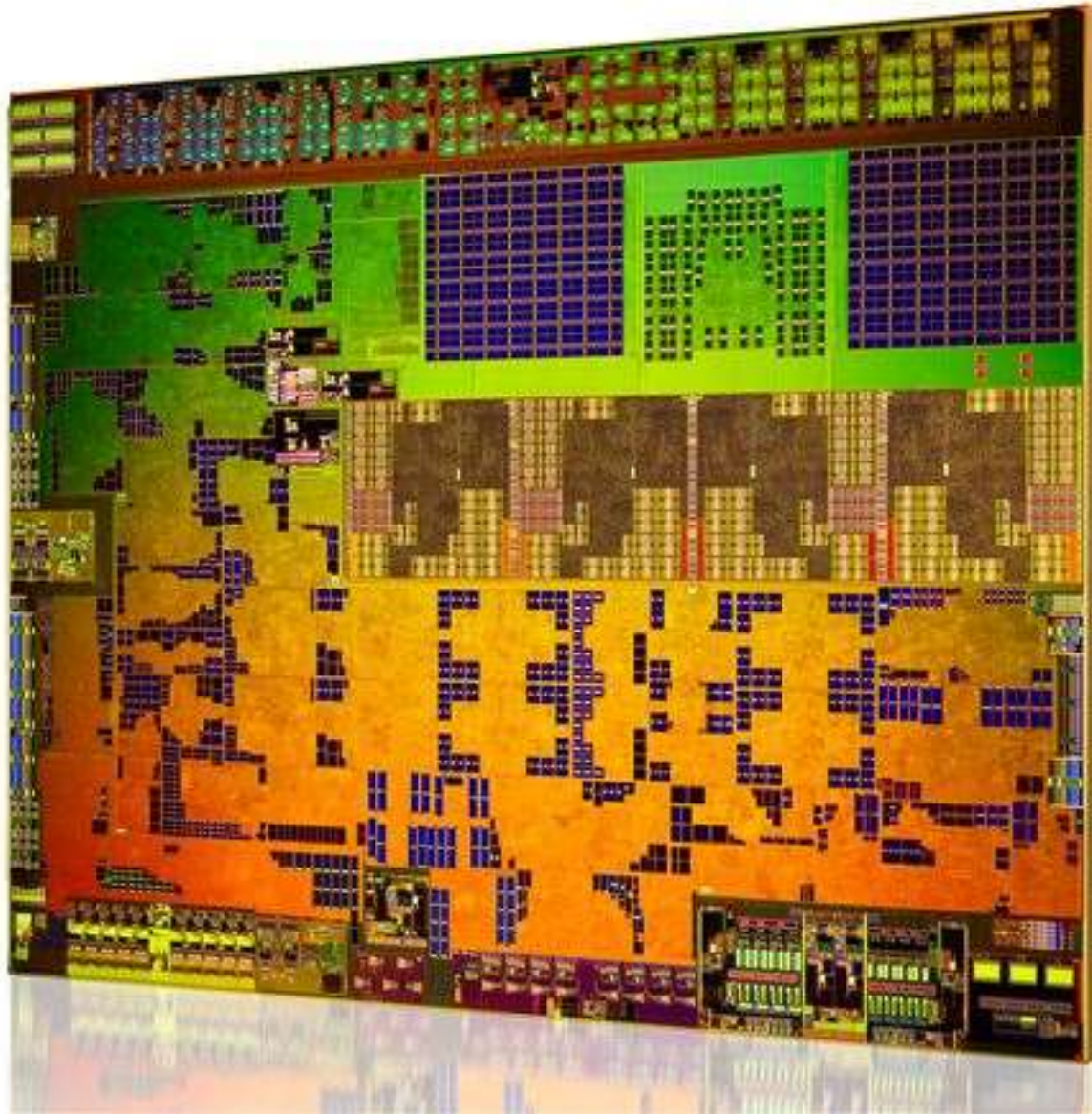
Digital Power Monitoring [60]

- ▶ In order to manage temperature and send the power wherever it's needed, we use power monitors in all chip components
- ▶ "Kabini" and "Temash" have power monitors in each CPU, the GPU, the Display Interface and the FCH
- ▶ The central controller uses this information to optimize performance within thermal constraints



3.3.3 The Kabini notebook APU line (8)

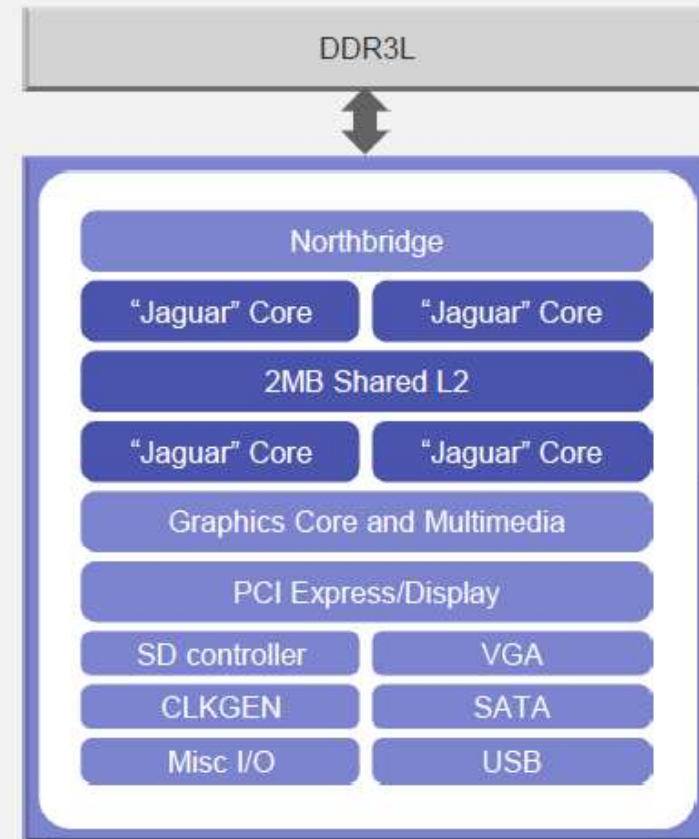
Die plot of the Kabini/Temash APU [61]



3.3.3 The Kabini notebook APU line (9)

Block diagram and main features of the Kabini notebook APU [59]

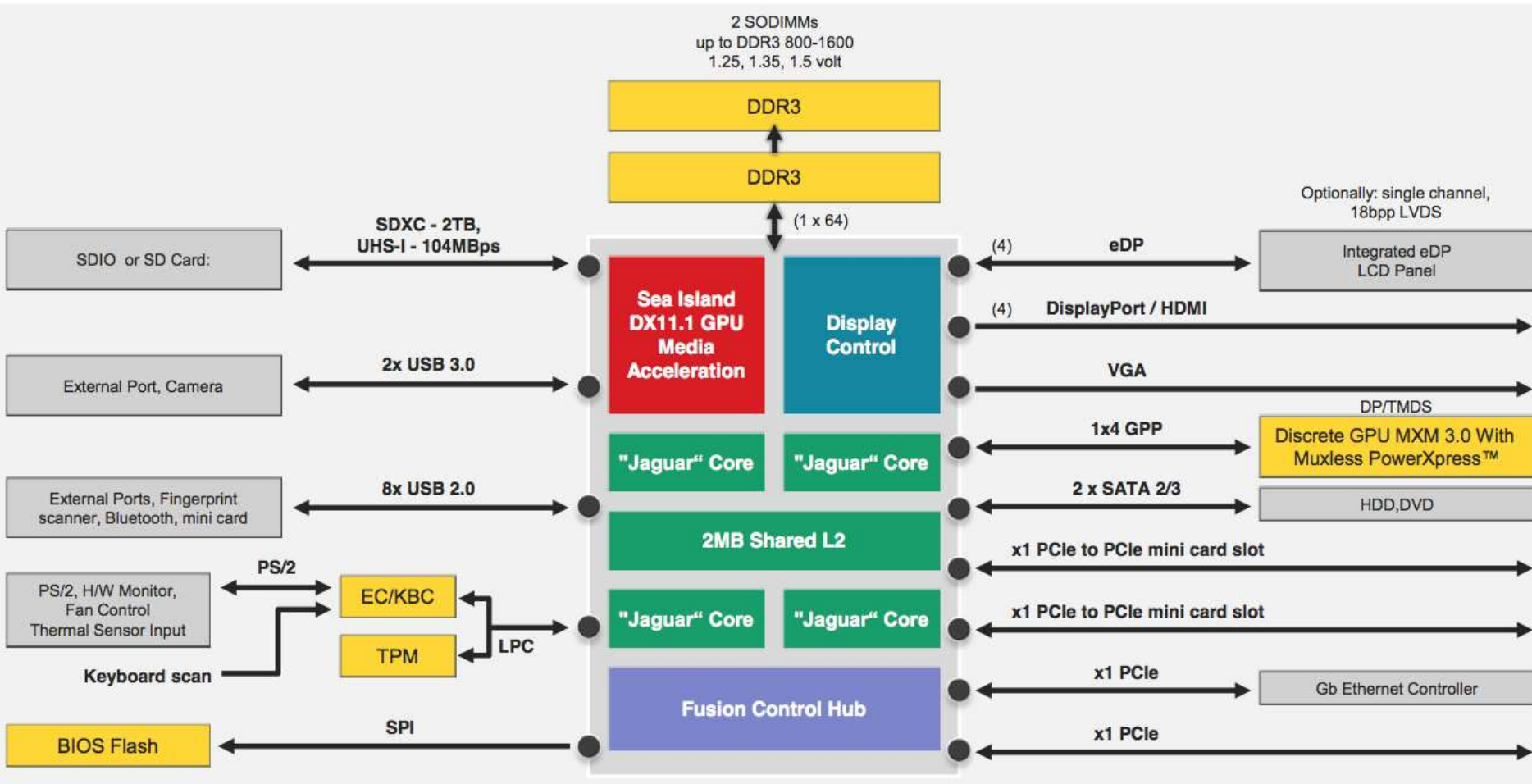
- ▶ "Jaguar" CPU Core
 - ▶ Quad Core options with a 2MB shared L2
- ▶ Graphics Core Next Radeon Graphics²⁷ with DirectX 11.1 support
- ▶ Single chip SOC enables small form factors with low BOM cost
- ▶ New Power Saving Features
 - ▶ Power gating added to DCE, UVD, VCE, UNB
 - ▶ DDR P-States for reduced power consumption
 - ▶ New IOIC 2.0
 - ▶ 9W-25W TDP
- ▶ Memory Support: Single-channel (64 bits) DDR3
 - ▶ Up to DDR3-1866; 1.5V, 1.35V & 1.25V voltage levels supported
 - ▶ 2 UDIMMs or 2 SODIMM
- ▶ Integrated display outputs
 - ▶ Supports Two Simultaneous Displays up to 4096 x 2160
 - ▶ Supports 4-lane DisplayPort 1.2, DVI, HDMI 1.4a
 - ▶ Two AUX paired lanes supporting DDC or AUX, 2 Hot Plug Detect pins, & Integrated VGA
 - ▶ Integrated eDP or 18bpp single channel LVDS
 - ▶ Next Gen AWD (AMD Wireless Display) support
- ▶ Updated I/O
 - ▶ Four x1 links of PCIe Gen 2 for GPPs
 - ▶ One x4 link of PCIe Gen 2 for discrete GPU (not on lower TDPs)
 - ▶ 8 USB2.0 + 2 USB3.0 or 10 USB2.0
 - ▶ 2 SATA Gen2/Gen3
 - ▶ SD Card Reader Version 3.0 or SDIO controller



DCE: Display Controller Engine
UVD: Unified Video Decoder
VCE: Video Compression Engine
UNB: Universal North Bridge

3.3.3 The Kabini notebook APU line (10)

Block diagram of the Kabini notebook APU platform [26]



3.3.3 The Kabini notebook APU line (11)

Main datapaths in the Kabini notebook APU platform [26]

FCL

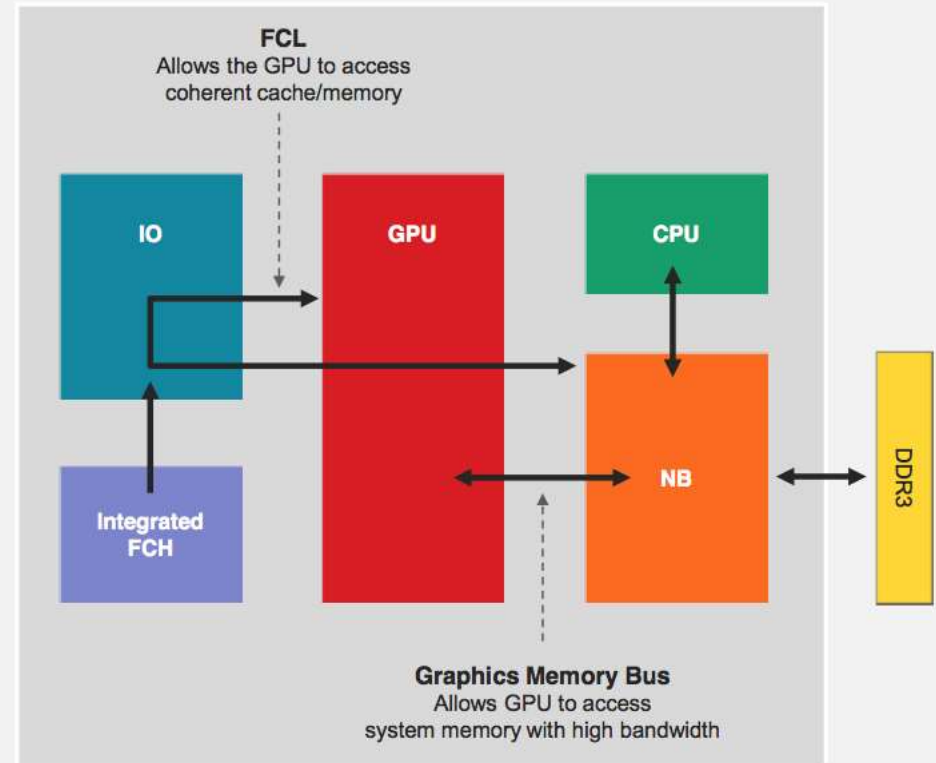
- ▶ 128b (each direction) path for IO access to memory
- ▶ GPU access to coherent memory space
- ▶ CPU access to dedicated GPU framebuffer

GRAPHICS MEMORY BUS

- ▶ 256b (each direction) for GMC access to memory
- ▶ Full bandwidth path for graphics to system memory
- ▶ DRAM-friendly stream of reads and write
- ▶ Bypasses coherency mechanism

INTEGRATED FCH

- ▶ Provides complete system connectivity
 - ▶ USB 3.0, USB 2.0, SATA 3, GPIO
 - ▶ Integrated system clock generator
- ▶ Reduced motherboard footprint required
- ▶ Higher IO performance at reduced power consumption



3.3.3 The Kabini notebook APU line (12)

Block diagram and main features of the HD8000 Graphics Core Next GPU of Kabini [26]

▶ First APU with GCN Architecture

▶ API Support:

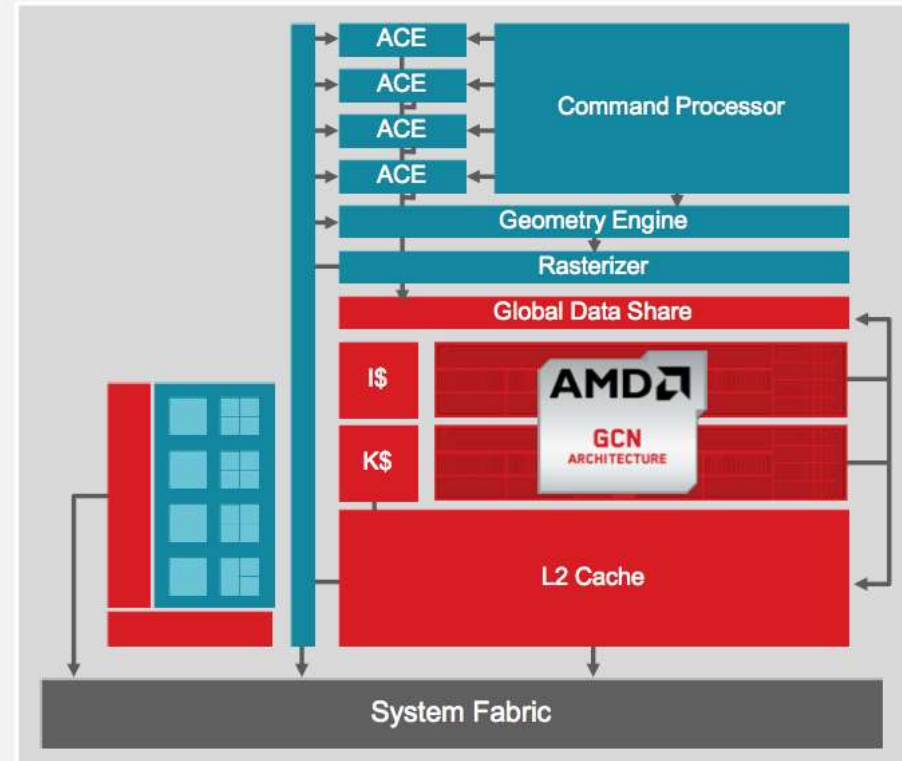
- ▶ Graphics: DirectX 11.1, OpenGL 4.3, OpenGL ES 3.0
- ▶ Compute: OpenCL1.2, DirectCompute, C++ AMP

▶ Hardware Configuration:

- ▶ Geometry Engine
 - ▶ $\frac{1}{4}$ prim/clock
- ▶ Two GCN Compute Units(CU)
- ▶ 1 Render Back-end
 - ▶ 4 Pixel Color Raster Operation Pipelines (ROPs)
 - ▶ 16 Depth Test (Z) / stencil Ops
 - ▶ Color Cache (C\$) / Depth Cache (Z\$)
- ▶ 128KB read/write L2 cache
- ▶ 4KB Global Data Share with Global synchronization resources

▶ Advanced Power Management:

- ▶ Fine grain clock/clock tree gating
- ▶ Power Tune – Dynamic V/F Scaling with power containment
- ▶ Zero Core Power – Power Gating






3.3.3 The Kabini notebook APU line (13)

AMD's preview of the Kabini notebook APU line [10]

ULTRATHINS and SMALL FORM FACTOR PCs: AMD A4 AND A6 "KABINI"


Long Battery Life, Quad-Core Performance and Rich Entertainment Features

<p>Rich Entertainment, Smart Price</p> 	<p>Responsive Performance</p> 	<p>Amazing Battery Life</p> 
---	--	---

- 50+% performance increase from "Brazos 2.0"¹⁰
- First quad-core x86 SoC
- Over 10 hours of battery life¹¹

AMD A4 **AMD A6**

AMD



3.3.3 The Kabini notebook APU line (14)

Performance figures and key features of select notebook APUs with 15-18 W dissipation [61]

CPU Performance								
	PCMark 7	Cinebench 11.5 (Single Threaded)	Cinebench 11.5 (Multithreaded)	7-Zip Benchmark (Single Threaded)	7-Zip Benchmark (Multithreaded)			
AMD A4-5000 (1.5GHz Jaguar x 4)	2425	0.39	1.5	1323	4509	28 nm	15 W	40 \$
AMD E-350 (1.6GHz Bobcat x 2)	1986	0.32	0.61	1281	2522	40 nm (Zacate)	18 W	80 \$
Intel Atom Z2760 (1.8GHz Saltwell x 2)	-	0.17	0.52	754	2304	32 nm	15 W	41 \$
Intel Core i5-3317U (1.7GHz IVB x 2)	4318	1.07	2.39	2816	6598	22 nm	17 W	225 \$

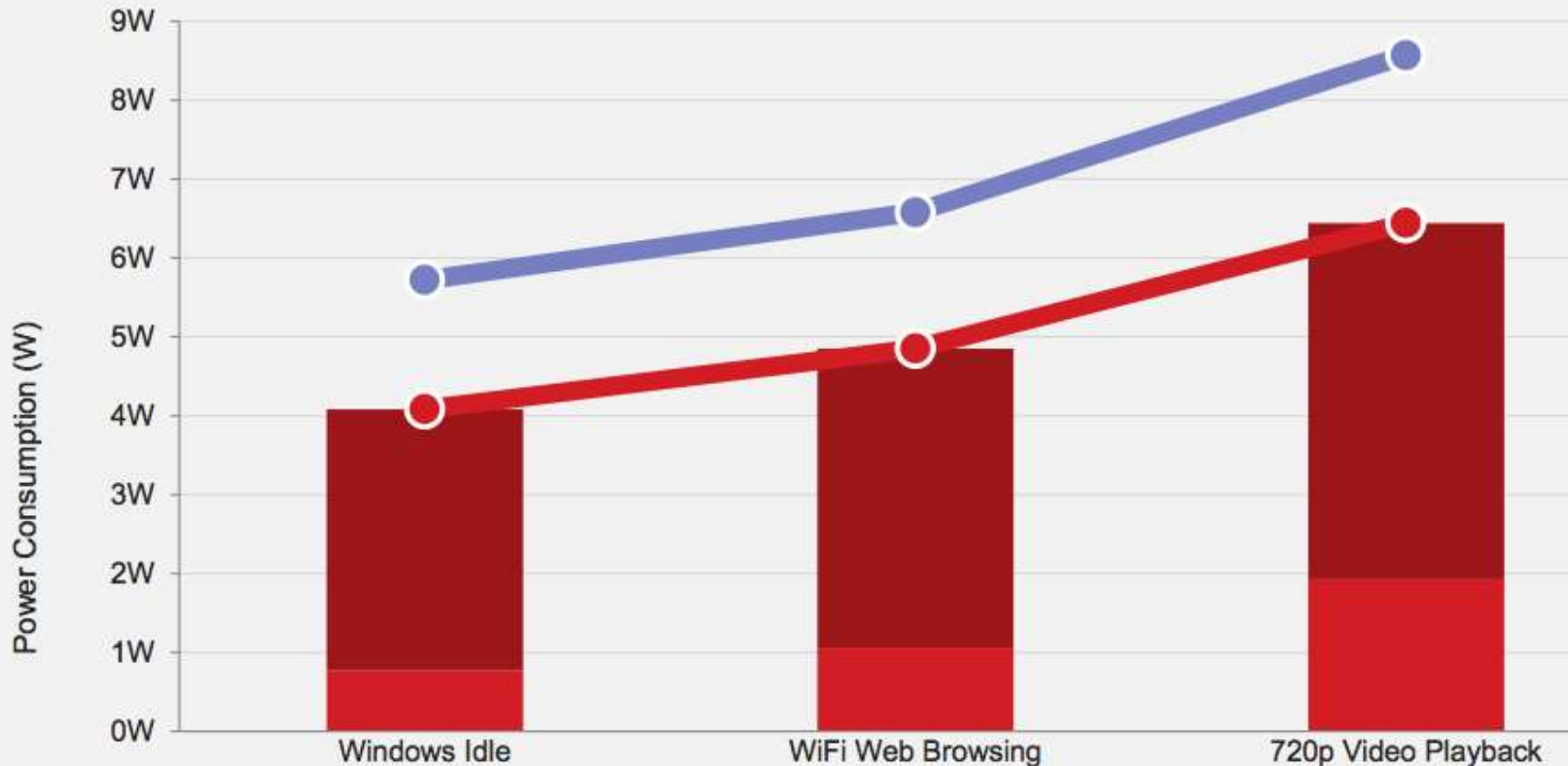
3.3.3 The Kabini notebook APU line (15)

Remarks

1. Both Intel processors are **dual-core dual-threaded** processors providing actually four logical cores for the OS.
2. While taking into account price and performance figures the **Jaguar-based Kabini APUs seem to have good market chances**.

3.3.3 The Kabini notebook APU line (16)

AMD's preview of the Kabini notebook APU line [10], [26]



Rest of System Power	3.31 W	3.79 W	4.52 W
Kabini 15W QC APU	0.77 W	1.06 W	1.92 W
Total Kabini System Power	4.08 W	4.85 W	6.44 W
Brazos 2.0 System Power	5.72 W	6.58 W	8.57 W

Brazos w/ 45Whr Battery	7.9 hours	6.8 hours	5.2 hours
Kabini w/ 45Whr Battery	11.0 hours	9.3 hours	6.9 hours

3.3.3 The Kabini notebook APU line (17)

Summary assessment of Kabini notebook APUs [61]

Compared with Bobcat-based models it can be stated that Jaguar-based Kabini APUs have compelling battery life and performance figures.

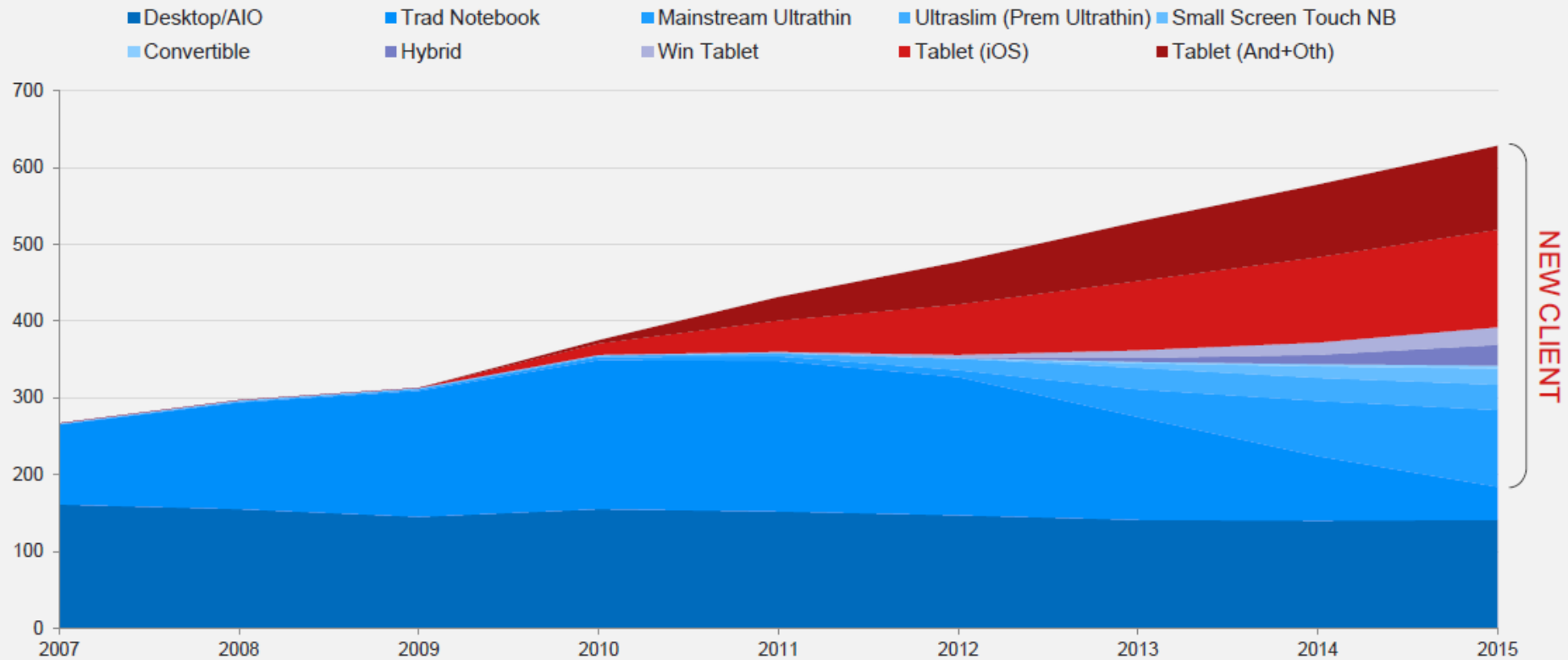
3.3.4 The Temash tablet APU line

3.3.4 The Temash tablet APU line (1)

3.3.4 The Temash tablet APU line

Increasing market share of tablets [59]

CHANGING MARKET PLACE CREATES WORLD OF "NEW CLIENT" PCS



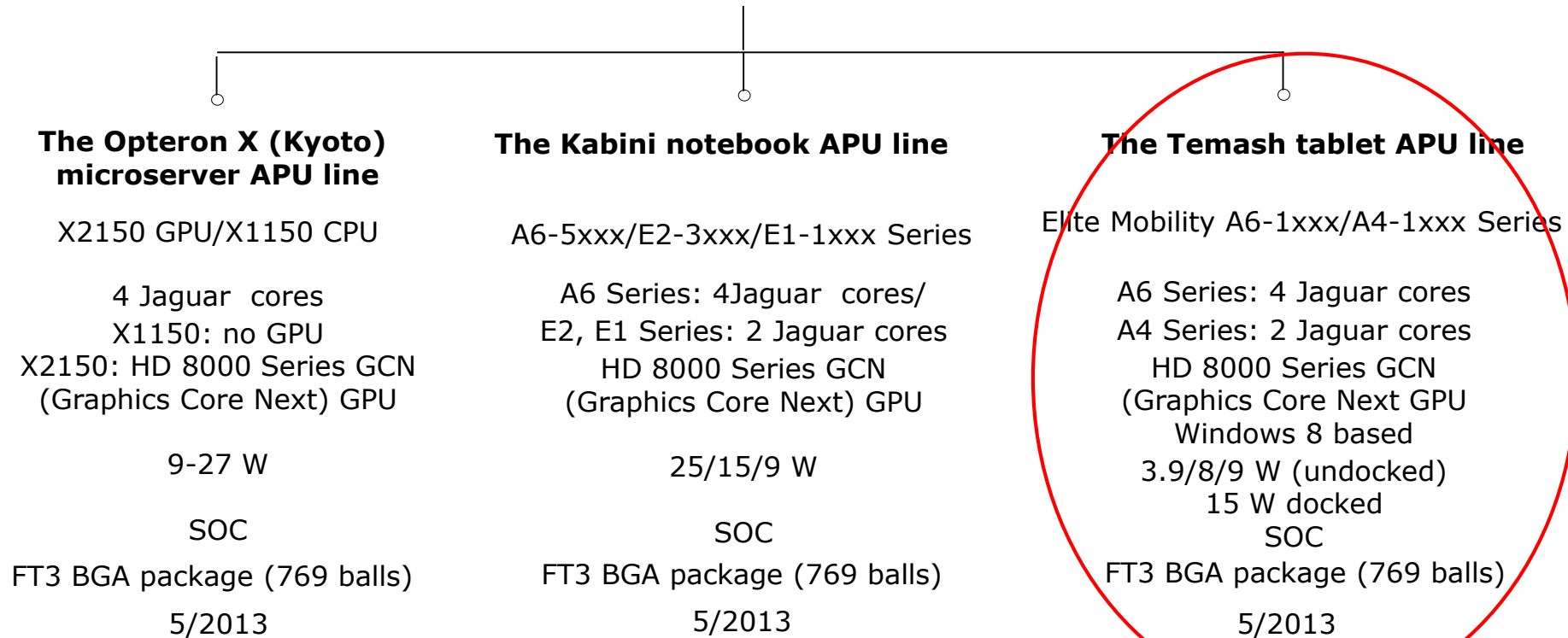
Sources: IDC AMD Extended Forecast Client World Wide by Country March 2013, IDC AMD Extended Forecast Tablet December 2012

AMD 2013 MOBILITY APU INTRODUCTION | MAY 2013

3.3.4 The Temash tablet APU line (2)

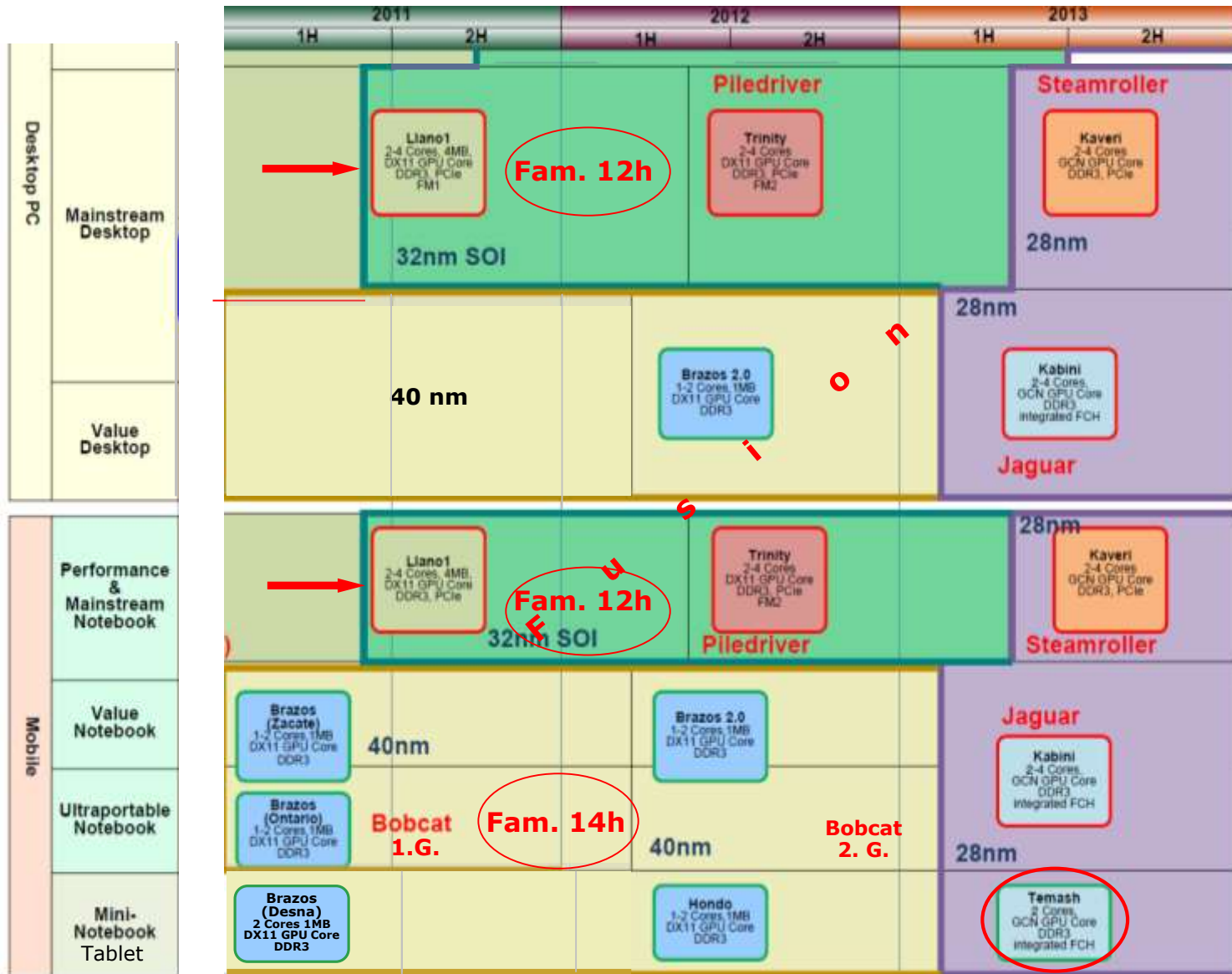
The Temash tablet line

Jaguar-based APU lines



3.3.4 The Temash tablet APU line (3)

Positioning the Temash tablet APU line -1 [based on 14]



3.3.4 The Temash tablet APU line (4)

Positioning the Temash tablet APU line -2 [2]

AMD 2013 Client Roadmap

Performance	AMD 2nd Generation A-Series APUs codename "Trinity"	AMD 2nd Generation A-Series APUs codename "Richland" Desktop, Standard notebook (35W) and Low Voltage (17-25W) 2-4 "Piledriver" CPU cores 2 nd Generation DirectX [®] 11 GPU	"Kaveri" 3rd Gen A-Series APUs 2-4 "Steamroller" CPU Cores Graphics Core Next (GCN) GPU HSA Application Support
Mainstream			
Low-Power Essential	AMD C-Series and E-Series APUs codename "Brazos 2.0" Low Voltage (9-18W) 2 "Bobcat" CPU Cores DirectX [®] 11 capable GPU		"Kabini" A-Series and E-Series APUs Complete SoC Low Voltage (9-15W) 2-4 "Jaguar" CPU cores Graphics Core Next (GCN) GPU
Ultra-Low Power Tablet/Fanless	AMD Z-Series APU codename "Hondo" 1-2 "Bobcat" CPU Cores, Ultra Low Voltage (4.5W), DirectX [®] 11 capable GPU		"Temash" A-Series Elite Mobility APUs Ultra Low Voltage; Complete SoC; 2-4 "Jaguar" CPU Cores Graphics Core Next (GCN) GPU

AMD roadmaps are subject to change without notice

40nm 32nm 28nm



January 7, 2013

Remark

Temash is AMD's third tablet design

Actually, AMD's **first tablet design** was the **Bobcat-based Desna Z-01**.

- It included dual Bobcat cores, a Rqdeon HD 6250 GPU and run at 1 GHz core frequency.
- The Z-01 **was not yet a SOC design** (it needed an FCH) and had a TDP of 5.9 W.
- Its major drawback was that it needed a fan.
- The Z-01 **did not gain a wide market acceptance**, only a single tablet opted for it (the MSI WinPad 110) [11].

AMD's **second tablet design** was the **2. gen. Bobcat based Z-60 Hondo**.

- The Hondo Z-60 supports **Windows 8** rather than Android.
- It has the **same basic features as the previous design** (dual 2. gen. Bobcat cores, the Radeon HD 6250 GPU, 1 GHz clock frequency) but a reduced TDP of 4.5 W).

In addition, Z-60 comes with a **redesigned Fusion controller hub** (FCH), which has a number of capabilities switched off **to reduce power consumption**.

- Also the Z-60 Hondo **could not achieve a wide market acceptance**, there are only a few tablet designs based on it [12].

3.3.4 The Temash tablet APU line (6)

Main features of Temash tablet APU models [59]

Model	Radeon™ Brand	TDP	CPU Cores	CPU Clock Speed (Max/Base)	L2 Cache	Radeon™ Cores*	GPU Clock Speed (Max/Base)	MAX DDR3 Speed
AMD A-Series Elite Mobility APUs								
A6-1450	HD 8250	8W	4	1.4GHz/1.0GHz	2MB L2	128	400MHz/300MHz	DDR3L-1066
A4-1250	HD 8210	9W	2	1.0GHz	1MB L2	128	300MHz	DDR3L-1333
A4-1200	HD 8180	3.9W	2	1.0GHz	1MB L2	128	225MHz	DDR3L-1066

3.3.4 The Temash tablet APU line (7)

Main features of the K16 Temash tablet APU line [13]

AMD's Family 14h (Jaguar)-based Temash tablet APU lines



Temash A6 tablet APU line

4 Jaguar cores

2 MB shared L2 cache

5/2003

Temash A4 tablet APU line

2 Jaguar cores

1 MB shared L2 cache

5/2013

HD-8000 Series (GCN) GPU.
DDR3 memory controller
Selected parts support Turbo Dock technology
Added SSE4, AVX, AES, F16C and BMI1 instructions.
FPU datapath width was increased from 64 to 128 bits.
Added hardware integer divider.
Doubled bandwidth of load/store units.
Added L2 prefetcher and enhanced L1 instruction cache prefetcher.
More aggressive clock and power gating, aimed at reducing overall power consumption.
SOC.
BGA FT3 package.

AMD's Turbo Dock technology-1

- First will be introduced in select models of Temash.
- The Turbo Dock technology is actually a **hybrid design** (as shown below) meaning that the tablet has a **dock station** that provides **keyboard, fan-based cooling and may provide an additional battery** as well.



Figure: Hybrid design with a dock station [14]

AMD's Turbo Dock technology-2

- Without the dock station the tablet runs at 1 GHz and has a TDP of 5.9 W.
- When docked, the tablet runs at 1.4 GHz and its TDP scales up to 15 W utilizing the fan-based cooling provided by the dock station.
This provides a performance gain of about 40 %.

Remark

The concept underlying the Turbo Dock technology is not new.

Already Lenovo's ThinkPad Helix tablet has a hybrid design such that the tablet boosts performance when docked with the aid of a cooling system located in the hinge of the keyboard docking station [15].

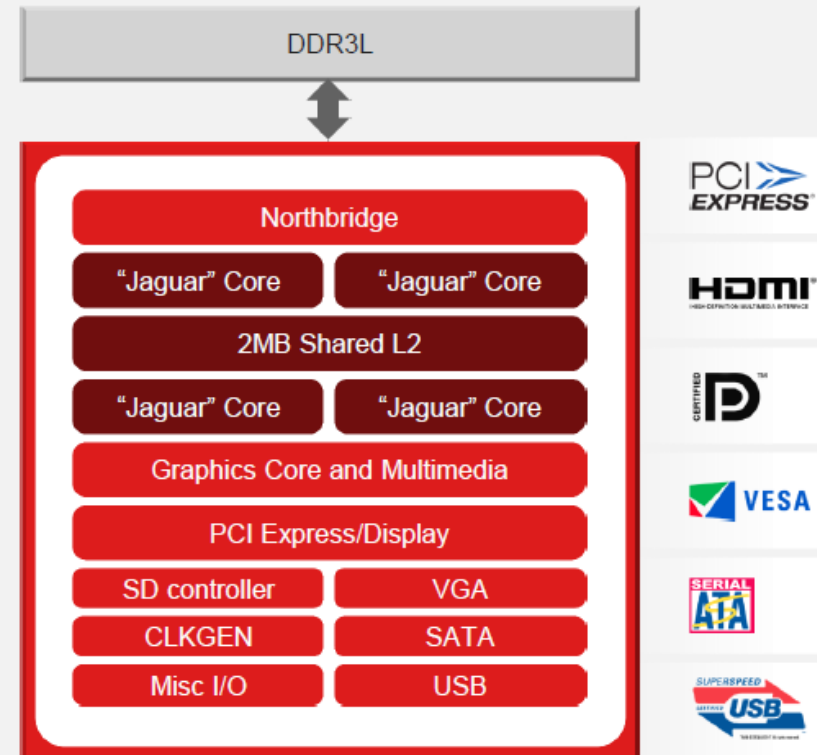
3.3.4 The Temash tablet APU line (10)

Block diagram and main features of the Temash tablet APU-based Elite Mobility APU platform [59]

2013 AMD ELITE MOBILITY APU PLATFORM DETAILS



- ▶ Dual/Quad Core, AMD Start Now Technology¹⁷ w/smart sleep
- ▶ AMD Turbo Dock Technology for 40% performance boost¹
- ▶ “Jaguar” Core: Up to 20% improvement over “Bobcat” cores¹⁸
- ▶ “GCN” GPU core: Up to 75% compute performance (GFLOP) improvement with DirectX® 11.1 support¹⁹
- ▶ Power gating for DCE, UVD, VCE, NB and DDR P-States
- ▶ Memory Support: Single-channel (64 bits) DDR3
- ▶ High Resolution display supporting dual up to 2560 x 1600
- ▶ Faster than real time HD encode - H.264, SVC HDCP 2.1
- ▶ Protected Content DRM offloaded from CPU, HDCP 2.1
- ▶ Updated I/O: Up to 8 USB 2.0 and 2 USB 3.0, 1 SATA Gen2, SD Card Reader Version 3.0 or SDIO controller

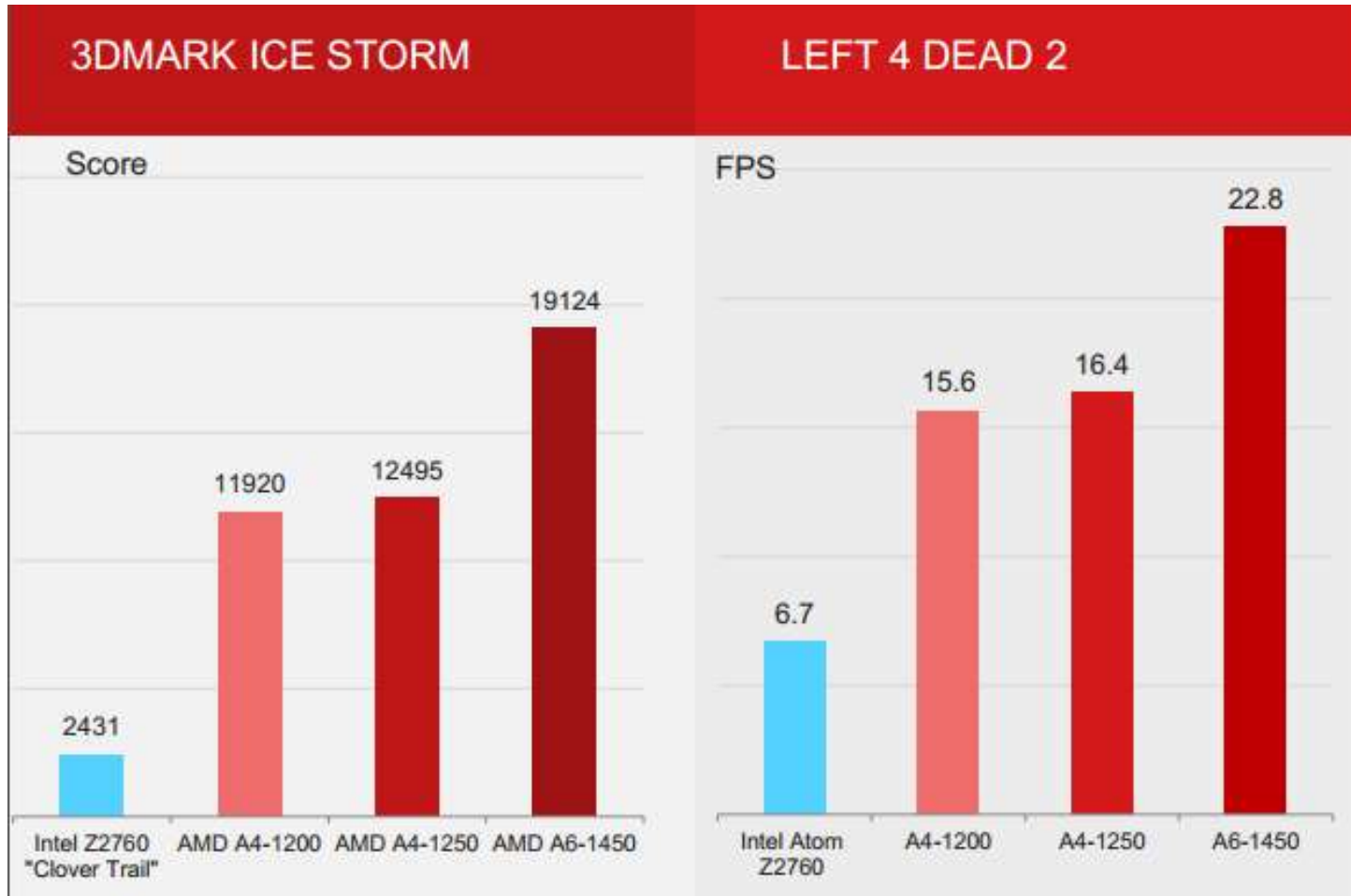


DCE: Display Controller Engine
UVD: Unified Video Decoder
VCE: Video Compression Engine
NB: North Bridge
HDCP: High-Bandwidth Digital Content Protection

See backup for footnotes 16

3.3.4 The Temash tablet APU line (11)

Performance figures of the Temash tablet line vs. Intel's Atom Z2760 [27]



4. Family 16h Models 30h-3FH (Puma+ based) APU lines

- 4.1 Overview of the Puma+ based APU lines
- 4.2 The Puma core
- 4.3 Enhancements and innovations introduced in the Puma+ based APU lines
- 4.4 The Beema notebook line
- 4.5 The Mullins tablet line
- 4.6 The Carrizo-L notebook line

4.1 Overview of the Puma+ based APU lines (1)

4.1 Overview of the Puma+ based APU lines -1

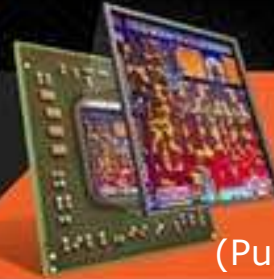
Brand names of AMD's Puma+ based processor lines

	Launched in	2011	2012	2013	2014	2015
		Family 14h (00h-0Fh) (Bobcat)	Family 14h (00h-0Fh) (Bobcat)	Family 16h (00h-0Fh) (Jaguar)	Family 16h (30h-3Fh) (Puma+)	Family 16h (30h-3Fh) (Puma+)
Servers	4P servers					
	2P servers					
	1P servers					
	(85-140 W)					
Desktops	High perf. (~95-125 W)					
	Mainstream (~65-100 W)					
	Entry level (~30-60 W)					
Notebooks	High performance/ mainstream/entry (~30-60 W)			Kabini A6		
	Ultra portable (~10-15 W)	Zacate E-Series Ontario C-Series	Zacate E1/E2	Kabini A/E-Series	Beema A/E-Series	Carrizo-L A/L-Series
	Tablet (~5 W)	Desna Z-Series		Temash A Series	Mullins A Series/E1	

4.1 Overview of the Puma+ based APU lines (2)

Key features of AMD's subsequent mobile generations [67]

CATEGORY CREATOR, PERFORMANCE LEADER



"MULLINS"
"BEEMA"

(Puma based)

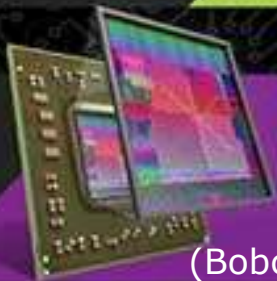
- ▲ Now delivering up to 2X the compute performance-per-watt vs. the competition for Mainstream PCs¹



"TEMASH"
"KABINI"

(Jaguar based)

- ▲ First to deliver x86 Quad-core SoC and Graphics Core Next (GCN) performance



"BRAZOS"

(Bobcat based)

- ▲ Re-created the essential-level notebook category, bringing more performance and features to <\$499













4.1 Overview of the Puma+ based APU lines (3)

AMD's announcement of the Puma+ based Beema and Mullins lines in 11/2013 [68]

AMD 2013-2014 MOBILITY ROADMAP



	2013	2014
Performance	<p>"Richland" APU 2-4 "Piledriver" CPU Cores 2nd Generation DX[®]11 GPU Cores 17W-35W</p> 	<p>"Kaveri" APU 2-4 "Steamroller" CPU Cores GCN Graphics Compute Units HSA Features AMD TrueAudio 15W-35W</p> 
Mainstream	<p>"Kabini" APU 2-4 "Jaguar" CPU Cores GCN Graphics Compute Units 15W-25W</p>  	<p>"Beema" APU 2-4 "Puma" CPU Cores GCN Graphics Compute Units AMD Security Processor 10W-25W</p>  
Low-Power Essential	<p>"Temash" APU 2-4 "Jaguar" CPU Cores GCN Graphics Compute Units 3W-4W SDP</p>  	<p>"Mullins" APU 2-4 "Puma" CPU Cores GCN Graphics Compute Units AMD Security Processor ~2W SDP</p>  

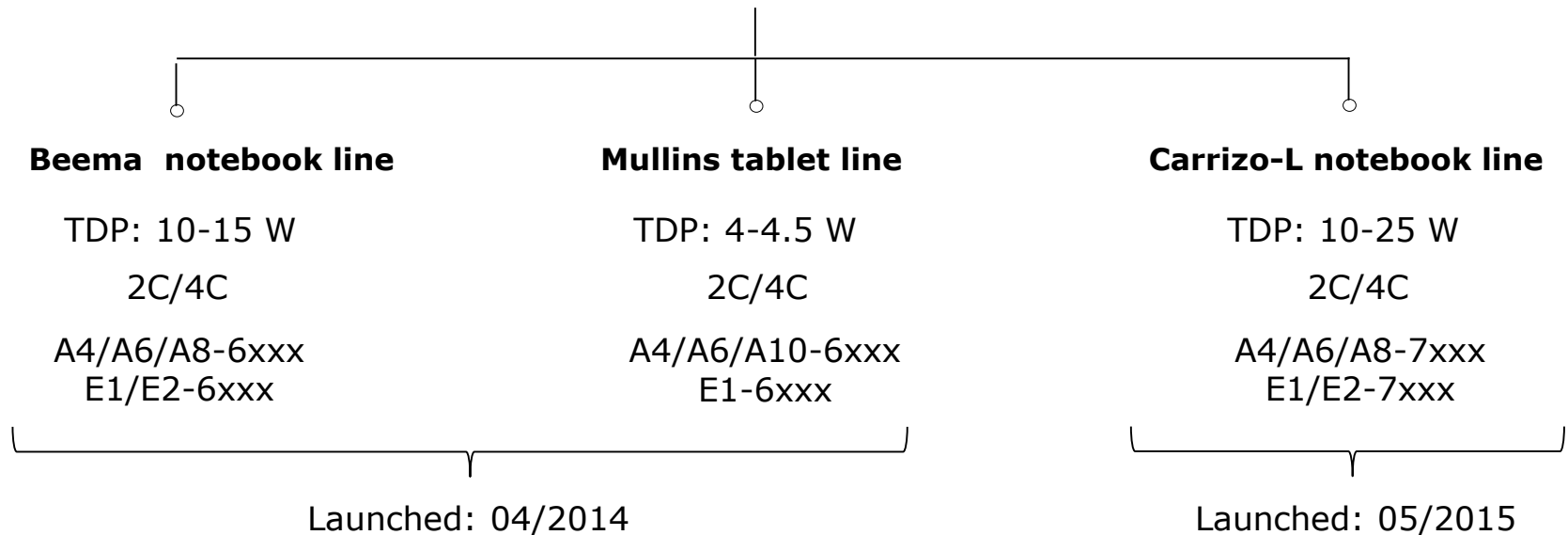
AMD roadmaps are subject to change without notice or obligations to notify of changes. Placement of boxes intended to represent first year of production shipments.

4.1 Overview of the Puma+ based APU lines (4)

Overview of the Puma+ based APU lines -2

- The **Puma+ core** provides **only modest performance improvements** rather they afford **advances in power management and security**, as detailed in Section 4.3.
- Puma+ based APU lines were launched in two groups, as indicated below.

Puma+ based APU lines



4.1 Overview of the Puma+ based APU lines (5)

Key features of the Puma+ based lines (based on [66])

Brand	Desna Ontario Zacate			Kabini	Temash	Beema	Mullins	Carrizo-L
Aim	T	T	EDT/NB	EDT/NB	T	EDT/NB	T	EDT/NB
Released	Jan 2011			May 2013		April 2014		May 2015
Fab. (nm)	TSMC 40			28		28		28
Die size (mm²)	75 (+ 28 FCH)			~107		~107		TBA
Core count (up to)	2			4		4		4
L2 cache	Privat			Shared		Shared		Shared
CPU microarch.	Bobcat			Jaguar		Puma+		Puma+
Socket	FT1			AM1, FT3		FT3b		FP4
Memory support	DDR3L-1333 DDR3L-1066			DDR3L-1600 DDR3L-1333	DDR3L-1333 DDR3L-1066	DDR3L-1866 DDR3L-1600 DDR3L-1333	DDR3L-1333 DDR3L-1066	DDR3L-1866 DDR3L-1600 DDR3L-1333
3D engine	TeraScale (VLIW5)			GCN 2nd Gen		GCN 2nd Gen		GCN 2nd Gen
Video Decoder ASIC	UVD 3.0			UVD 4.0		UVD 4.2		UVD 6.0
Video Encoding ASIC	N/A			VCE 2.0		VCE 2.0		VCE 3.1

EDT: Entry-level desktop NB: Notebook T: Tablet

4.1 Overview of the Puma+ based APU lines (6)

Transistor count and die area comparisons of mobile processors [69]

AMD/Intel Transistor Count & Die Area Comparison			
SoC	Process Node	Transistor Count	Die Area
AMD Zacate	TSMC 40nm	450M+	75mm ²
AMD Kabini/Temash	TSMC 28nm	914M	~107mm ² (est)
AMD Beema/Mullins	GF 28nm	930M	~107mm ² (est)
AMD Llano	GF 32nm SOI	1.18B	228mm ²
AMD Trinity/Richland	GF 32nm SOI	1.30B	246mm ²
AMD Kaveri	GF 28nm SHP	2.41B	245mm ²
Intel Haswell (4C/GT2)	Intel 22nm	1.40B	177mm ²

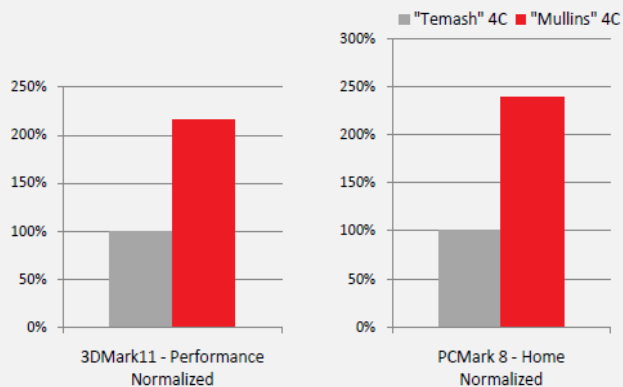
GF: Globalfoundries (USA) TSMC: Taiwan Semiconductor Manufacturing Company

4.1 Overview of the Puma+ based APU lines (7)

Preliminary performance figures given by AMD at announcing Beema and Mullins [68]

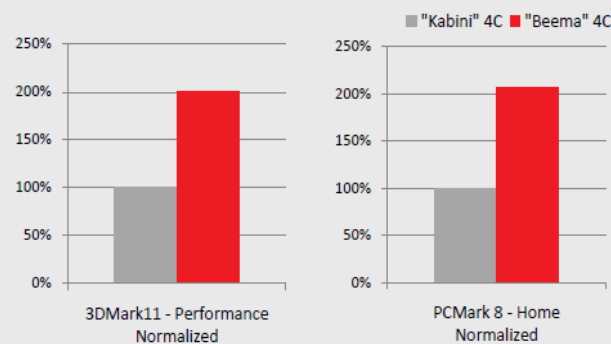
“MULLINS”

Outstanding performance in an SOC designed for fanless tablets, 2-in-1s, and notebooks



“BEEMA”

More performance and the latest features for a better experience in mainstream & entry 2-in-1s AND NOTEBOOKS



More than **2X** the performance per watt of the previous generation¹

- ▲ AMD Radeon™ graphics: The world's best graphics technology that is found in all the latest game consoles AND in PCs that deliver richer more lifelike videos, movies, photos and the best gaming experience
- ▲ AMD DockPort technology support
- ▲ Microsoft 8.1 optimizations and Microsoft InstantGo² for faster wake times and to ensure data, such as e-mail, actively refreshes in standby
- ▲ Platform security processor based on the ARM Cortex™-A5 processor featuring ARM TrustZone® technology for enhanced data security

4.2 The Puma core

4.2 The Puma core (1)

4.2 The Puma+ core

- As AMD states in [], there are only a few minor changes concerning the Puma+ core (underlying the Family 16h Models 30h-3Fh processors) compared to the Jaguar core (underlying the Family 16h Models 00h-0Fh processors).

These minor changes include the introduction of a performance time-stamp counter, a processor power accumulator and the implementation of the RDRAND instruction.

- Accordingly, the Puma+ core has a two-wide out-of-order superscalar microarchitecture like the Jaguar core.
- AMD claims a 19 % reduction in the core leakage at 1.2 V compared to the Jaguar core.
- This contributes to achieving higher clock frequencies within the same TDP [70].

Remark to the Puma+ designation of the core

- AMD names the CPU core of the Beema and Mullins processors in different publications differently.

On the one hand, AMD terms these cores Puma in their 2014 roadmap (revealed in 11/2013) whereas at launching (04/2014) these processors were dubbed Puma+.

- A possible explanation for this may be found in newer releases of the original description of the Puma+ based processor lines (e.g. [63]), as Revision 3.01 (dated on 12/2014) provides a long list of changes.

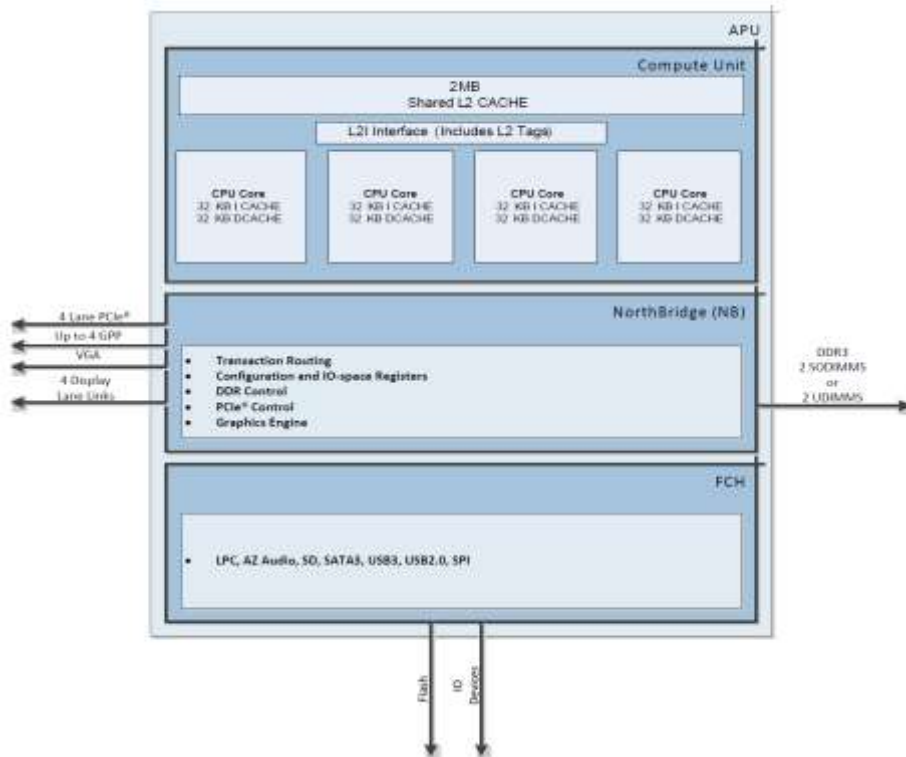
Based on this, the original Puma core can be assumed to have undergone an update and a renaming to Puma+ but the new designation obviously could not retrospective be employed to the roadmap issued previously.

4.3 Enhancements and innovations of the Puma+ based APU lines

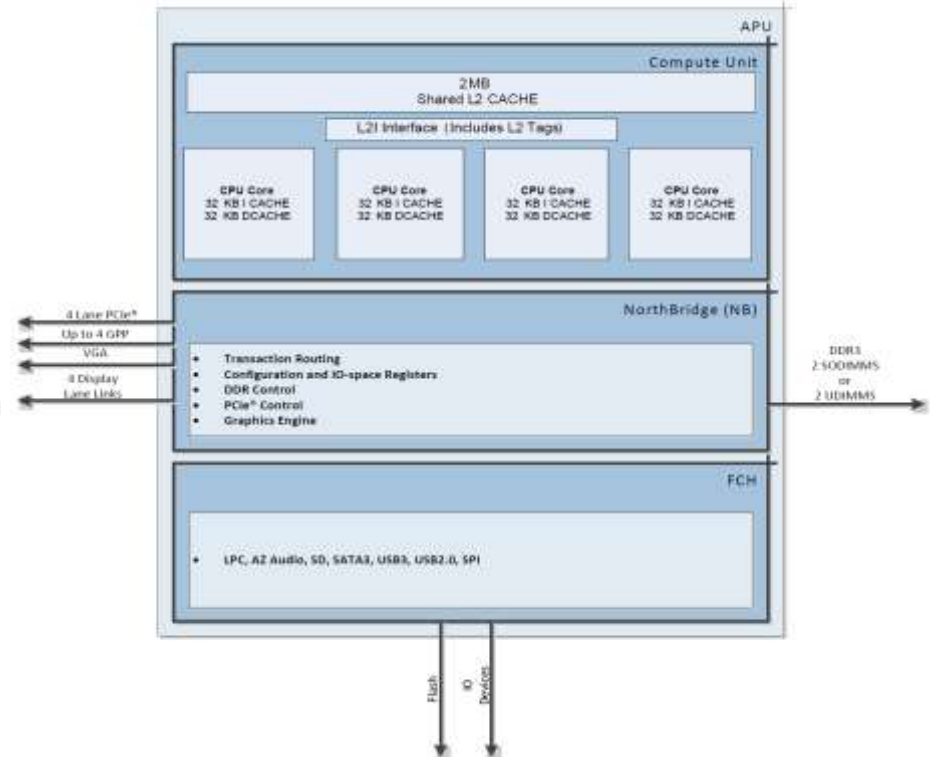
4.3 Enhancements and innovations of the Puma+ based APU lines (1)

4.3 Enhancements and innovations introduced into Puma+ based APU lines Comparing the layouts of Jaguar and Puma+ based APUs [63], [64]

Jaguar



Puma+



As a comparison shows the **layouts** of Jaguar-and Puma+ APUs as revealed in the official BKDG (BIOS and Kernel Developer Guide) publications are **identical**.

4.3 Enhancements and innovations of the Puma+ based APU lines (2)

Enhancements of the Puma+ core based Beema and Mullins APUs


- a) Higher clock frequencies at lower power consumption
- b) Higher memory transfer rates
- c) Lower powered memory and display controllers

4.3 Enhancements and innovations of the Puma+ based APU lines (3)

a) Higher clock frequencies at lower power consumption [70]

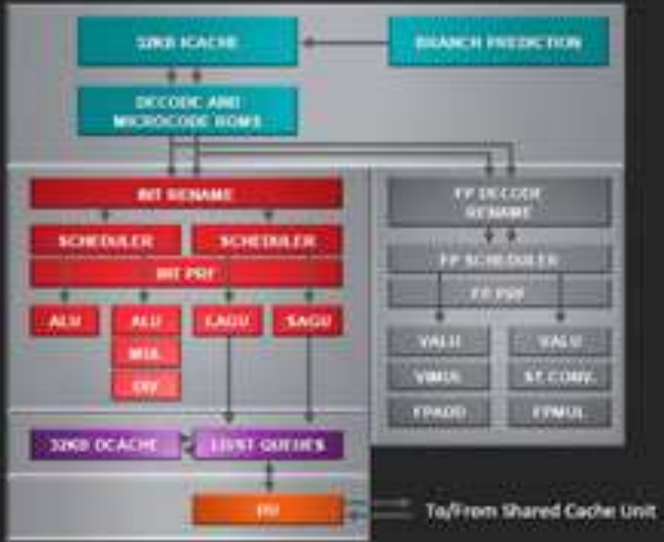
CPU CORE ENHANCEMENTS

"PUMA+" SPRINTS AHEAD



"JAGUAR" MICROARCHITECTURE

WITH MORE FREQUENCY AND OPTIMIZED POWER



Ta/From Shared Cache Unit

URNS "PUMA+" INTO A SIGNIFICANT LEAP UP

2013	"Jaguar"	2014	"Puma+"
2.0 GHz	"Kabini"	2.4 GHz	"Beema"
1.4 GHz	"Temash"	2.2 GHz	"Mullins"

POWER OPTIMIZED

19% LEAKAGE REDUCTION²²

4.3 Enhancements and innovations of the Puma+ based APU lines (4)

b) Higher memory transfer rates

Both Beema and Mullins have **single channel DDR3L** memories but the desktop and entry-level Beema has a higher max. transfer rates than the preceding Kaveri, as indicated below:

- **Entry-level desktop and notebook aimed lines:**
 - Beema provides up to 1866 MT/s vs. up to 1600 MT/s furnished by Kaveri
- **Table aimed lines:**
 - Mullins provides the same max. transfer rate of 1333MT/s as the preceding Temas.

4.3 Enhancements and innovations of the Puma+ based APU lines (5)

c) Lower powered memory and display controllers [70]

I/O ENHANCEMENTS



LOW POWER DDR INTERFACE

- ▲ New low power DDR mode optimized for lowest power DDR3-1333
- ▲ Over 500 mW reduction compared to DDR3-1333 in standard DDR mode²⁴

DDR3-1866

- ▲ Optimized performance for mainstream notebooks
- ▲ 5% improvement in 3DMark® Cloud Gate performance versus DDR3-1600²⁵

LOWER POWER DISPLAY INTERFACE

- ▲ Power reduction through use of voltage-mode logic (VML)
- ▲ Estimated 200 mW power reduction for high resolution displays²⁸



4.3 Enhancements and innovations of the Puma+ based APU lines (6)

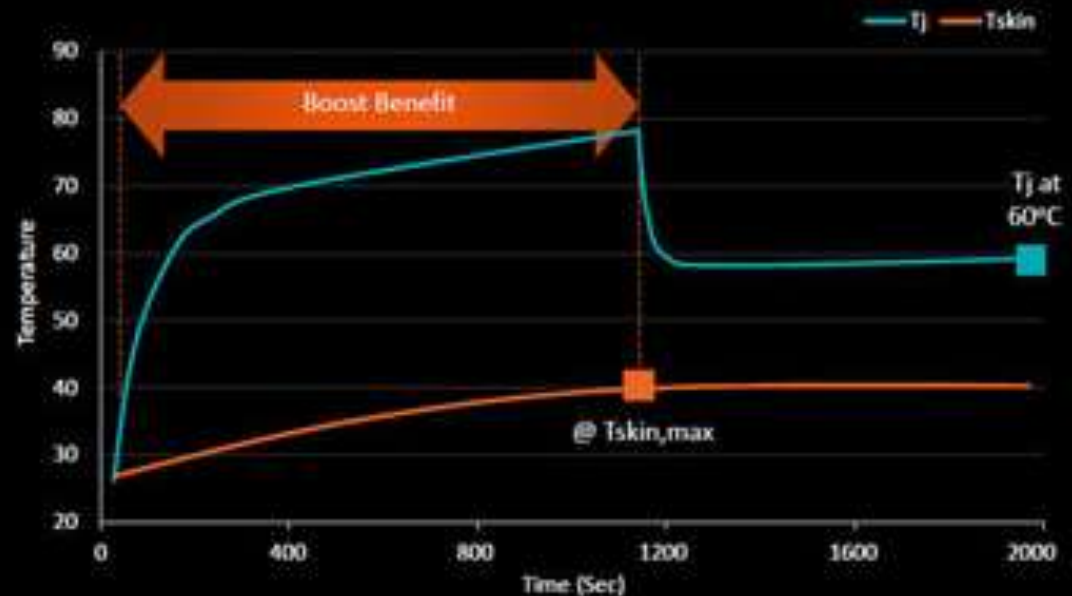
Innovations introduced by the Puma+ based APUs (Beema/Mullins)

- a) Skin temperature aware power management (STAM)
- b) Intelligent boost (selective boost)
- c) Adaptive voltage control to encounter short voltage drops
- d) Support for ARM TrustZone via integrated Cortex-A5 processor

4.3 Enhancements and innovations of the Puma+ based APU lines (7)

a) Skin temperature aware power management (STAM) [70] (Chassis temperature aware turbo boost)

- ▲ Boost aggressively until T_{skin} reaches user defined maximum
- ▲ Reduce power only when necessary to adhere to $T_{skin,max}$ limit
- ▲ Most use-cases for mobile devices are short in duration → Result is higher performance most of the time
- ▲ All without using more power



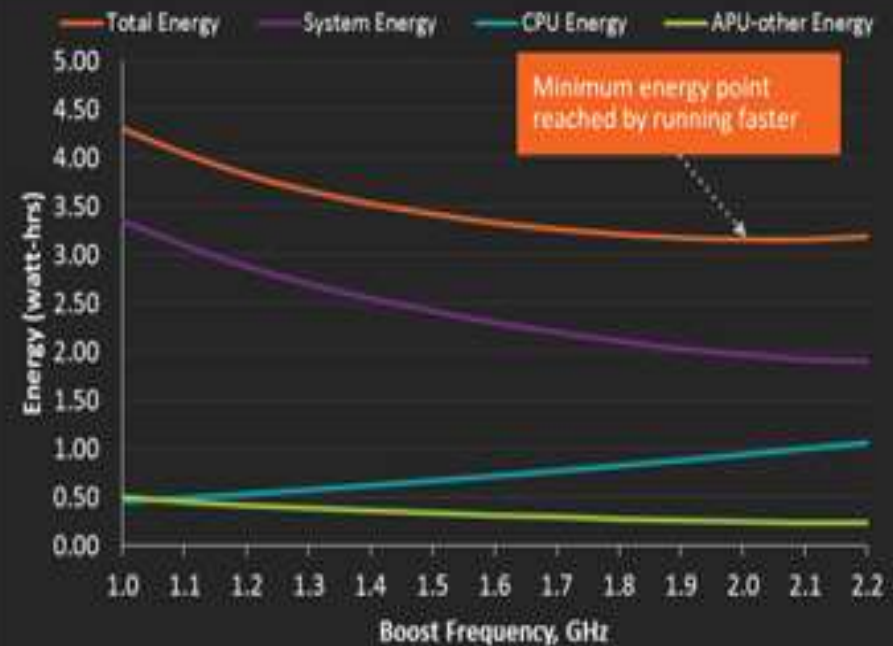
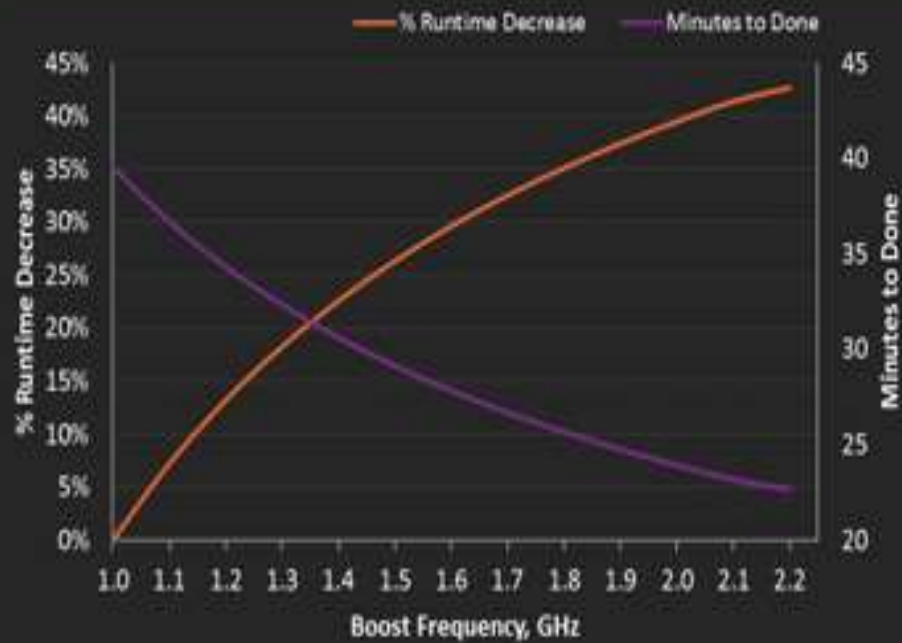
**DYNAMIC SKIN-TEMPERATURE AWARE POWER MANAGEMENT CAN ENABLE UP TO
63% PERFORMANCE INCREASES¹ ON KEY WORKLOADS.**

1. Based on 3DMark11-P and PCMark8 V2 Home on 3.5W TSP Mullins with and without STAPM enabled. Pre-production engineering sample of "Mullins" quad-core APU with next generation AMD Radeon graphics (model number TBD), 2x2GB DDR3-1333MHz RAM, Windows 8.1, and unreleased reference driver.

4.3 Enhancements and innovations of the Puma+ based APU lines (8)

Benefit of STAM: Higher turbo boost frequency reduces the total energy consumption [71]

SINGLE CORE WEB BROWSING BENCHMARK EXAMPLE¹



4.3 Enhancements and innovations of the Puma+ based APU lines (9)

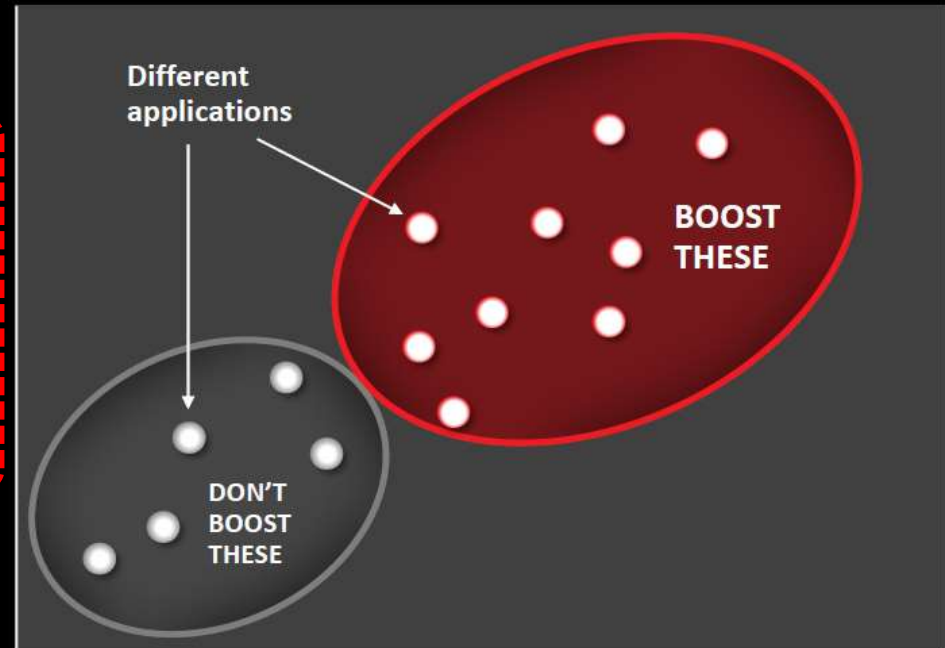
b) Intelligent boost (selective boost) [72]

AVOIDING POWER WASTE WITH INTELLIGENT BOOST CONTROL



- ▲ Intelligent Boost is designed to avoid power waste that results from boosting applications that benefit very little from higher frequency
- ▲ Enables long battery life and cool operation while maintaining great performance
- ▲ Power management micro-controller tracks application behavior real-time to determine frequency sensitivity
- ▲ Boost behavior is adjusted accordingly

Frequency Sensitivity
(i.e. % perf gain for % freq gain)



Performance metrics tracked by power manager

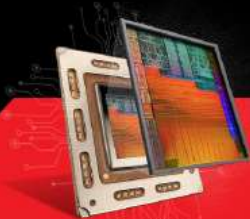
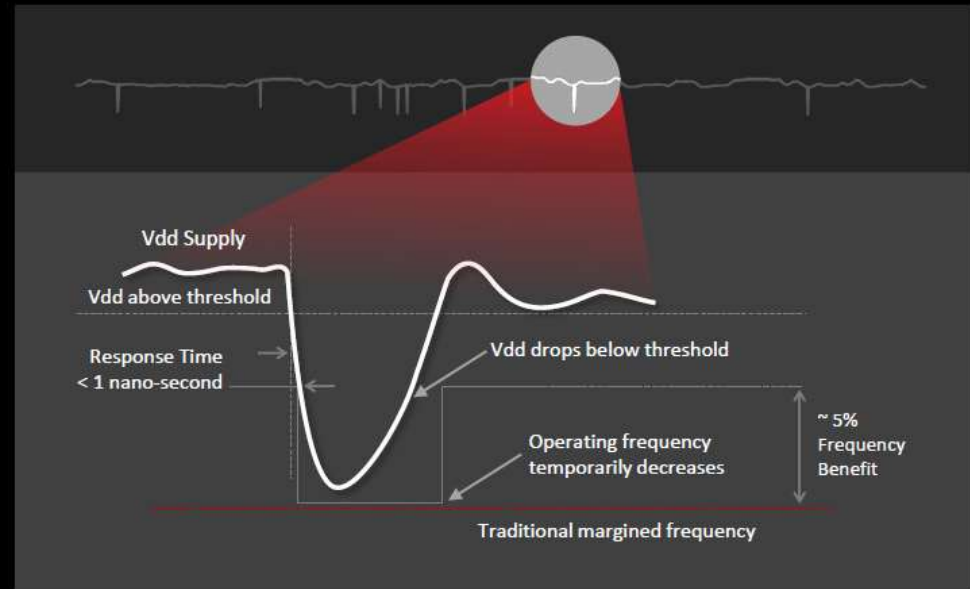
4.3 Enhancements and innovations of the Puma+ based APU lines (10)

c) Adaptive voltage control to encounter short voltage drops [72]

VOLTAGE ADAPTIVE OPERATION



- ▲ CPUs, GPUs and APUs all operate at low voltages with high current – this creates a challenge for power supplies and packages to delivery a quality voltage
- ▲ In fact it's impossible to deliver a perfect voltage, and the variations that happen are often about 10% of the nominal value – that means at least 20% power is wasted covering these voltage variations
- ▲ AMD's unique voltage adaptation feature recovers most of that wasted power by operating at the average voltage and quickly reducing frequency for the brief periods when the voltage reduces



VOLTAGE REDUCTION AT 3.5GHZ IS 50MV-70MV ACROSS TEMPERATURE
→ 10% TO 20% POWER REDUCTION FOR THE SAME PERFORMANCE¹⁴

4.3 Enhancements and innovations of the Puma+ based APU lines (11)

d) Support for ARM TrustZone via integrated Cortex-A5 processor [68]

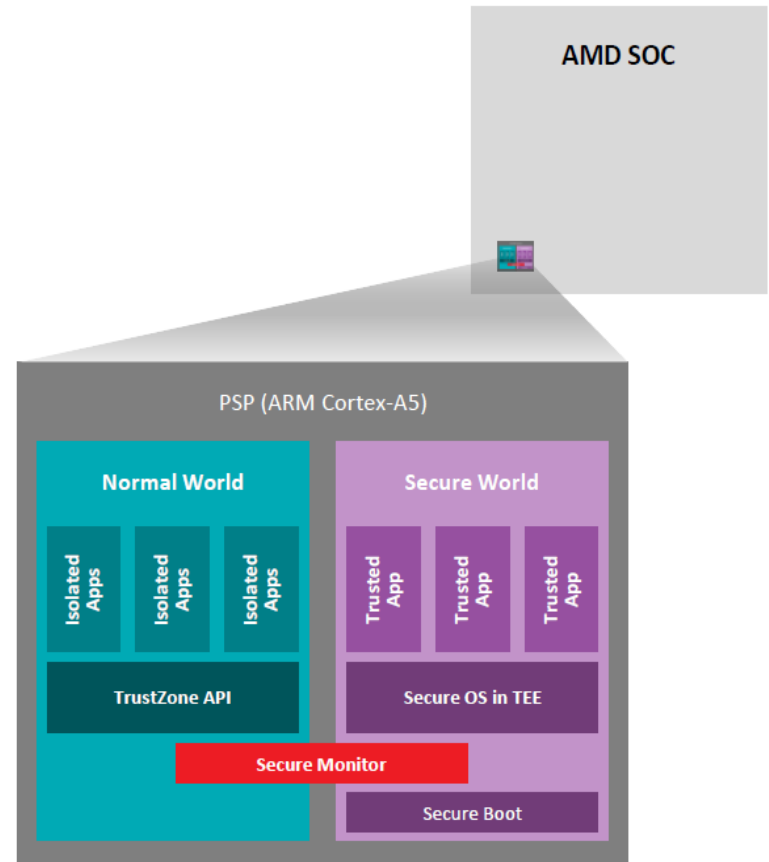
- Mullins and Beema are AMD's first lines to integrate ARM's TrustZone technology to provide enhanced system security.
- This technology is analogous to Intel's Trusted Computing technology.

▲ Provides a Trusted Execution Environment (TEE)

- Protects against software attack from open/rich OS side of system
- Provides scalable environment for secure applications like user authentication, anti-malware, content management, online payments, etc.

▲ Delivers two separate domains, normal and **secure**

- Extends across entire system
- Beyond simply the processor/SOC
- Can deliver secure
 - Processing data path
 - On/off-chip memory
 - I/O and display



New features

Turbo Core: AMD's Kabini and Temash could reduce their own clock speeds to save power but didn't have a Turbo Mode for additional performance in single-threaded workloads. Beema and Mullins both add this capability to certain chips — Beema, the notebook processor, can burst up to 2.4GHz while Mullins, the tablet SoC, can ramp as high as 2.2GHz.

ARM TrustZone: Mullins and Beema are the first AMD processors to integrate a Cortex-A5 on-die for additional system security and management. TrustZone is analogous to Intel's Trusted Computing technology — ARM's own website says that the feature is analogous to the Intel standard. This is essentially a corporate or government-oriented feature; there doesn't seem to be much consumer software that actually uses the TrustZone system.

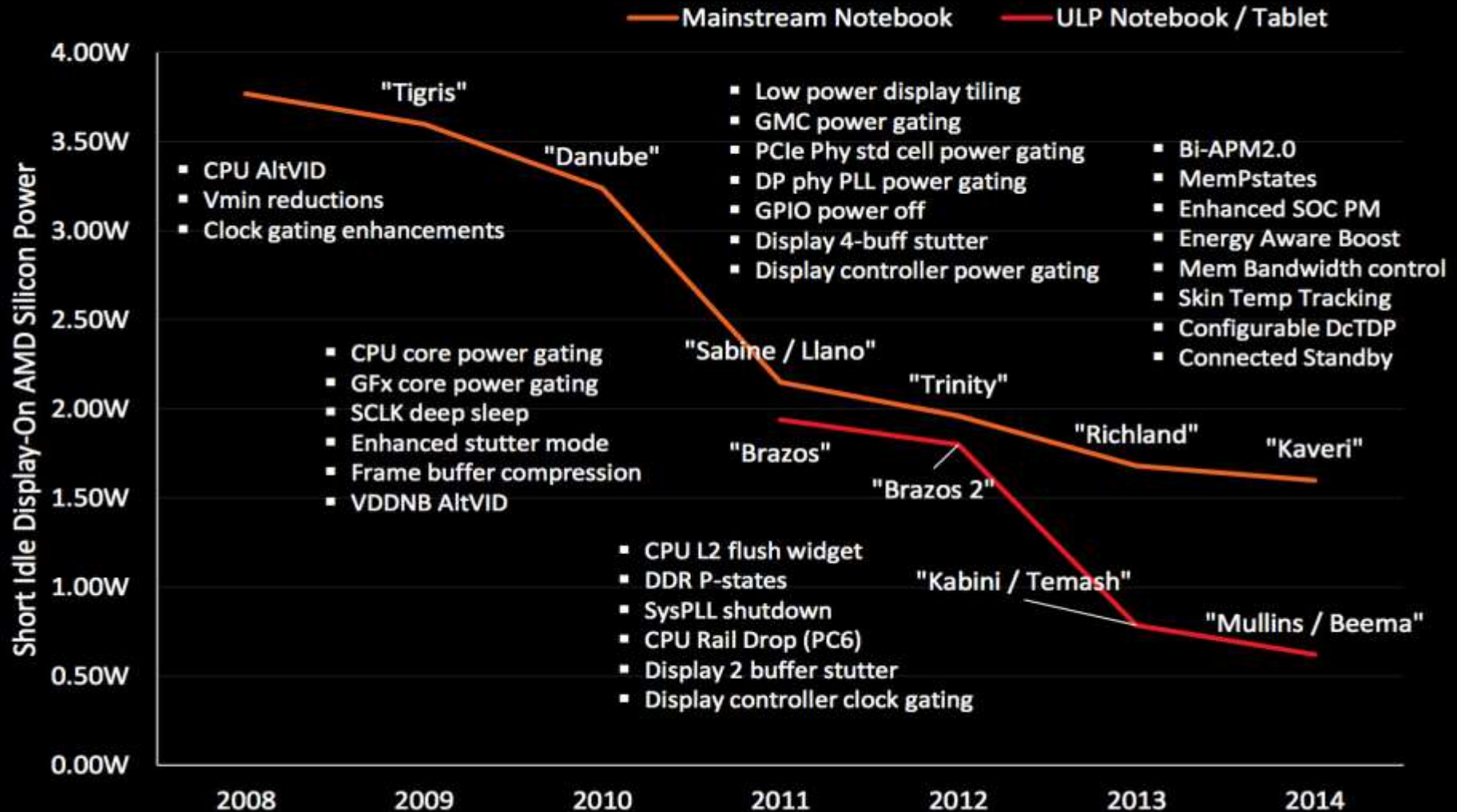
Reduced leakage: AMD claims that it's reduced leakage current loss by 19% in Mullins as compared to Kabini. This isn't the same thing as reducing total power consumption, but it should still have a measurable impact. The on-board GPU has improved even more; Beema and Mullins have 38% reduced leakage compared to Kabini/Temash.

A number of additional improvements were made to reduce power consumption in other areas — the display controller now draws less power when using DisplayPort and low-power DDR optimizations allowed AMD to reduce memory controller power consumption by 600mV compared to standard DDR modules.

New power management: This ties into the Turbo Core feature but is distinct enough to deserve its own mention. According to AMD, Beema and Mullins will include the ability to directly measure the skin temperature of the laptop or tablet and will adjust frequency based on how warm the chassis is — not just according to their own T_{max}. Because heat dissipates out to the chassis rather slowly, AMD can therefore run their cores at a higher frequency for a longer period of time. According to AMD, T_{skin} will be a user definable variable (it's not clear how this capability will be exposed in software).

4.3 Enhancements and innovations of the Puma+ based APU lines (12)

Power management techniques introduced by AMD and improvements achieved both in their mainstream and mobile lines [69]



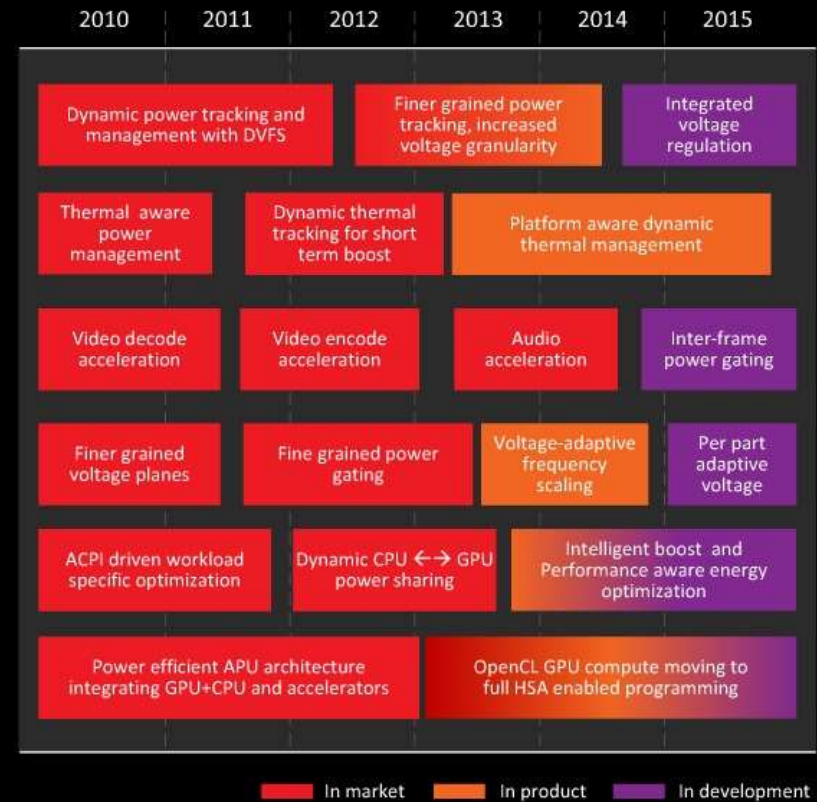
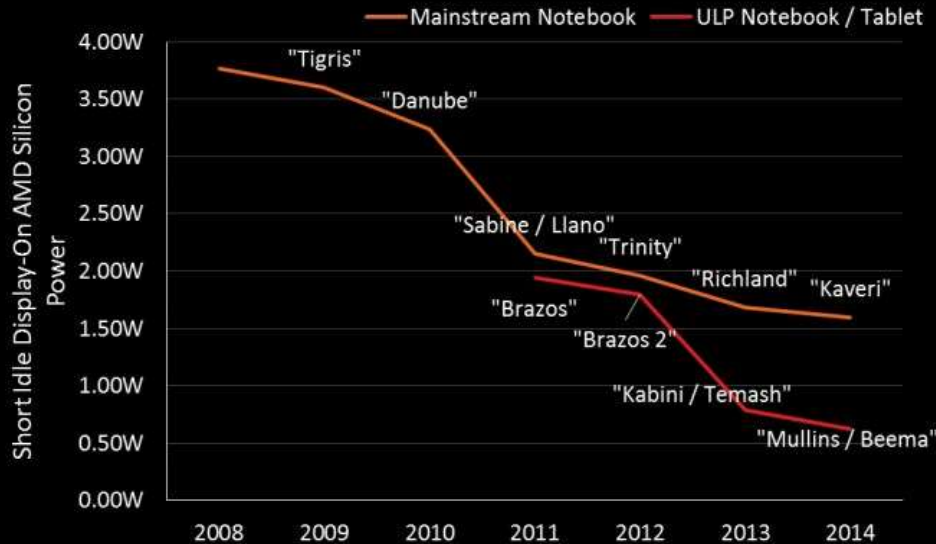
4.3 Enhancements and innovations of the Puma+ based APU lines (13)

Power management techniques in development by AMD [73]

MULLINS/BEEMA FEATURES ARE JUST THE TIP OF THE ICEBERG



- ▲ AMD has been building a pipeline of power focused IP for many years
- ▲ Watch for more leading edge innovations enabling accelerated power gains in the future













4.4 The Beema notebook line

4.4 The Beema notebook line

Launched in 04/2014.

4.4 The Beema notebook line (2)

Announcing the Puma+ based Beema notebook line in AMD's 2013-2014 mobile roadmap in 11/2013 [68]

	2013	2014
Performance	<p>"Richland" APU 2-4 "Piledriver" CPU Cores 2nd Generation DX®11 GPU Cores 17W-35W</p> 	<p>"Kaveri" APU 2-4 "Steamroller" CPU Cores GCN Graphics Compute Units HSA Features AMD TrueAudio 15W-35W</p> 
Mainstream	<p>"Kabini" APU 2-4 "Jaguar" CPU Cores GCN Graphics Compute Units 15W-25W</p>  	<p>"Beema" APU 2-4 "Puma" CPU Cores GCN Graphics Compute Units AMD Security Processor 10W-25W</p>  
Low-Power Essential	<p>"Temash" APU 2-4 "Jaguar" CPU Cores GCN Graphics Compute Units 3W-4W SDP</p>  	<p>"Mullins" APU 2-4 "Puma" CPU Cores GCN Graphics Compute Units AMD Security Processor ~2W SDP</p>  
Ultra-Low Power		

AMD roadmaps are subject to change without notice or obligations to notify of changes. Placement of boxes intended to represent first year of production shipments

4.4 The Beema notebook line (3)

Key features of the Beema notebook line [67]

UNMATCHED FEATURE SET



- ▲ Puma+ x86 Cores
- ▲ Graphics Core Next (GCN)
- ▲ System-Aware Power Management
- ▲ Platform Security Processor
- ▲ DDR3-1866 memory support
- ▲ Over 50% more frequency at nearly half the TDP of the previous generation ²



4.4 The Beema notebook line (4)

Main features of the Beema notebook line [74]

Family	Model	Socket	CPU				GPU		TDP	Memory
			Cores	Frequency	Max. Turbo	L2 Cache	Model	Max. Freq.		
A8	6410	Socket FT3b	4	2.00 GHz	2.4 GHz	2 MB	Radeon R5	800 MHz	15 W	DDR3L-1866
A6	6310			1.80 GHz			Radeon R4	800 MHz		
A4	6250J			2.00 GHz	Radeon R3		600 MHz	25 W		
A4	6210		1.80 GHz	N/A	Radeon R3	600 MHz	15 W	DDR3L-1600		
E2	6110		1.50 GHz		Radeon R2	500 MHz				
E1	6010		1.35 GHz			350 MHz	10 W		DDR3L-1333	
				2			1 MB			

4.4 The Beema notebook line (5)

Positioning AMD's Beema notebook processors vs. Intel's corresponding processors [67]

POSITIONING BACKED BY PERFORMANCE VS. COMPETITION



2014

**AMD A6-6310 APU
with Radeon™ R4 Graphics**

15W TDP

778 / 1923 / 22

**Pentium 3556U
"Haswell U"**

518 / 1974 / 3

**AMD A4-6210 APU
with Radeon™ R3 Graphics**

703 / 1817 / 21

**Pentium N3510
"Bay Trail M"**

233 / 1331 / 5

**AMD E2-6110 APU
with Radeon™ R2 Graphics**

614 / 1712 / 19

**Celeron N2820
"Bay Trail M"**

209 / 1212 / 5

**AMD E1-6010 APU
with Radeon™ R2 Graphics**

438 / 1466 / 15

**Celeron N2805
"Bay Trail M"**

199 / 937 / 5

3DMark 11 Performance

PCMark 8 Home

Basemark CL

- ▲ AMD A6-6310 gives 50% better GRAPHICS PERFORMANCE than "Haswell U" Pentium¹⁷
- ▲ And 7X the COMPUTE PERFORMANCE of "Haswell U" Pentium¹⁸
- ▲ A4 -6210 delivers 3X the GRAPHICS PERFORMANCE of "Bay Trail M" Pentium¹⁹
- ▲ And over 35% better COMPUTE PERFORMANCE than "Bay Trail M" Pentium²⁰



3DMark11 for Graphics Performance

Basemark CL

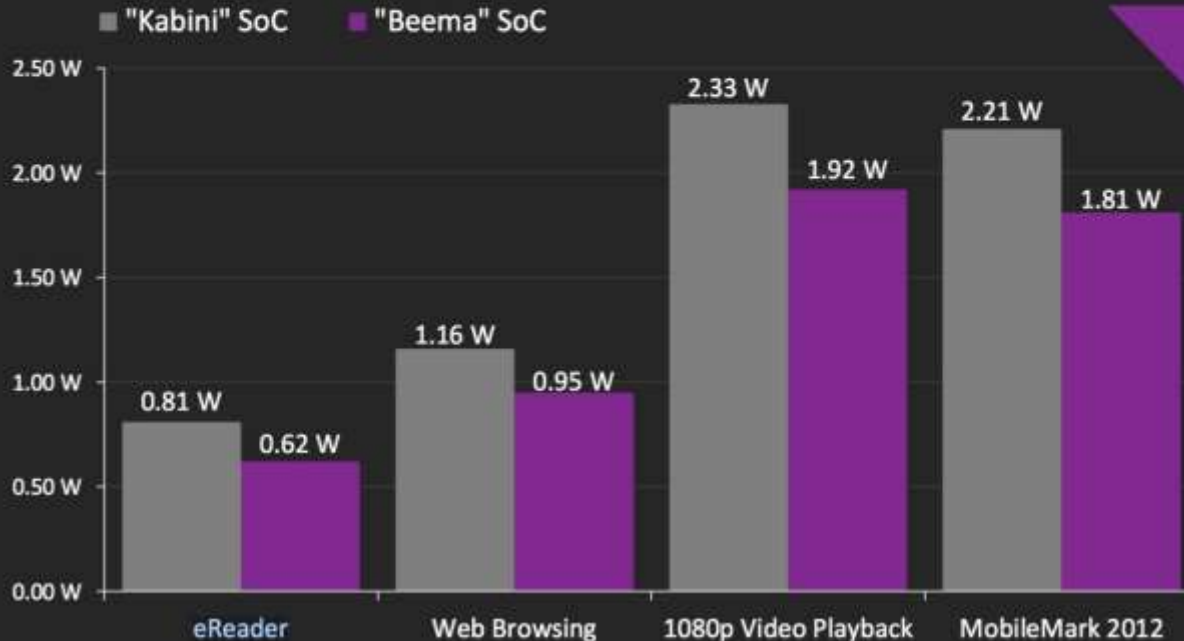
4.4 The Beema notebook line (6)

Power improvements of the Beema line vs. the preceding Kabini line [69]

REDUCED POWER CONSUMPTION, MORE BATTERY LIFE
GENERATION OVER GENERATION



"BEEMA" POWER IMPROVEMENTS



Up to 20%
POWER REDUCTION ²¹

4.5 The Mullins tablet line











4.5 The Mullins tablet line (1)

4.5 The Mullins tablet line

Launched in 04/2014.

4.5 The Mullins tablet line (2)

Announcing the Puma+ based Mullins tablet line in AMD's 2013-2014 mobile roadmap in 11/2013 [68]

	2013	2014
Performance	<p>"Richland" APU 2-4 "Piledriver" CPU Cores 2nd Generation DX[®]11 GPU Cores 17W-35W</p> 	<p>"Kaveri" APU 2-4 "Steamroller" CPU Cores GCN Graphics Compute Units HSA Features AMD TrueAudio 15W-35W</p> 
Mainstream	<p>"Kabini" APU 2-4 "Jaguar" CPU Cores GCN Graphics Compute Units 15W-25W</p>  	<p>"Beema" APU 2-4 "Puma" CPU Cores GCN Graphics Compute Units AMD Security Processor 10W-25W</p>  
Low-Power Essential	<p>"Temash" APU 2-4 "Jaguar" CPU Cores GCN Graphics Compute Units 3W-4W SDP</p>  	<p>"Mullins" APU 2-4 "Puma" CPU Cores GCN Graphics Compute Units AMD Security Processor ~2W SDP</p>  

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4.5 The Mullins tablet line (3)

Main features of the Mullins tablet line [74]

Family	Model	CPU				GPU		Power		Memory
		Cores	Frequency	Max. Turbo	L2 Cache	Model	Max. Freq.	TDP	SDP	
A10 Micro	6700T	4	1.2 GHz	2.2 GHz	2 MB	Radeon R6	500 MHz	4.5 W	2.8 W	DDR3L-1333
A6 Micro	6500T			1.8 GHz		Radeon R4	401 MHz			
A4 Micro	6400T		1.0 GHz	1.6 GHz		Radeon R3	350 MHz			
E1 Micro	6200T	2		1.4 GHz	1 MB	Radeon R2	300 MHz	3.95 W	DDR3L-1066	

4.5 The Mullins tablet line (4)

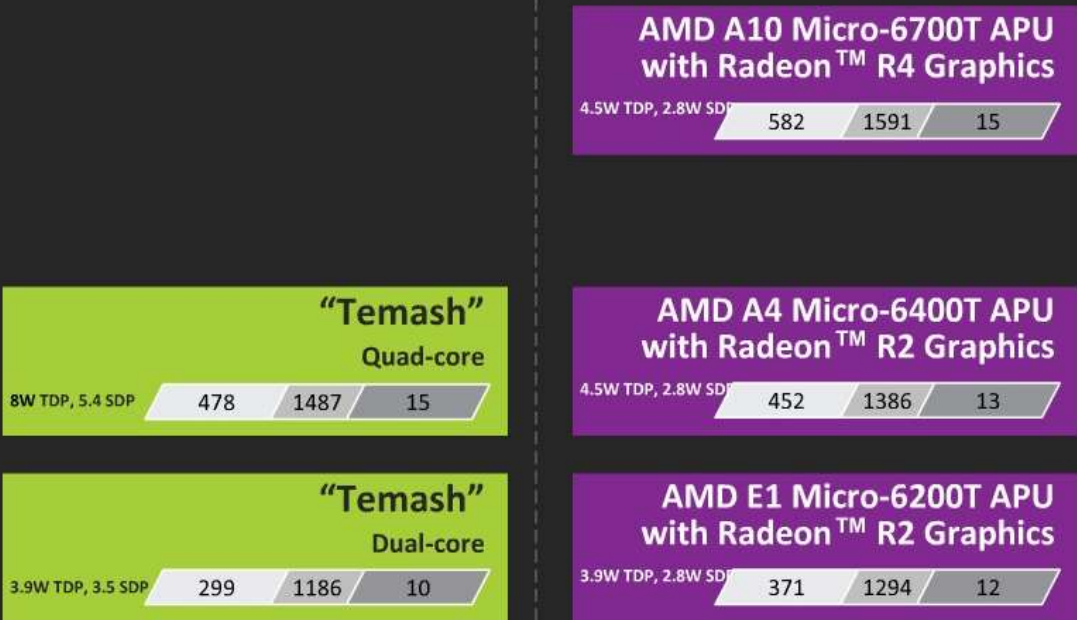
Positioning AMD’s Mullins tablet processors vs. the previous Temash processors [67]

GENERATION VS. GENERATION, TOP OF STACK COMPARISON*

2013

2014

AMD A10 Micro-6700T vs. AMD A6-1450



Over 2X THE GRAPHICS PERFORMANCE PER WATT OF “TEMASH”¹²

3DMark11

NEARLY 2X THE SYSTEM PRODUCTIVITY PER WATT OF “TEMASH”¹³

PCMark 8 – Home v2

3DMark 11 Performance

PCMark 8 Home

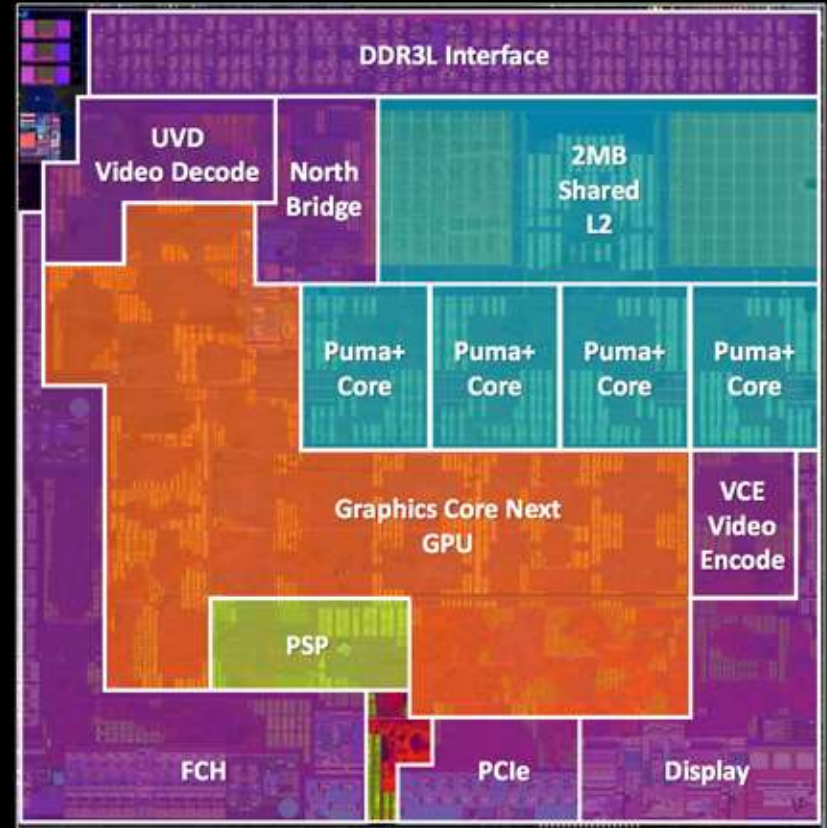
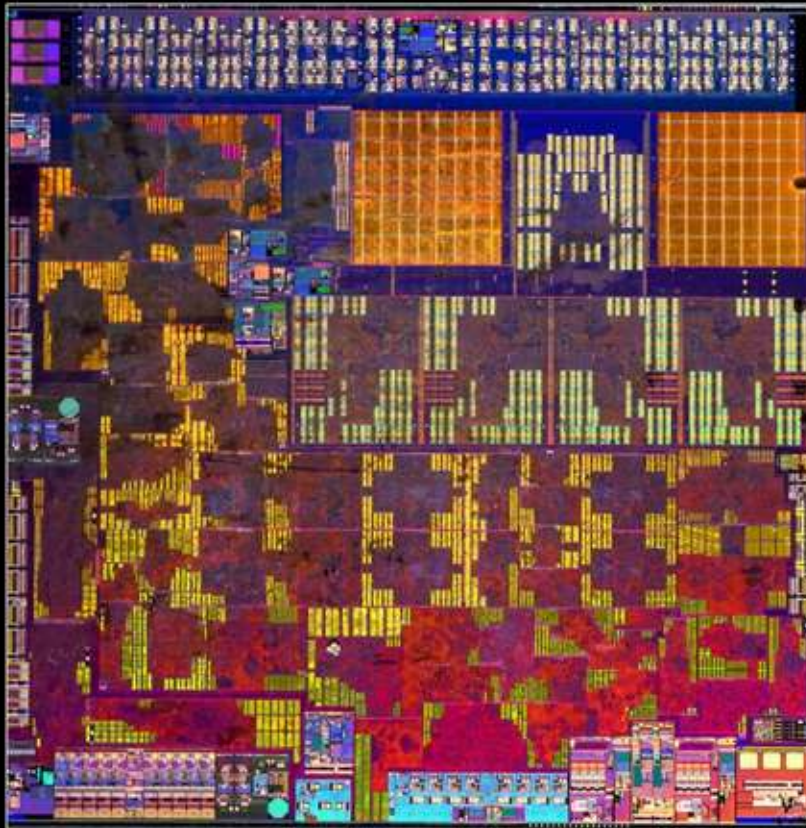
Basemark CL

As seen, the new Mullins processors provide higher performance for substantially lower power (4.5 W vs. 8 W) or substantially higher performance for the same power (3.9 W).

4.5 The Mullins tablet line (5)

Die shot and floorplan of the Mullins tablet processor [73]

MULLINS

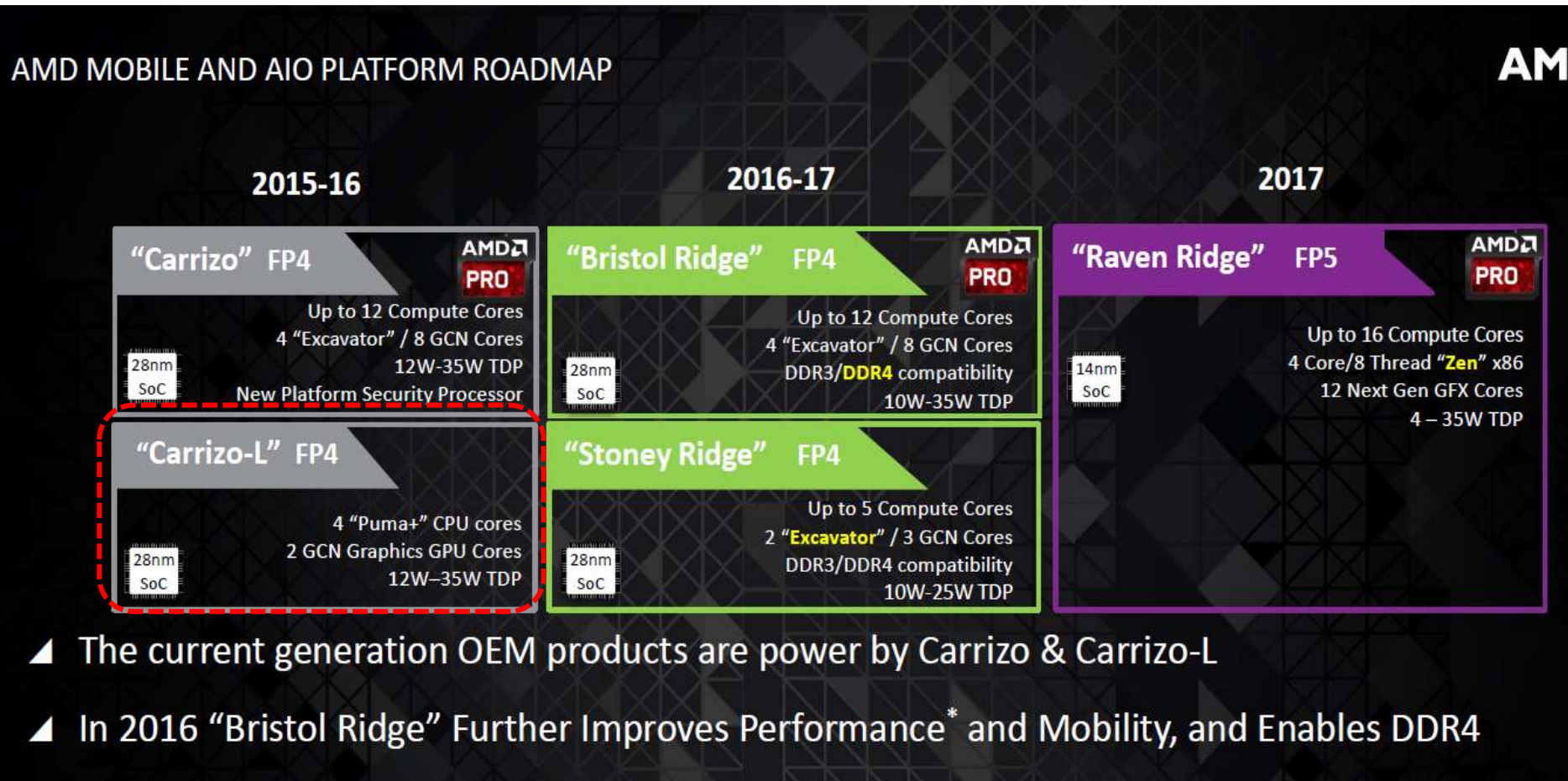


4.6 The last processor based on the Puma+ core: the Carrizo-L APU line

4.6 The last processor based on the Puma+ core: the Carrizo-L APU line (1)

4.6 The last processor based on the Puma+ core: the Carrizo-L APU line -1

As seen in AMD's Mobile and AIO platform roadmap for 2015 – 2017 Carrizo-L is AMD's last processor based on the Cat line, actually on the Puma+ core. [75] [76]



4.6 The last processor based on the Puma+ core: the Carrizo-L APU line (2)

The last processor based on the Puma+ core: the Carrizo-L APU line -2

- The Carrizo-L line was launched in 05/2015.
- It is based on the same Puma+ CPU core as the previous Beema notebook line.
- There are no significant improvements vs. the previous Beema line, max. clock frequencies are only 5 -10 % higher.

4.6 The last processor based on the Puma+ core: the Carrizo-L APU line (3)

Key features of the Carrizo-L notebook processor line [76]

"CARRIZO-L"
GREAT PERFORMANCE AT AN UNBELIEVABLE VALUE



"CARRIZO-L"
MORE PERFORMANCE AND FEATURES FOR MAINSTREAM PCS

- ▲ WORK with Great Battery Life
- ▲ THIN & LIGHT Mainstream Platforms
- ▲ The BEST User Experiences

Up to 4 CPU Cores with GCN

AMD Perfect Picture

AMD Start Now Technology

Ready for Windows 10

AMD PERFECT PICTURE WITH AMD STEADY VIDEO

AMD RADEON™ R-SERIES GRAPHICS

AMD START NOW TECHNOLOGY

AMD RADEON™ R-SERIES GRAPHICS

AMD SECURE TECHNOLOGY

AMD ENDURO TECHNOLOGY

AMD WIRELESS DISPLAY

15

4.6 The last processor based on the Puma+ core: the Carrizo-L APU line (4)

Main features of the processors of the Carrizo-L line [77]

AMD Carrizo-L					
	A8-7410	A6-7310	A4-7210	E2-7110	E1-7010
Cores / Threads	4 / 4	4 / 4	4 / 4	4 / 4	2 / 2
CPU Frequency	Up to 2.5 GHz	Up to 2.4 GHz	Up to 2.2 GHz	Up to 1.8 GHz	Up to 1.5 GHz
TDP	12-25W	12-25W	12-25W	12-15W	10W
L2 Cache	2MB	2MB	2MB	2MB	1MB
DRAM Frequency	DDR3L-1866	DDR3L-1600	DDR3L-1600	DDR3L-1600	DDR3L-1333
Radeon Graphics	R5	R4	R3	'Radeon'	'Radeon'
GPU Frequency	Unknown	Unknown	Unknown	Unknown	Unknown

5. AMD's withdrawal from the mobile market

5. AMD's withdrawal from the mobile market (1)

5. AMD's withdrawal from the mobile market

Sail statistics of application processors to be incorporated in smartphones and notebooks (see below) reveal that no traditional processor or graphics card firms, including Intel, AMD or NVIDIA could achieve a favorable market position in worldwide sales.

Smartphone application processors worldwide market share 2015 (revenue)	
Qualcomm (USA)	42 %
Apple (USA)	21 %
MediaTek (Taiwan)	19 %
Samsung (S. Korea)	
Spreadtrum (China)	

Tablet application processors worldwide market share 2015 (revenue)	
Apple (USA)	31 %
Qualcomm (USA)	16 %
Intel (USA)	14 %
MediaTek (Taiwan)	
Samsung (S. Korea)	

[Source: Related press releases of Strategy Analytics]

Worldwide market share of smartphone and tablet application processors in 2015 (based on revenue) [34]

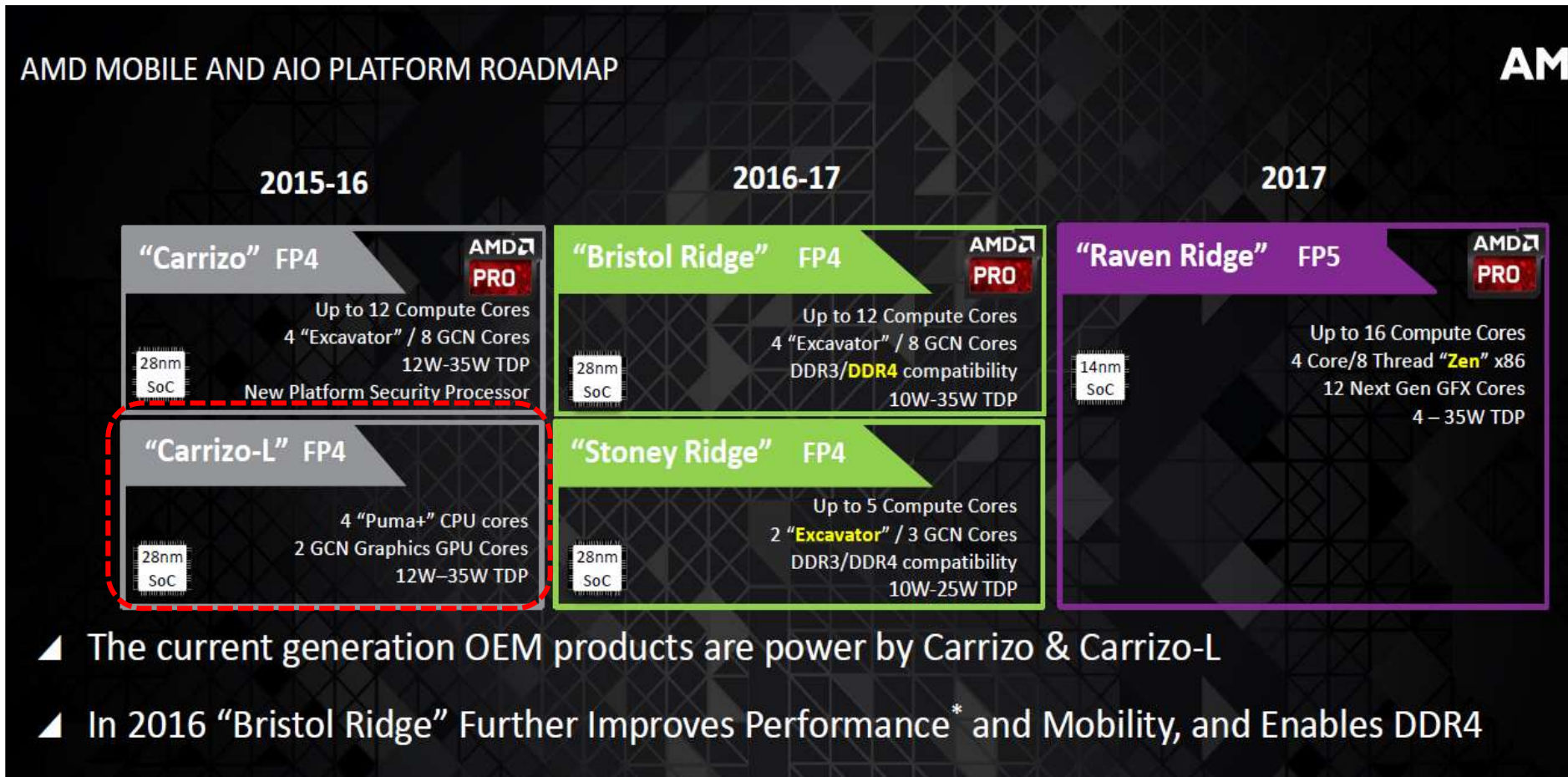
Note that seemingly Intel achieved the 3. place in tablet application processor sales, but this is brought about by paying high subsidies to OEMs for choosing Intel processors what could not long be maintained due to high losses incurred (about 7 billion USD I two years).

As a consequence, all three vendors mentioned have withdrawn from the mobile market in 2015/2016, as shown next.

5. AMD's withdrawal from the mobile market (2)

The last processor based on the Puma+ core: the Carrizo-L APU line -1

As seen in AMD's Mobile and AIO platform roadmap for 2015 – 2017 Carrizo-L is AMD's last processor based on the Cat line, actually on the Puma+ core. [75] [76]



5. AMD's withdrawal from the mobile market (3)

Cancellation of AMD's low-power Cat line in 2015

- Neither Intel nor AMD became successful on the mobile market, so beyond Intel also AMD stopped their activities on this market.
- The last core of AMD's Cat line was the Puma+ core (launched in 6/2015 in the Carrizo-L APU).
- In AMD's 2016 Mobility roadmap there is no sign of an APU powered by the Puma+ core or a derivative of a core belonging to the Cat line, as seen in the next slice.
- Instead AMD placed emphasis on the development of Zen core based products.

5. AMD's withdrawal from the mobile market (4)

Intel's withdrawal from the smartphone and mobil market

- As Intel failed to gain traction in the mobile sector and suffered high losses on the mobile segment the firm announced their **withdrawal from the mobil market** in 4/2016.
- Intel's statement says [78]:

"I can confirm that the changes included canceling the Broxton platform as well as SoFIA 3GX, SoFIA LTE and SoFIA LTE2 commercial platforms to enable us to move resources to products that deliver higher returns and advance our strategy.

These changes are effective immediately."
- At the same time Intel laid off about 12000 employees (~ 11 % of their workforce).

5. AMD's withdrawal from the mobile market (5)

Nvidia's leaving the smartphone and tablet market in June 2016 [79]

- **NVIDIA's** Tegra 4 chips were also not successful, so **the firm announced in 05/2014 that they will abandon the phone market.**

Apple's iPad Air 2 with its A8X processor and its GPU with 256 EUs became a very powerful rival to NVIDIA's subsequent 64-bit K1 chip including a GPU with 192 EUs.

As a consequence, **NVIDIA also gave up their tablet interests.**

- In 6/2016 (at Computex) NVIDIA's CEO declared the firm's leaving the smartphone and tablet market by saying:
“**We are no longer interested in that market**”. He adds, “**Anybody can build smartphones, and we're happy to enjoy these devices, but we'll let someone else build them**”.
- Instead NVIDIA became interested in designing in-car computers and car infotainment systems.

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