Intel's Core 2 family - TOCK lines
The Skylake line

Dezső Sima

Vers. 3.1

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Only Sections 6.1 to 6.3 will be discussed.

6.1 Introduction to the Skylake line

6.1 Introduction to the Skylake line

- The Skylake line is built on 14 nm technology.
- Announced: 08/2015
- Available: 10/2015

Skylake processors are termed also as the 6. gen. Intel Core processors, as indicated below.

*

6.1 Introduction to the Skylake line (2)

The Skylake line -1

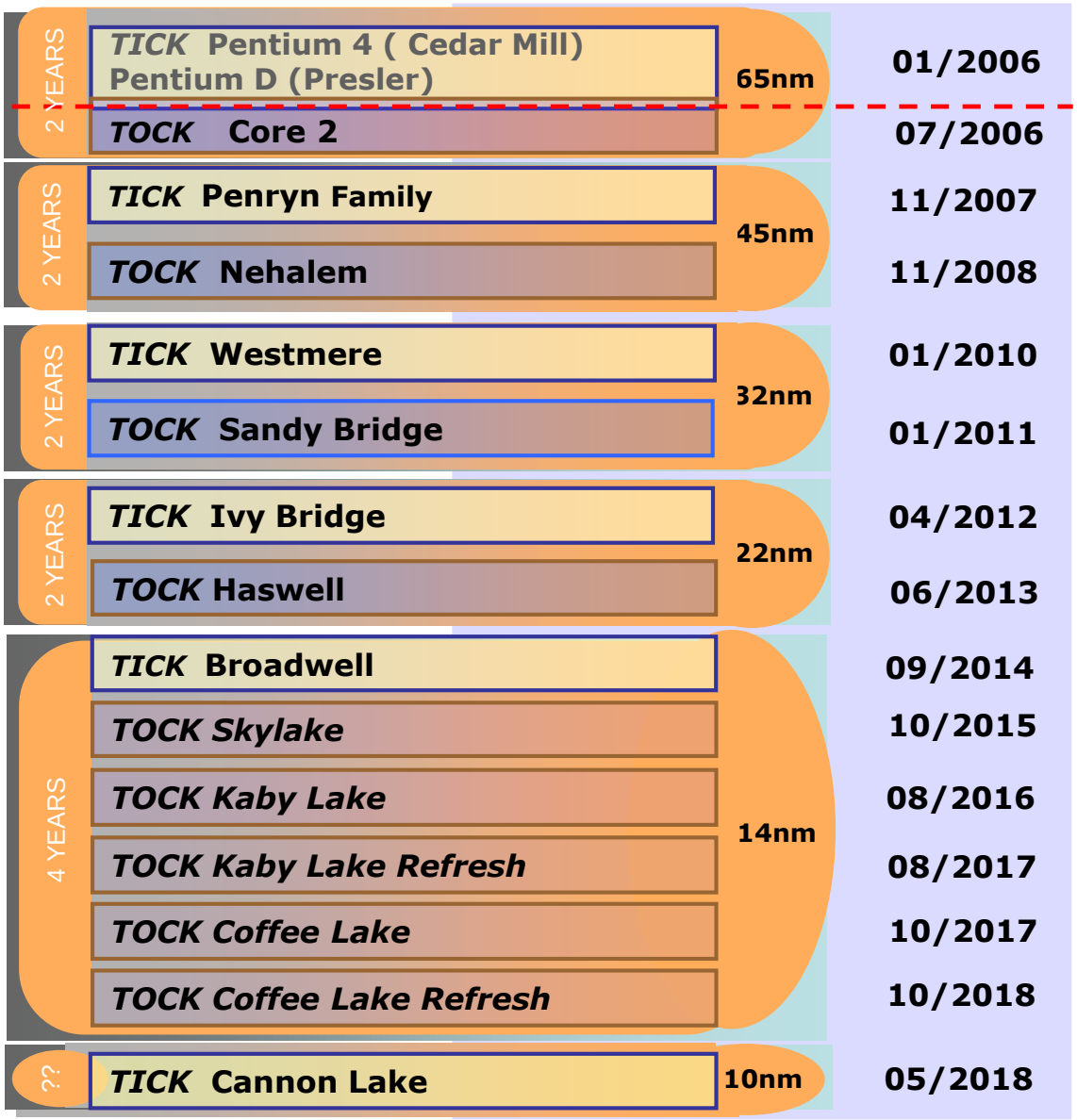
1. gen.				2. gen.	3. gen.	4. gen.	5. gen.
Core 2 New Microarch. 65 nm	Penryn New Process 45 nm	Nehalem New Microarch. 45 nm	West-mere New Process 32 nm	Sandy Bridge New Microarch. 32 nm	Ivy Bridge New Process 22 nm	Haswell New Microarchi. 22 nm	Broad-well New Process 14 nm
TOCK	*TICK*	*TOCK*	*TICK*	*TOCK*	*TICK*	*TOCK*	*TICK*
(2006)	*(2007)*	*(2008)*	*(2010)*	*(2011)*	*(2012)*	*(2013)*	*(2014)*

6. gen.	7. gen.	8. gen.[1]	9. gen.
Skylake New Microarch. 14 nm	Kaby Lake New Microarch. 14 nm	Kaby Lake R KL G-series Coffee Lake Cannon Lake 14/10 nm	Coffee Lake R New Mocroarch. 14 nm
TOCK	*TOCK*	*TOCK*	*TOCK*
(2015)	*(2016)*	*(2017/18)*	*(2018)*

[1]Astonishingly, the 8th generation encompasses four processor lines, as follows:

- Kaby Lake Refresh
- Kaby Lake G with AMD Vega graphics
- Coffee Lake (all 14 nm) and the
- 10 nm Cannon Lake designs [218].

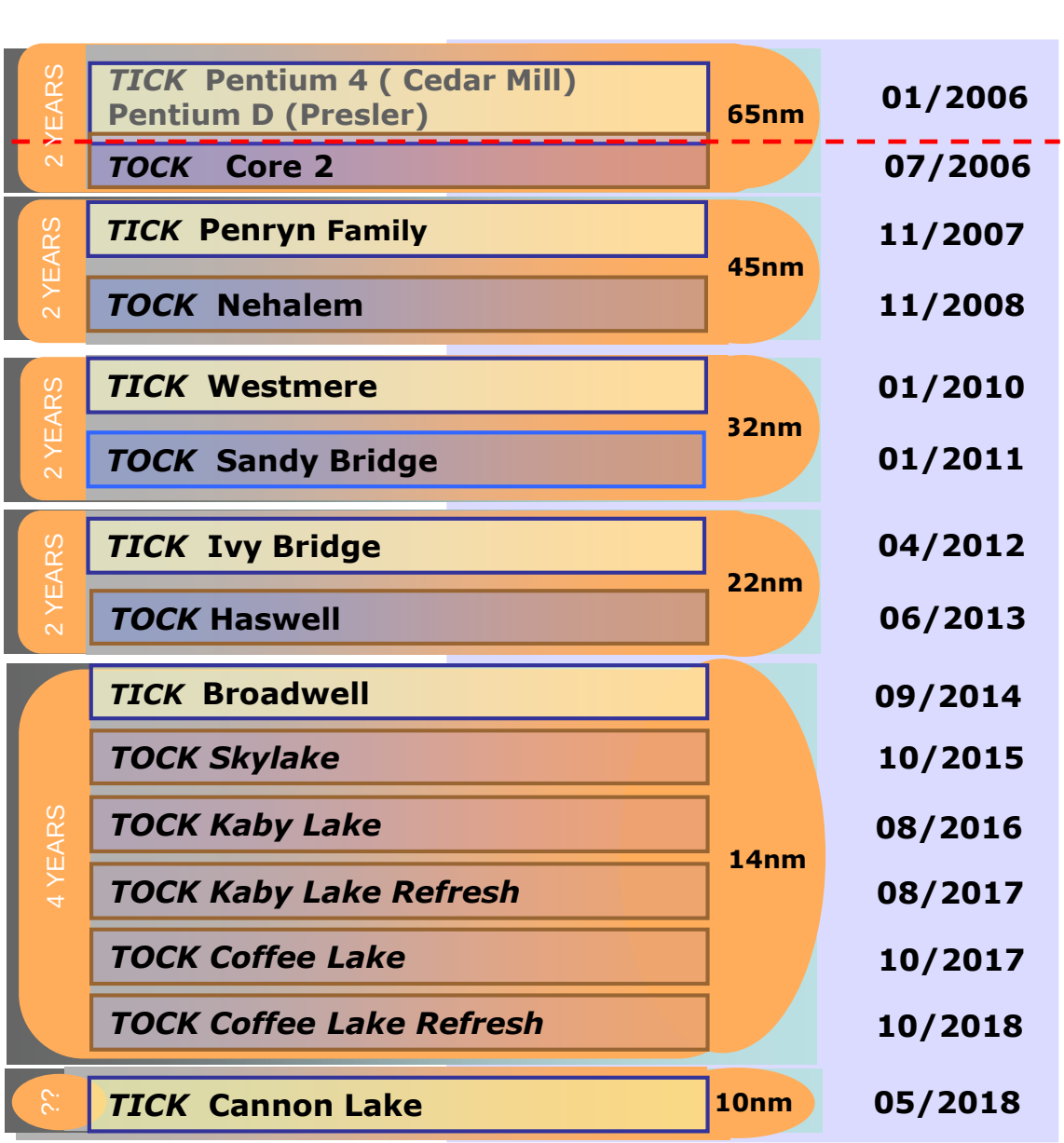
The Skylake line -2 (based on [3]



Key new features of the ISA and the microarchitecture

- New microarch.: 4-wide core, 128-bit SIMD FX/FP EUs, shared L2 , no HT
- New microarch.: 4 cores, integr. MC, QPI, private L2, (inclusive) L3, HT
- In package integrated GPU
- New microarch.: 256-bit (FP) AVX, ring bus, integrated GPU
- New microarch.: 256-bit (FX) AVX2, L4 cache (discrete eDRAM), TSX
- Shared Virtual Memory
- New microarch.: 5-wide core, ISP, Memory Side L4 cache, no FIVR
- Optane memory, in KBL G series: in package integr. CPU, GPU, HBM2
- 6C, (PCHs of S-series DTs support: USB G2, integr. conn., Optane 2)
- 8C
- AVX512

The Skylake line -3 (based on [3])



Key new features of the power management

- Clock gating, PECI, Platform Thermal Control by 3. party controller
- EDAT
- Integrated Power Gates, PCU, Turbo Boost
- Turbo Boost 2.0
- FIVR
- 2. gen. FIVR
- Speed Shift Technology, Duty Cycle control, No FIVR except Skylake X
- Speed Shift Technology v2
- In H-series: TVB (Thermal Velocity Boost)
- STIM

6.1 Introduction to the Skylake line (5)

Performance improvements provided by the Skylake line

According to sources quoting Intel's statements [206] on average, Skylake has 10% better performance, 30% better graphics performance.

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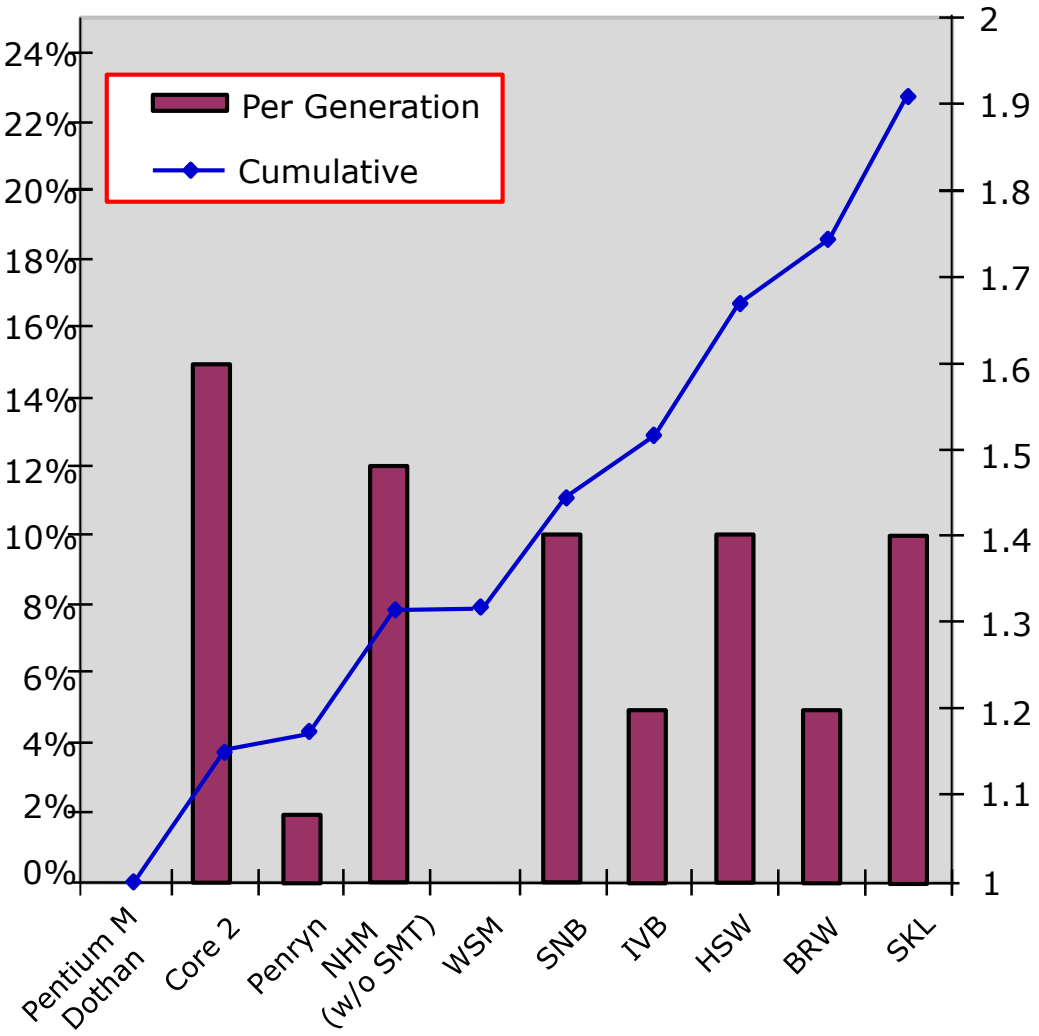
Single thread IPC in Intel's basic architectures (Based on [195])



Note that Intel raised IPC in the Core family only less then 2-times in about 10 years.

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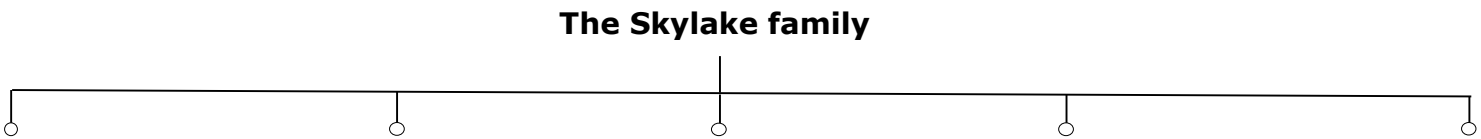
6.1 Introduction to the Skylake line (7)

Skylake-based processor lines



Skylake Mobiles	Skylake Desktops	Skylake-E	Skylake Microservers	Skylake-SP (2S servers)
(SOCs)	(2-chip designs)	(2-chip designs)	(SOCs/2-chip designs)	(2-chip designs)
BGA1515/1356/1440)	LGA1151 100 series PCH	LGA2066 X299 PCH	BGA1440 LGA1151/C230 PCH	LGA3647 C620 series PCH
Up to 4 cores + G m3/m5/m7 designartions i3/i5/i7 designations	Up to 4 cores + G i3/i5/i7 designations	Up to 10 cores i7 designation	4 cores w/without G E3 designation	Up to 28 cores Platinum/Gold/Silver/Bronze designations
(See on a subsequent slide)	(See on a subsequent slide)	(See on a subsequent slide)	(See on a subsequent slide)	(Won't be detailed here)

6.1 Introduction to the Skylake line (8)

The Skylake (6th Gen) mobile and desktop lines - Overview

Mobiles (SoC designs)

4.5 W Core M-line (Y-line) (BGA1515)

Core m7-6Y7x, 2C+HD 515, HT, 10/2015
Core m5-6Y5x, 2C+HD 515, HT, 10/2015
Core m3-6Y3x, 2C+HD 515, HT, 10/2015

15 W U-line (SoC, BGA1356)

Core i7-66x0U/65x0U, 2C+HD 515, HT, 10/2015
Core i5-63x0U/62x0U, 2C+HD 515, HT, 10/2015
Core i3-6100U, 2C+HD 515, HT, 10/2015

28 W U-line (SoC, BGA1356)

Core i7-65x7U, 2C+HD 550, HT, 10/2015
Core i5-62x7U, 2C+HD 550, HT, 10/2015
Core i3-61x7U, 2C+HD 550, HT, 10/2015

45 W HQ/H-lines (BGA1440)

Core i7-6920HQ/6820HQ/6700HQ, 4C+HD 530, HT, 10/2015
Core i5-6440HQ/6300HQ, 4C+HD 530, HT, 10/2015
Core i3-6100H, 2C+HD 530, HT, 10/2015

SoC: System on Chip

6.1 Introduction to the Skylake line (9)

Desktops (2-chip designs, 100 Series chipset)

35 W S-lines (LGA 1151)

Core i7-6700T 4C+HD 530, HT, 10/2015
Core i5-6600T/6500T/6400T, 4C+HD 530, HT, 10/2015
Core i3-6300T/6100T, 2C+HD 530, HT, 10/2015

65 W S-lines (LGA 1151)

Core i7-6700, 4C+HD 530, HT, 10/2015
Core i5-6600/6500/6400 4C+HD 530, HT, 10/2015
Core i3-6320/6300/6100, 2C+HD 530, HT, 10/2015

91 W S-lines, unlocked (LGA1151)

Core i7-6700K/6600K, 4C, HT, 8/2015

HEDs (2-chip designs, X299 PCH)

140 W X-line, unlocked (LGA2066)

Core i7-7800X/7820X/7900X, 10C, HT, 6/2017

6.1 Introduction to the Skylake line (10)

Microservers

25 W v5-lines (LGA 1151)

Xeon E3-1240L v5, 4C, HT, 10/2015
Xeon E3-1235L v5, 4C+HD P530, HT, 10/2015

25 W v5-lines (BGA 1440)

Xeon E3-1505L v5, 4C+HD P530, HT, 10/2015

45 W v5-lines (LGA 1151)

Xeon E3-1260L v5, 4C, HT, 10/2015

45 W v5-lines (BGA 1440)

Xeon E3-1505M/1535M v5, 4C+HD P530, HT, 10/2015
Xeon E3-1545M/1575M v5, 4C+HD P580, HT, 1/2016

80 W v5-lines (LGA1151)

Xeon E3-12x0L v5, 4C, HT, 10/2015
Xeon E3-12x5L v5, 4C+HD P530, HT, 10/2015

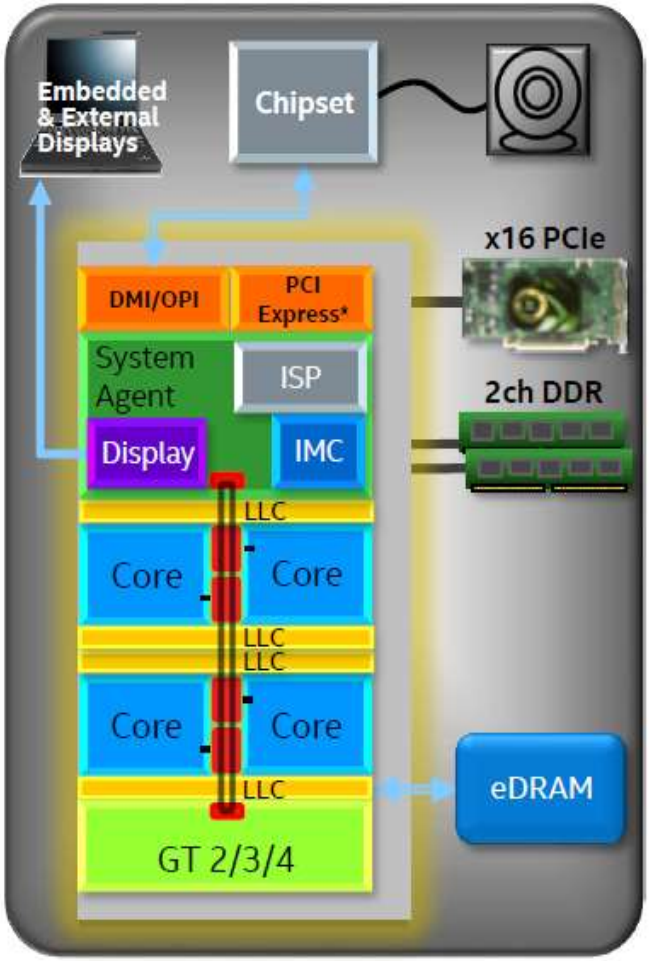
Main enhancements and innovations of Intel's Skylake microarchitecture [200]

Increased chipset I/O throughput, Tablet I/Os, Audio DSP Upgrade, Sensor Hub

Higher resolution display

Bigger/wider core, better instruction per clock, improved power efficiency

Enhanced ring/LLC for improved throughput



Integrated camera ISP

Extended overclocking capabilities

Faster DDR Memory

Advanced Processor Graphics GT3 + eDRAM, GT4 + eDRAM; OpenCL™ 2.0 API, DirectX® 12, OpenGL* 4.4

ISP: Image Signal Processor

This diagram shows a kind of "superset" of Skylake. Different versions will not include all of these parts, but these are all the different components that can be included.

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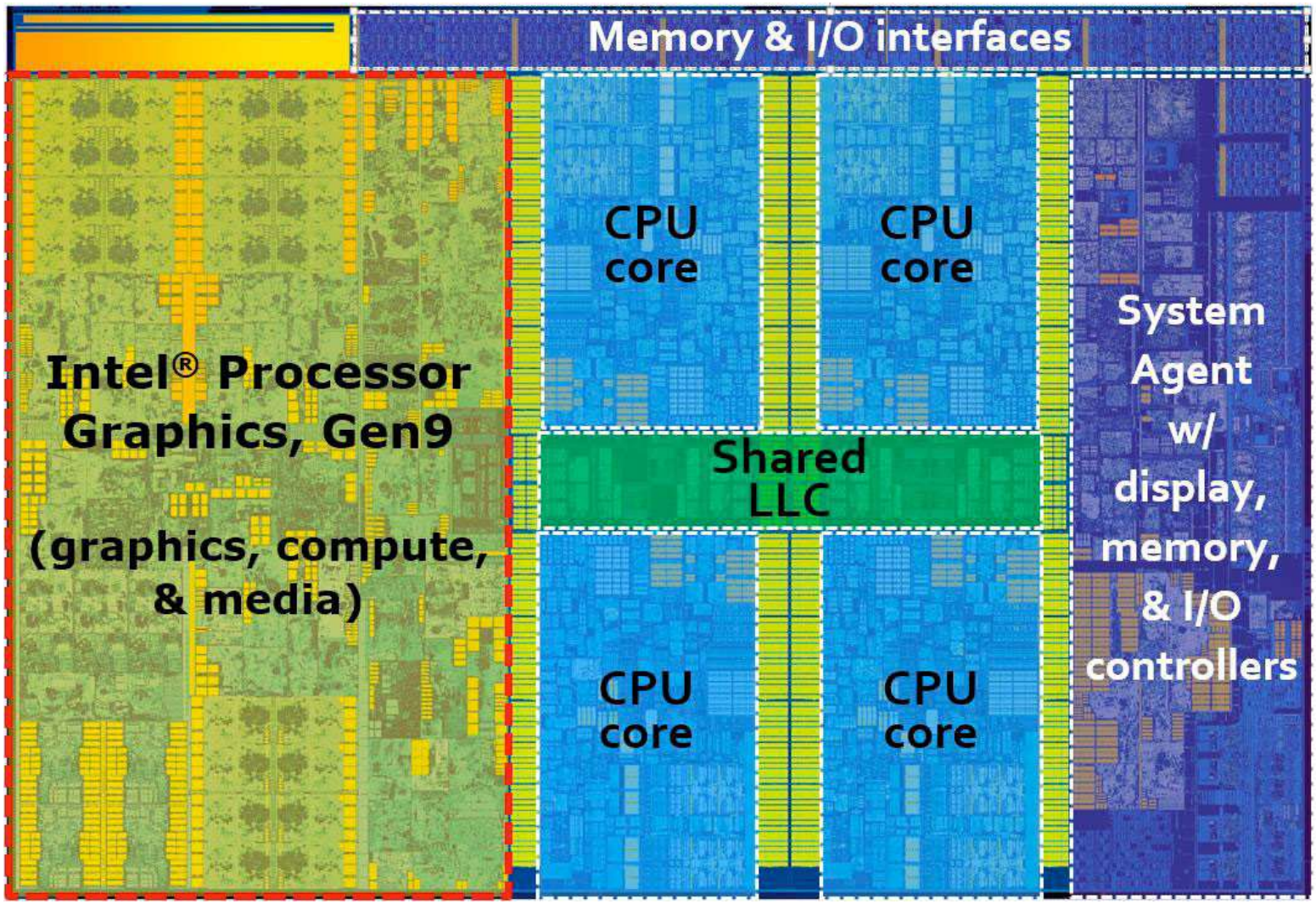
The Skylake die [208]



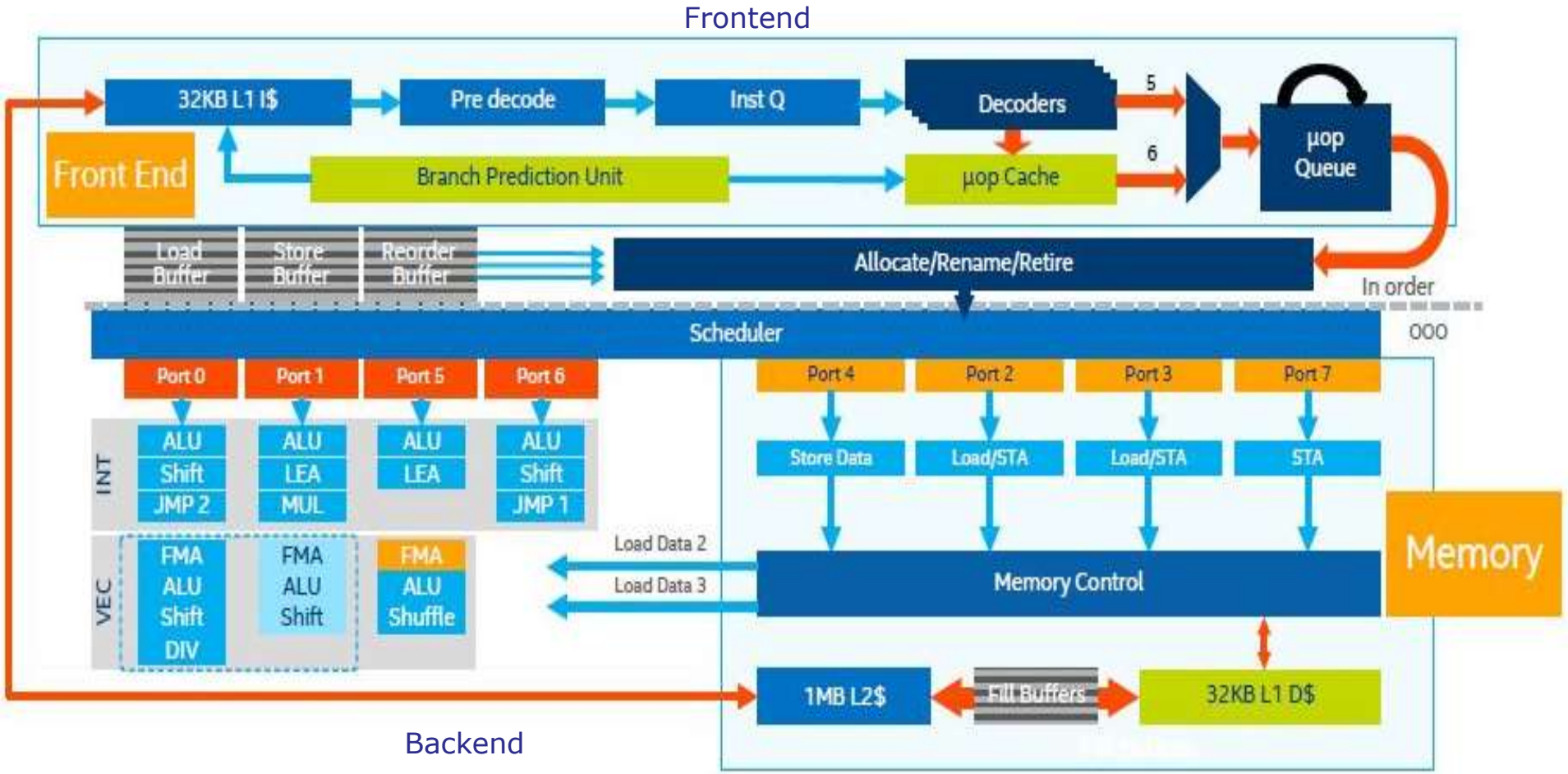
6.2 Major enhancements of the Skylake line

- 6.2.1 More advanced microarchitecture of the cores
- 6.2.2 Enhanced graphics
- 6.2.3 Support of PCIe 3.0

Enhancement: Továbbfejlesztés

6.2 Major enhancements of the Skylake line

6.2.1 More advanced microarchitecture of the cores [239]



Note

The Skylake core is basically a master superset (see above) core with two derivatives:

- the server core (supporting e.g. AVX-512) and
- the client core.

6.2.1 More advanced microarchitecture of the cores (1)

Key improvements of the microarchitecture of the cores

- 5-wide decoding (vs. 4 previously)
- larger buffer and register sizes (as detailed subsequently).

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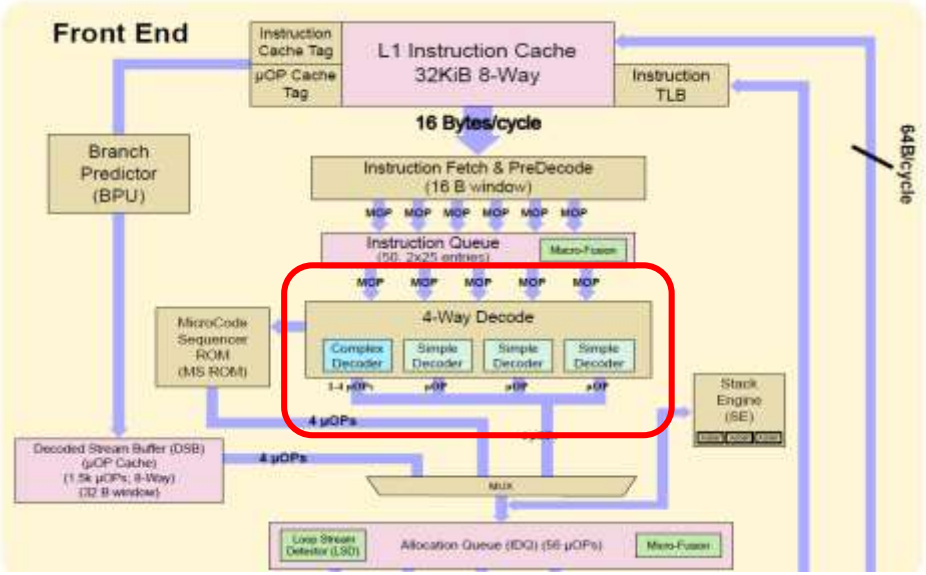
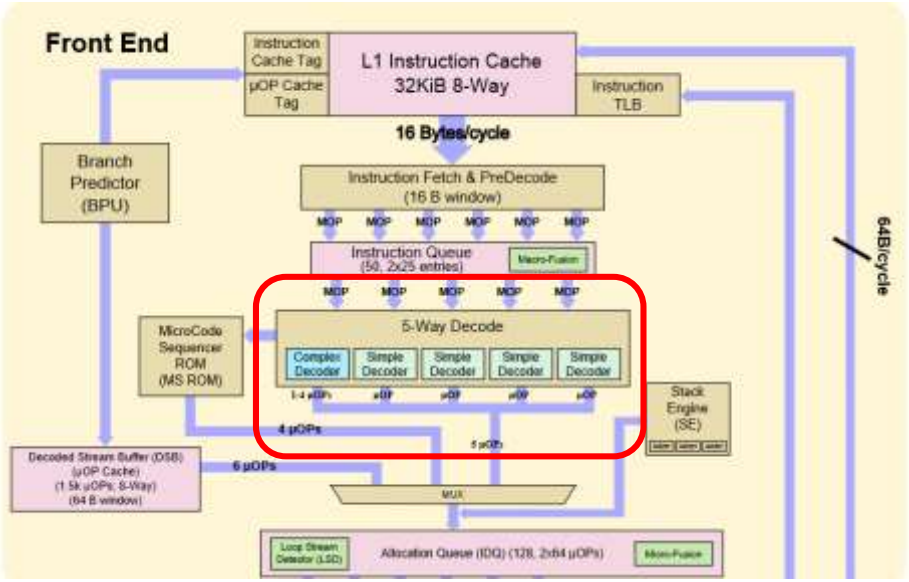
6.2.1 More advanced microarchitecture of the cores (2)

5-wide decoding -1



Broadwell's frontend [241]



Skylake's frontend [240]

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5-wide decoding -2

With 5-wide decoding the front-end becomes also 5-wide, as shown below.

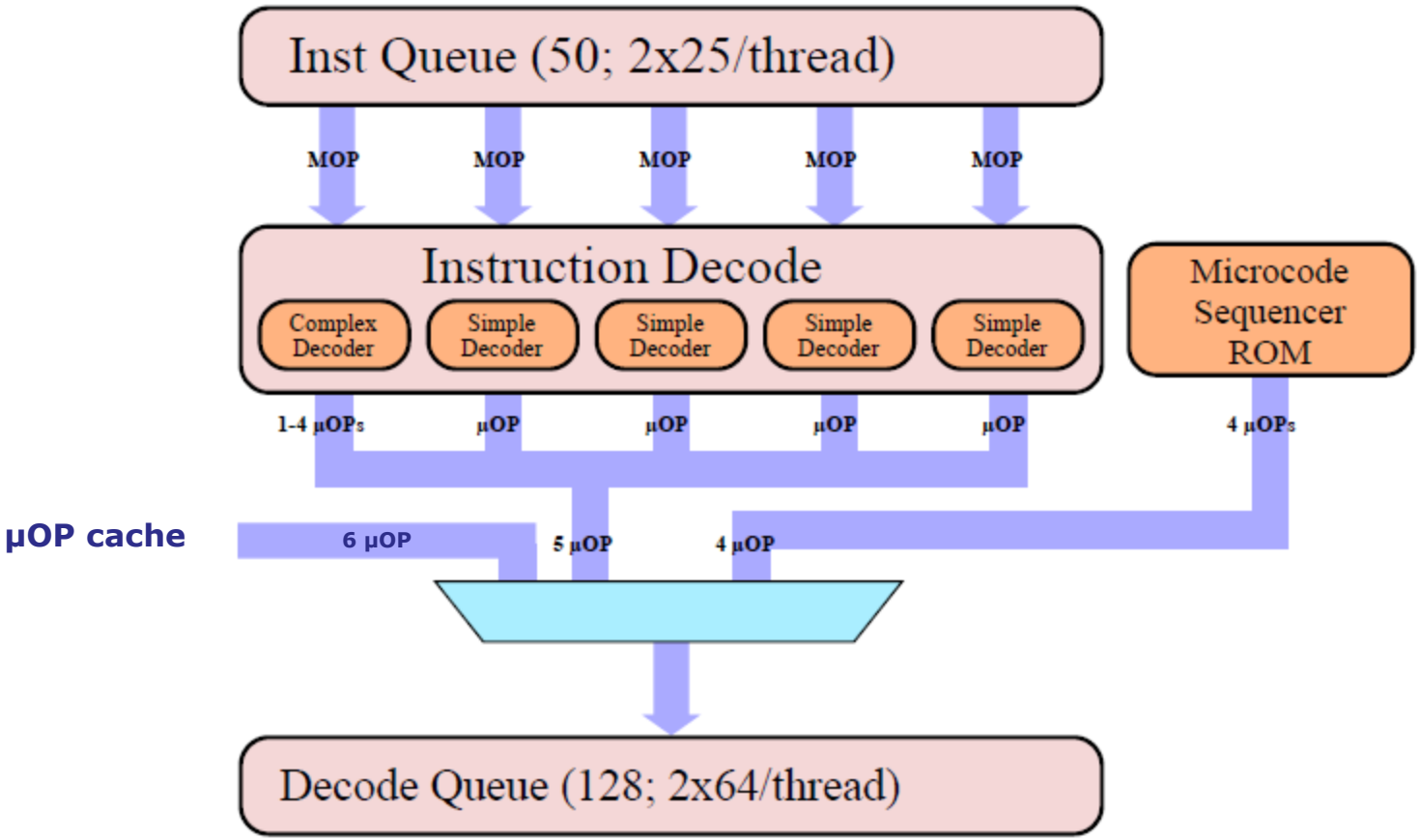

Figure: Decoding in Skylake's core [240]

https://en.wikichip.org/wiki/intel/microarchitectures/skylake_(client)

*

5-wide decoding -3

Front-end width in Intel's microarchitectures

- Up to the Pentium 4 (2000): 3-wide
- Beginning with the Core 2 (2006): 4-wide
- Beginning with the Skylake (2015): 5-wide

As illustration see the next Figures.

Remark

Also AMD's highly successful K7 Athlon microarchitecture (1999) had a front-end width of 3, subsequently, AMD switched only quite late to a 4-wide microarchitecture along with their K15 Bulldozer line (in 2011).

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Figure: Block diagram of AMD's Athlon microarchitecture (1999) [4]

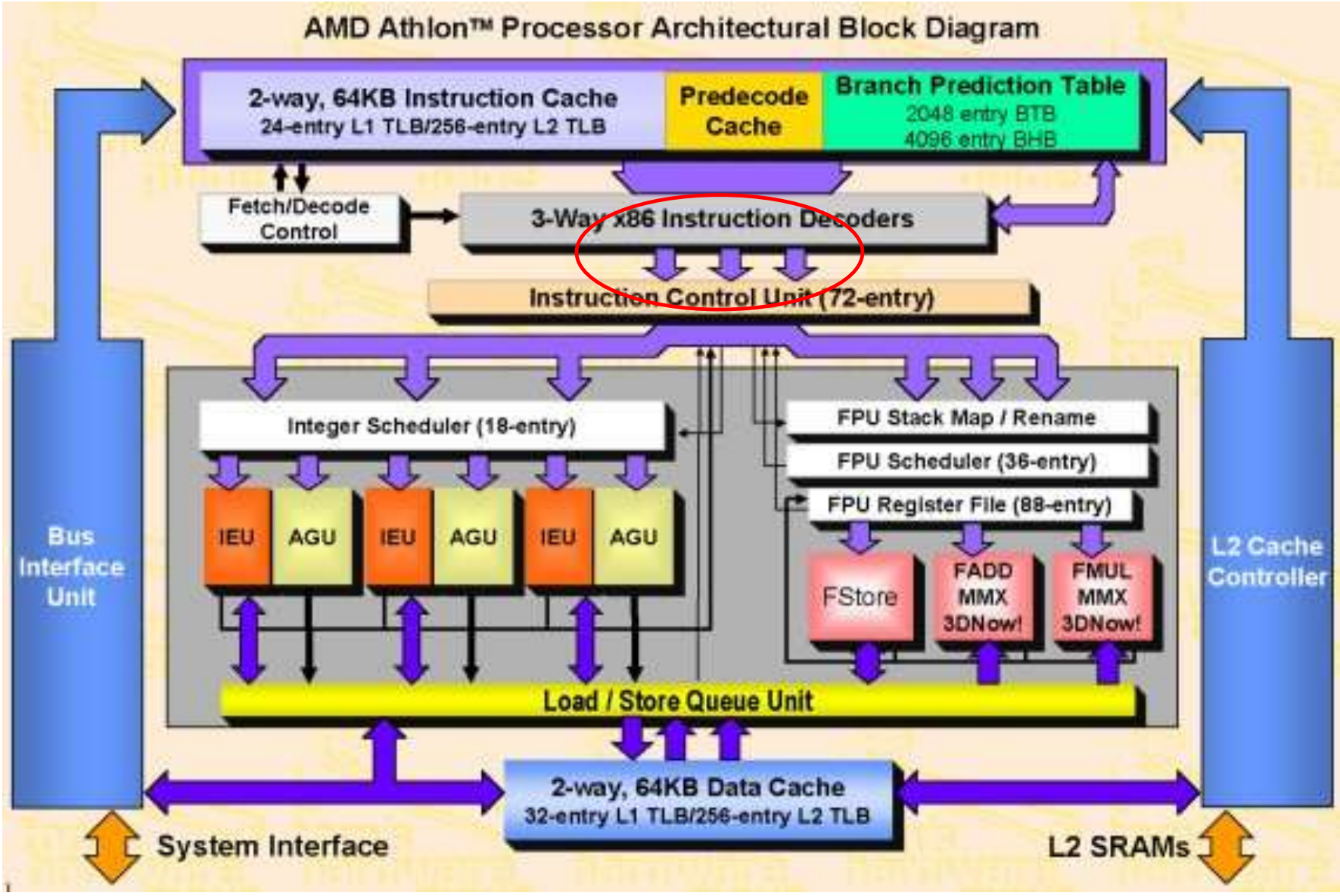
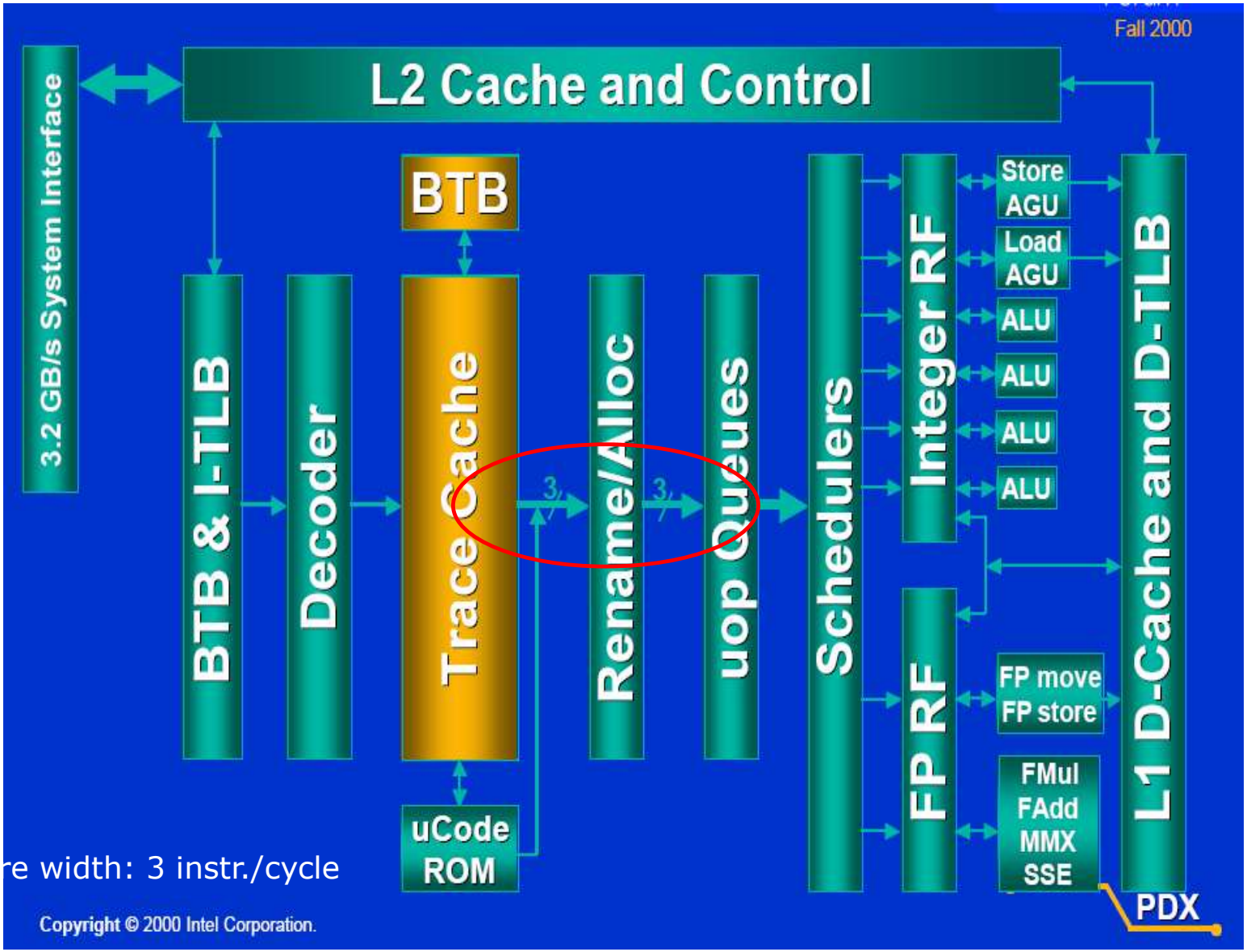
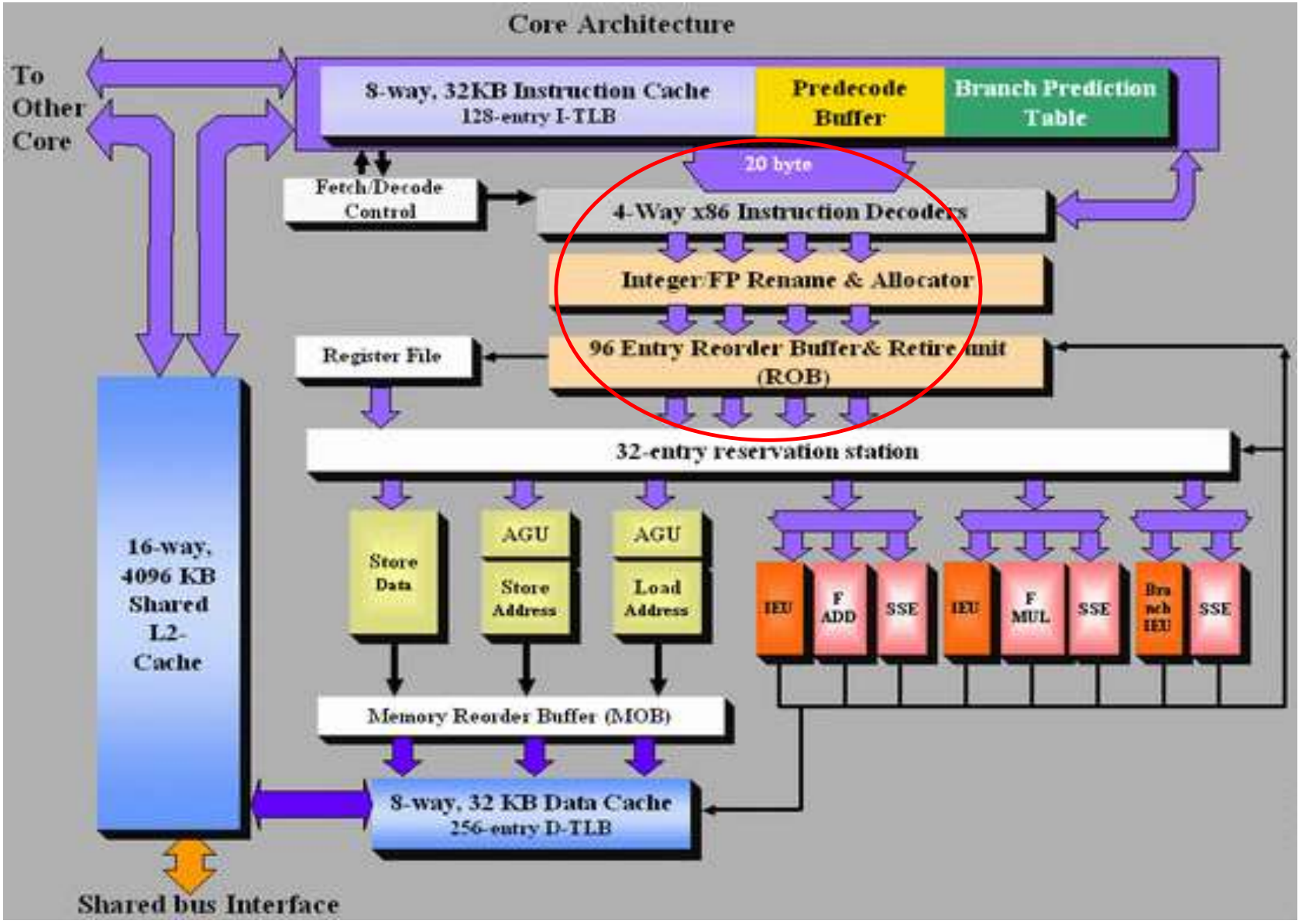


Figure: Block diagram of Intel's Pentium 4 microarchitecture 2000) [5]



re width: 3 instr./cycle

Figure: Block diagram of Intel's Core 2 microarchitecture (2006) [3]



Larger buffer and register sizes

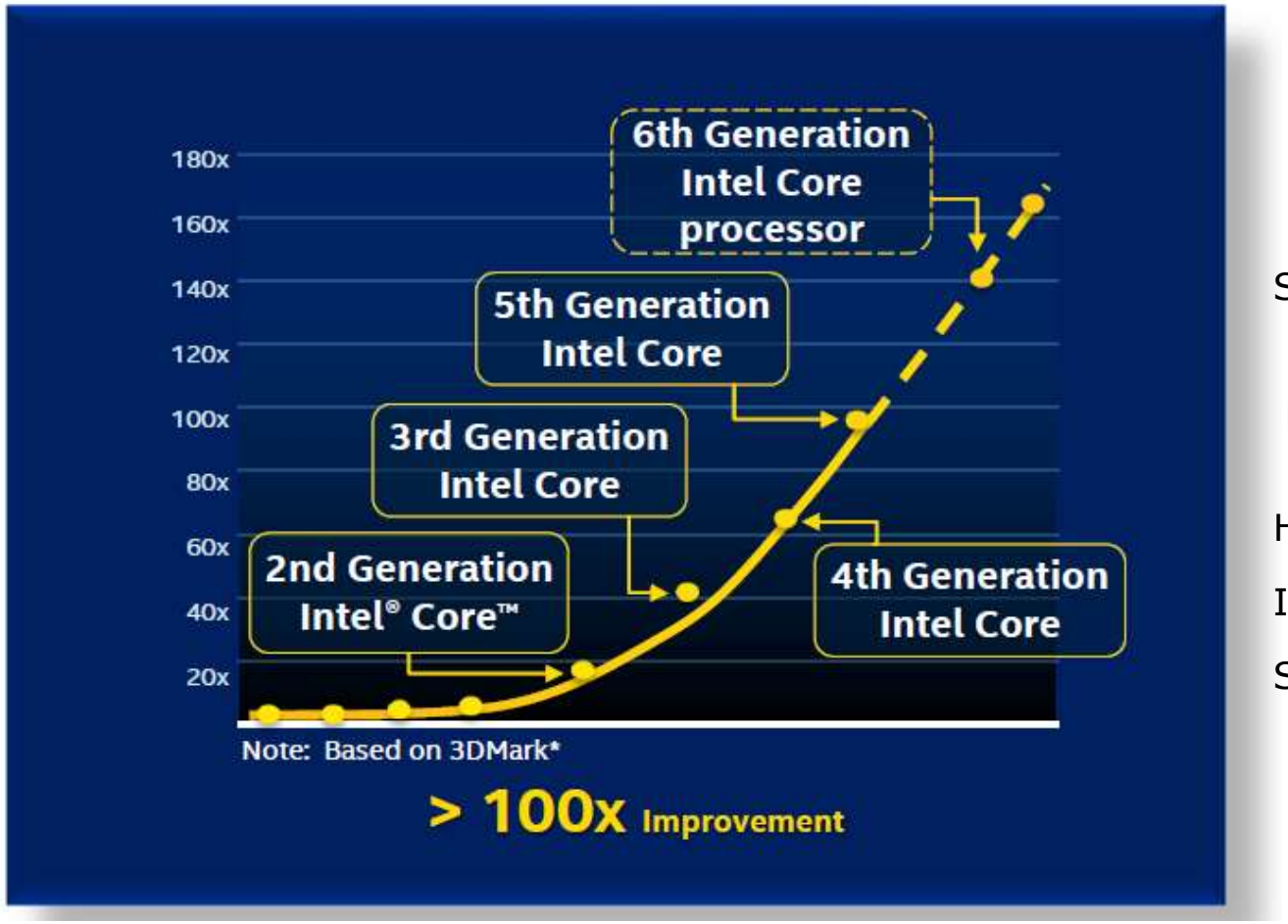
Instruction window (ROB), buffer and register sizes of subsequent generations of the Core 2 family [200]

	Sandy Bridge	Haswell	SkyLake
Out-of-order Window	168	192	224 ↑
In-flight Loads	64	72	72
In-flight Stores	36	42	56 ↑
Scheduler Entries	54	60	97 ↑
Integer Register File	160	168	180 ↑
FP Register File	144	168	168
Allocation Queue	28/thread	56	64/thread ↑

Out-of-order Window: Reorder Buffer (ROB)

6.2.2 Enhanced graphics

Performance increase of Intel's graphics over generations [196]



Skylake

Broadwell

Haswell

Ivy Bridge

Sandy Bridge

6.2.2 Enhanced graphics (2)

Evolution of main features of Intel's graphics families

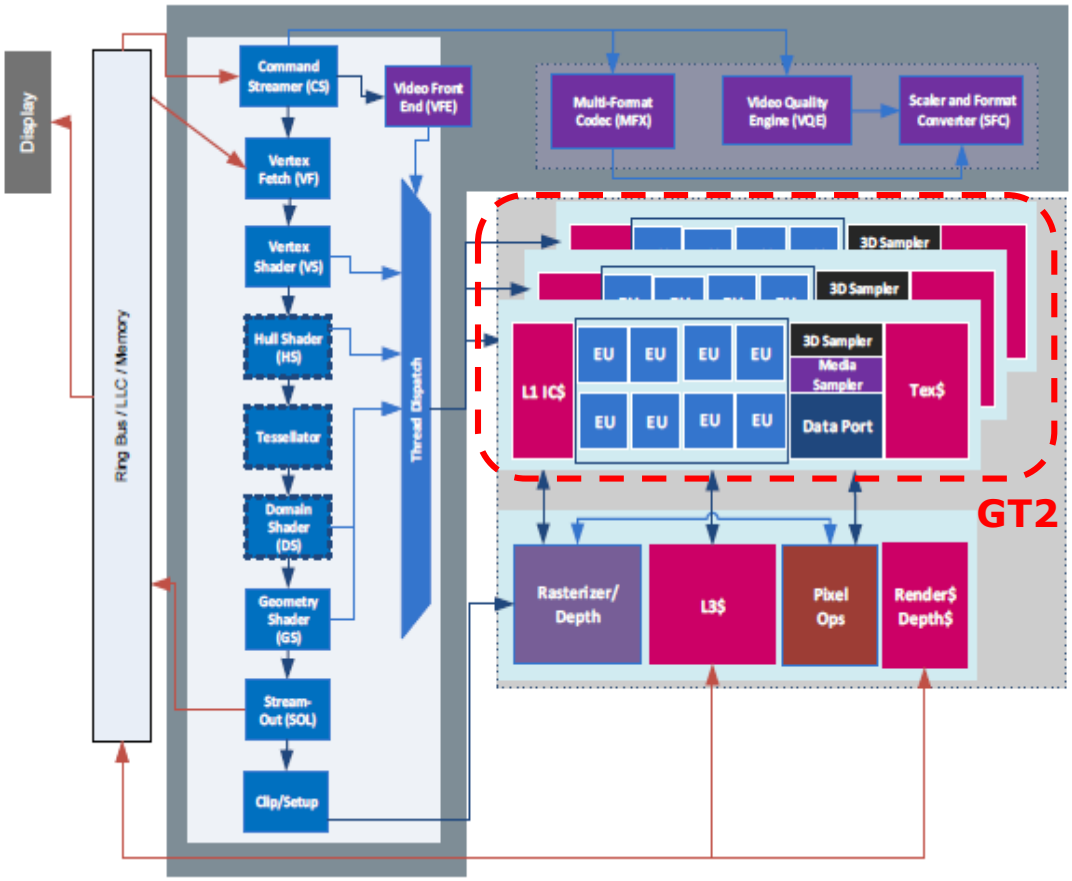
Intel Core generation	Graphics generation	Models	Graphics Technology level	No. of graphics slices	No. of EUs	eDRAM	OpenGL version	DirectX version	OpenCL version
Westmere	5th (Ironlake)	HD			12	--	2.1	10.1	n.a.
Sandy Bridge	6th	HD 2000	GT1	1 (2x3 EU)	6		3.1/3.3	10.1	n.a.
		HD 3000	GT2	1 (4x3 EU)	12				
Ivy Bridge	7th	HD 2500	GT1	1 (6 EU)	6	--	4.0	11.0	1.2
		HD 4000	GT2	1 (2x8 EU)	16				
Haswell	7.5th	HD 4200-HD 4700	GT2	1 (2x10 EU)	20	--	4.3	11.1	1.2
		HD 5000 Iris 5100	GT3	2	40				
		Iris Pro 5200				128 MB			
Broadwell	8th	HD 5300-HD 5600	GT2	1 (3x8 EU)	23/24	--	4.3	11.2	2.0
		HD 6000 Iris 6100	GT3	2	47/48				
		Iris Pro 6200	GT3e	2	48	128 MB			
Skylake	9th	HD 510	GT1	1 (3x4 EU)	12	--	4.4	12	2.0
		HD 515	GT1.5	1 (3x6 EU)	18				
		HD 520	GT2	1 (3x8 EU)	24				
		HD 530	GT2	1	24				
		HD 540	GT3e	2	48	64 MB			
		HD 580	GT4e	3	72	64/128 MB			

Main features of the Skylake line [190]

WCCFTech.com	Intel 14nm Tabla de configuración Skylake			
Variante	SKL-Y (BGA)	SKL-U (BGA)	SKL-H (BGA)	SKL-S (LGA)
Cores Configuraciones	2	2/2	4/4	4/2/4
Configuraciones gráficas	GT2	GT2 / GT3e	GT2 / GT4e	GT2 / GT2 / GT4e
eDRAM	-	64MB - GT3e	128MB - GT4e	64MB - GT4e
Memoria	LPDDR3 1600Mhz	LPDDR3 1600Mhz	DDR4 2133MHz	DDR3L / DDR3L-RS 1600Mhz, 2133MHz DDR4
TDP	4W	15-28W	35-45W	35-95W

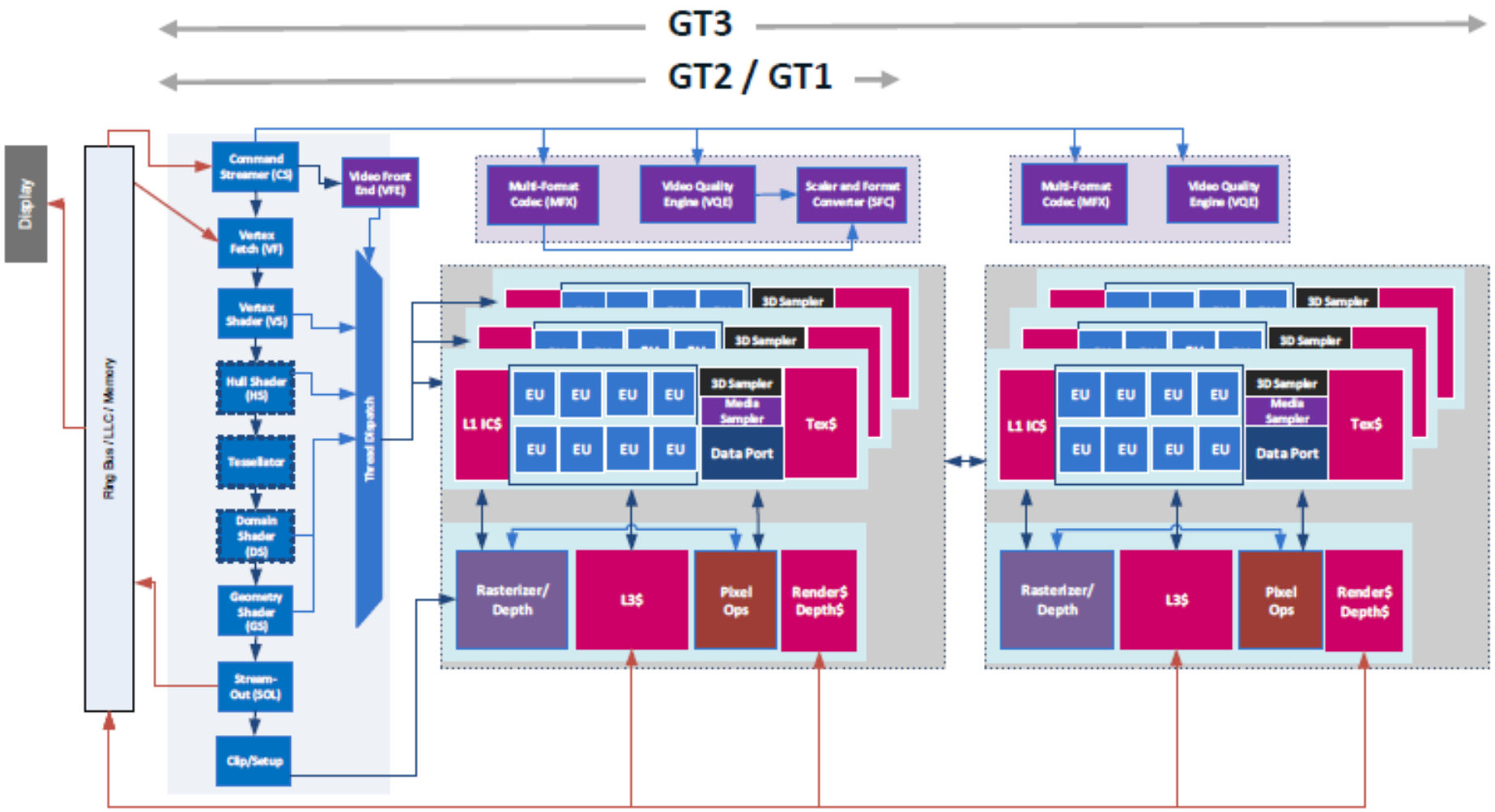
Tablets Mobiles High-perf. mobiles Desktops

Skylake/Gen9 graphics architecture overview [196]



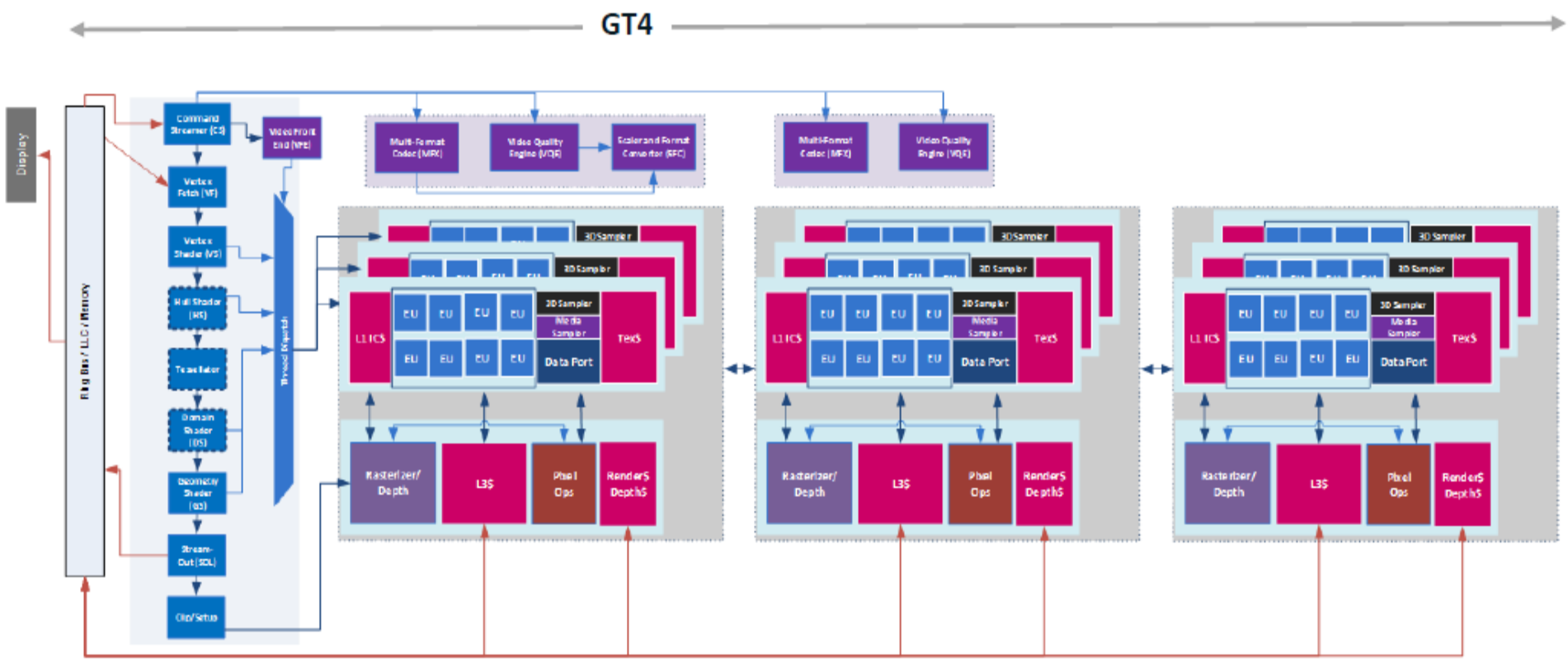
- 6th Generation Intel® Core™ Processor Graphics on 14nm process
- Adds support of latest APIs
  - DirectX* 12/11.3
  - OpenCL™ 2.0
  - OpenGL* 4.4
- Maintains similar uArch partitioning to Broadwell architecture
  - Unslice, slice, subslice, etc.

Gen9 graphics scalability -1 [196]



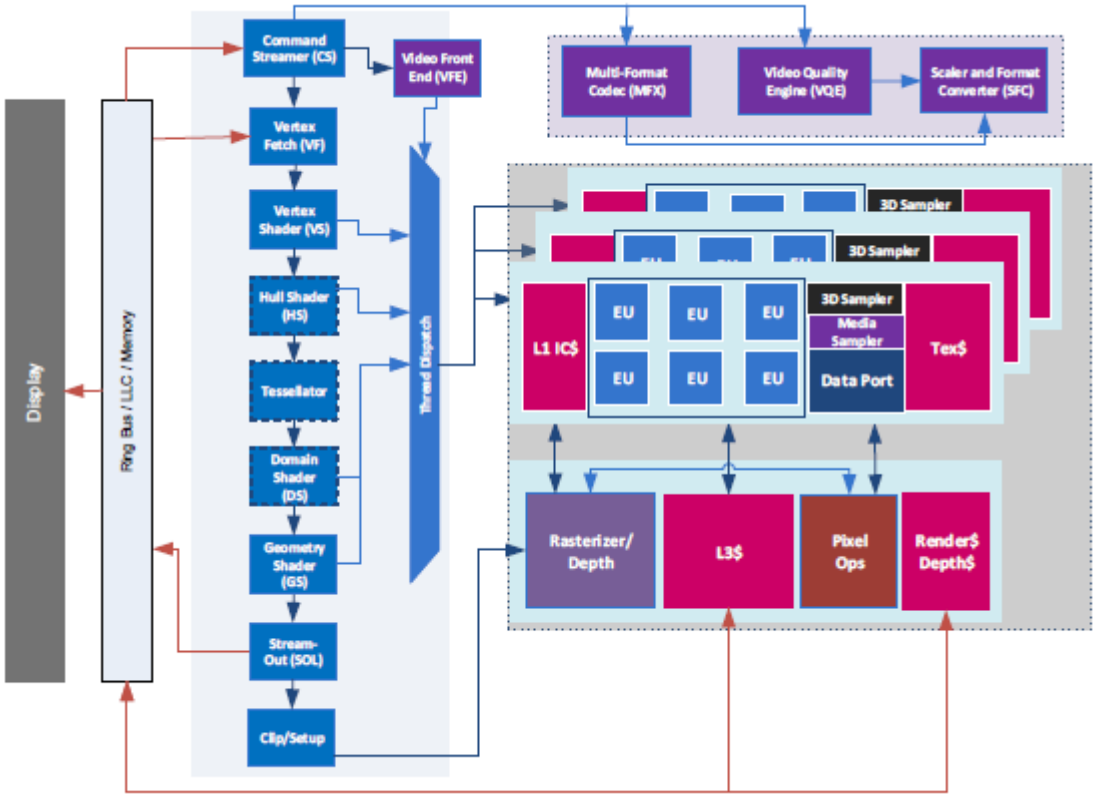
6.2.2 Enhanced graphics (6)

Gen9 graphics scalability -2 [196]



Gen9 graphics scalability -3 [196]

Scaling for GT 1.5 to reduce power



6.2.2 Enhanced graphics (8)

Gen9 graphics Codec support [196], [201]

Codecs	Decode	Encode
JPEG	Yes	Yes
MJPEG	Yes	Yes
MPEG2	Yes	Yes
AVC	Yes	Yes
MVC (Long GUID)	Yes	Yes
HEVC 8 bit	Yes	Yes
HEVC 10 bit	Yes*	No
VC-1	Yes	No
VP8	Yes	Yes
VP9	Yes*	No

New in Gen9

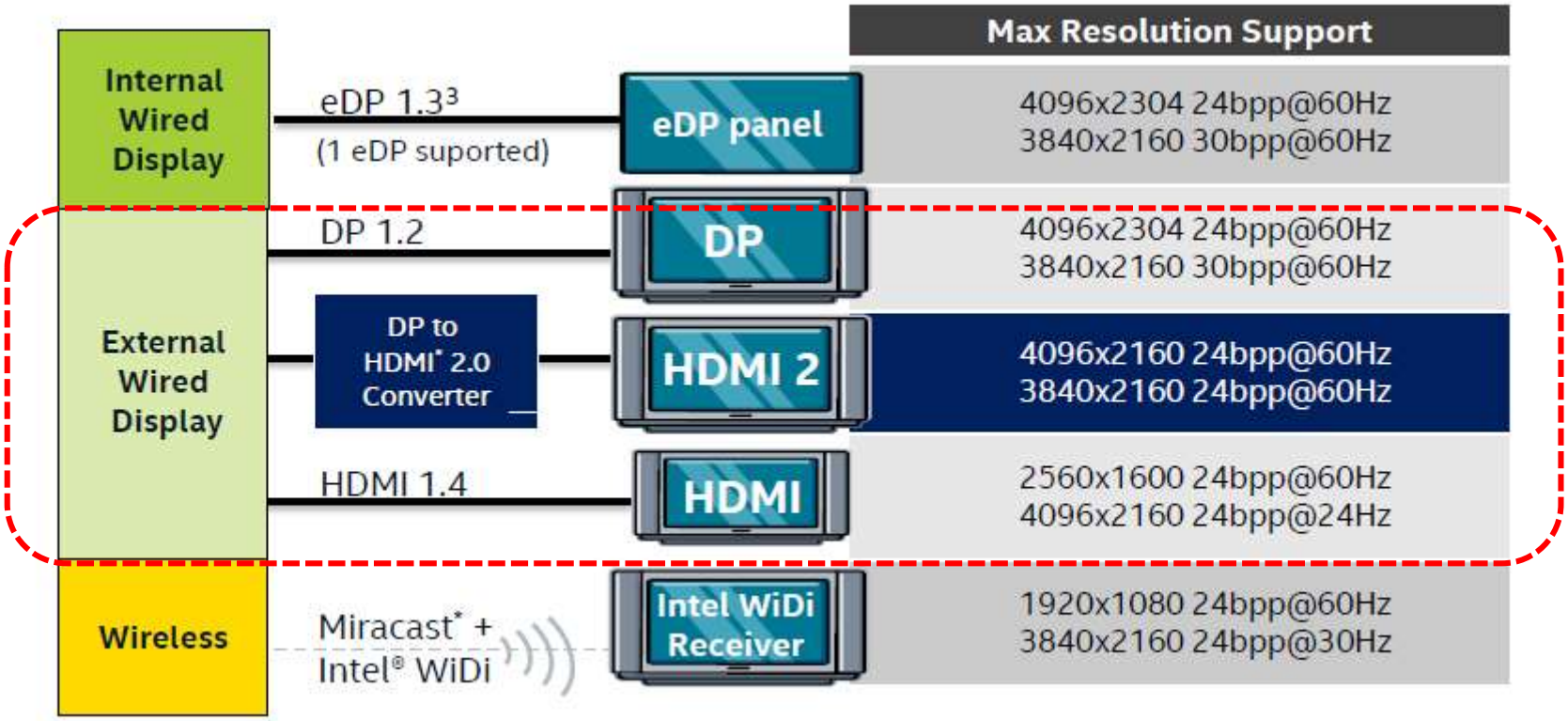
New Hardware Accelerated

*GPU Accelerated

Rich Codec Support
Mixture of Fixed-Function and GPU-Accelerated

With the new hardware accelerated codec solution watching a movie or video conferencing can be done by highly efficient fixed-function circuits rather than by using more flexible, but more power hungry CPU and GPU cores [201]

Gen9 graphics display support [201]



- It supports 3 display pipes.
- WiDi is Intel's **W**ireless **D**isplay technology to transmit music, videos, movies, photos etc. from a WiDi compatible computer to a compatible HDTV.

  The initial version of WiDi supported only a low resolution of 720p, Skylake provides already HD quality with a resolution of 1080.
- Miracast is a WiDi standard of the Wi-Fi Alliance providing HD quality.

6.2.2 Enhanced graphics (10)

Note

- Skylake does not make use of the FIVR technology, as indicated in the Figure below.
- The reason for omitting FIVR in Skylake (and probably also is the subsequent Cannon Lake) is that it increases unduly the die temperature and limits overclocking.

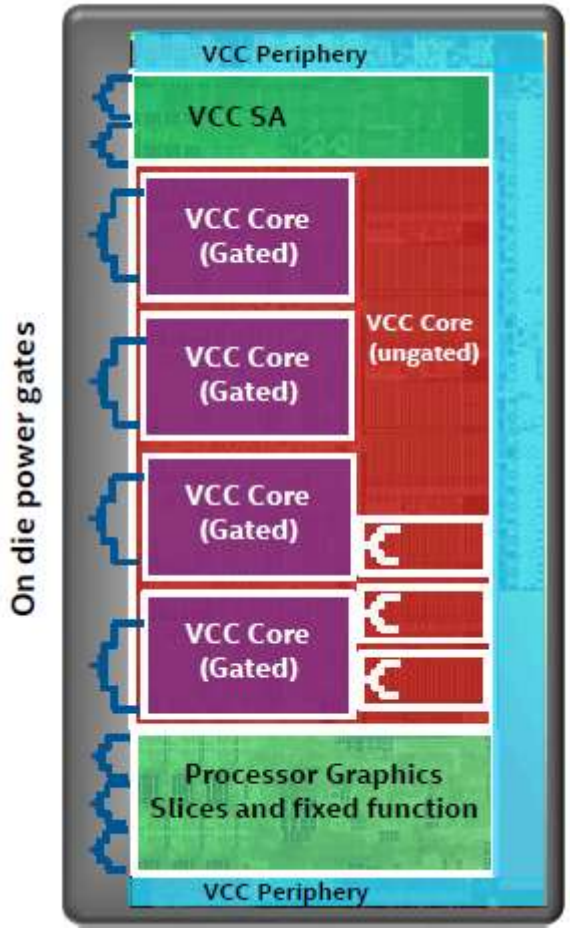


Figure: Voltage domains of Skylake [200]

Note that all cores share the same voltage and even the same frequency.

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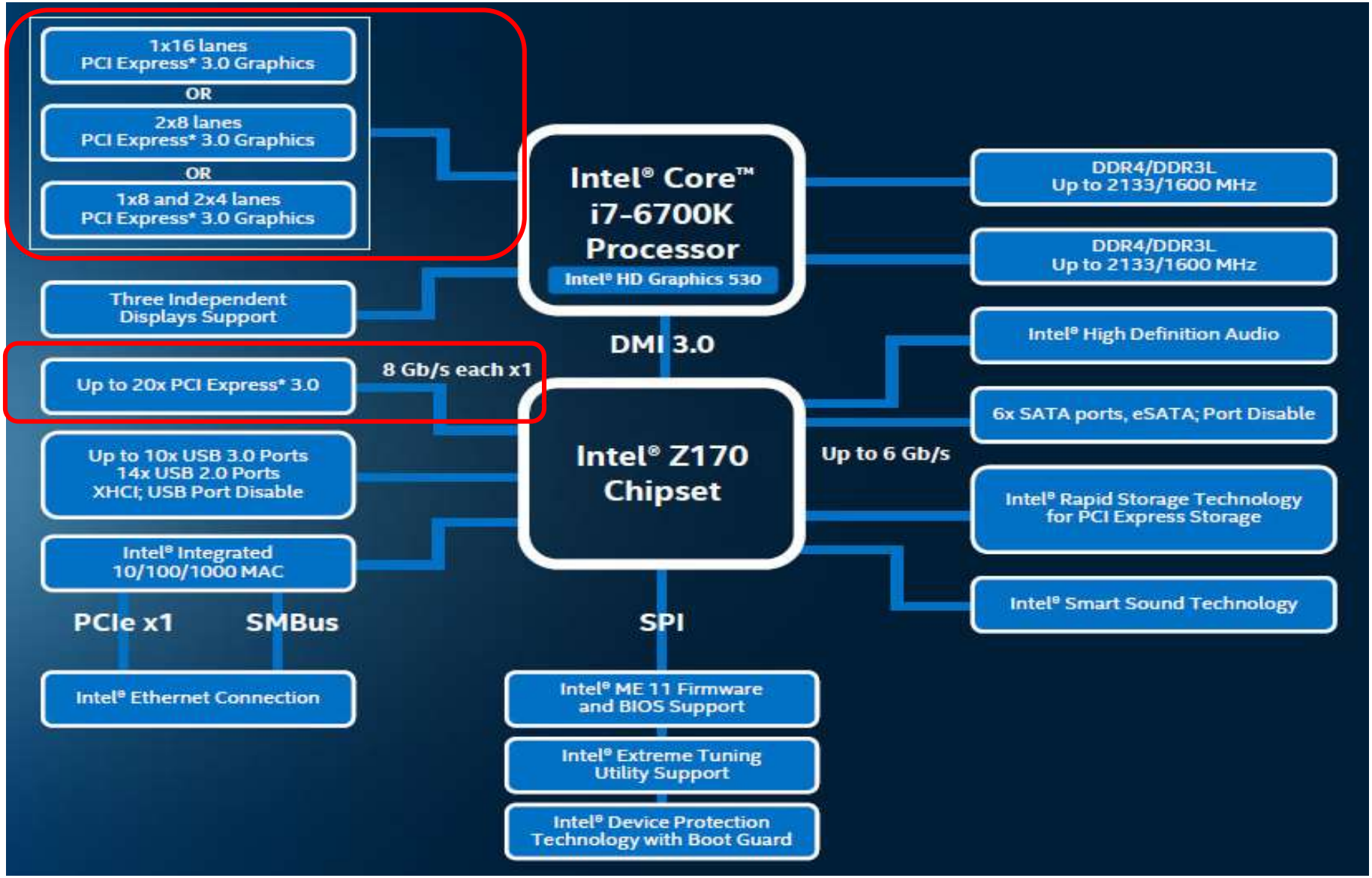
6.2.3 Support of PCIe 3.0

Example: Intel Core i7-6700K desktop processor platform [203]



6.2.3 Support of PCIe 3.0 (2)

Performance features of the PCIe standards [227]

PCI Express version	Line code	Transfer rate	Throughput per direction ×1	×4	×8	×16	Issued
1.0	8b/10b	2.5 GT/s	250 MB/s	1 GB/s	2 GB/s	4 GB/s	2003
2.0	8b/10b	5 GT/s	500 MB/s	2 GB/s	4 GB/s	8 GB/s	2007
3.0	128b/130b	8 GT/s	984.6 MB/s	3.94 GB/s	7.9 GB/s	15.8 GB/s	2010
4.0	128b/130b	16 GT/s	1969 MB/s	7.9 GB/s	15.8 GB/s	31.5 GB/s	2017
5.0	128b/130b	32 or 25 GT/s	3938 or 3077 MB/s	15.8 or 12.3 GB/s	31.5 or 24.6 GB/s	63.0 or 49.2 GB/s	2019 (expected)

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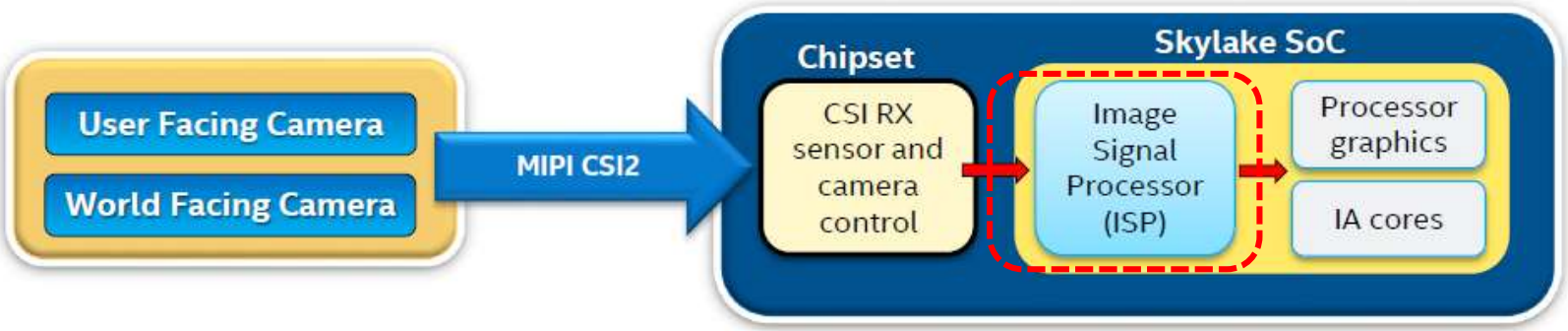
6.3 Major innovations of the Skylake line

- 6.3.1 Integrated ISP (Image Signal Processing)
- 6.3.2 Memory Side Cache
- 6.3.3 Innovations in power management

6.3 Major innovations of the Skylake line

6.3.1 Integrated ISP (Image Signal Processing) [200]



Complete Imaging & Camera Solution

- Full hardware and software integration
- Optimized module/sensor support:
  - Support up to 4 cameras (2 concurrent)
  - Up to 13MP sensors
- Premium quality imaging optimized system (ISP+ CPU + GPU + display)
- Partnerships with sensor ecosystem for TTM, reduced engineering costs, smaller form factors

Integrated ISP for Greater Efficiency

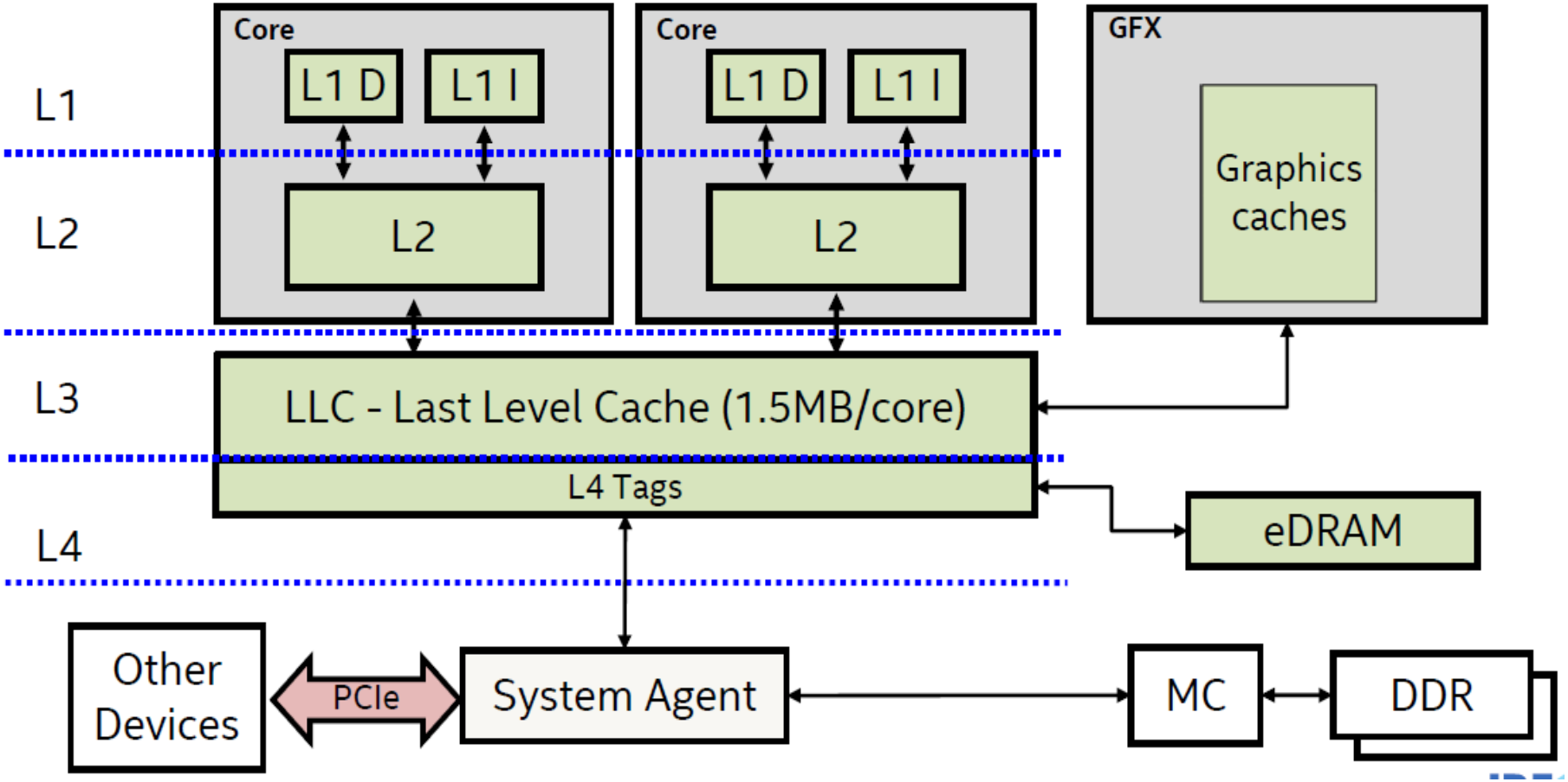
- BOM reduction
- Reduced module footprint
  - Enables smaller and thinner form factors
- Power optimized
- Enables advanced imaging and camera features

CSI: Camera Serial Interface
BOM: Bill of Material

*

6.3.2 Memory Side Cache (MSC)

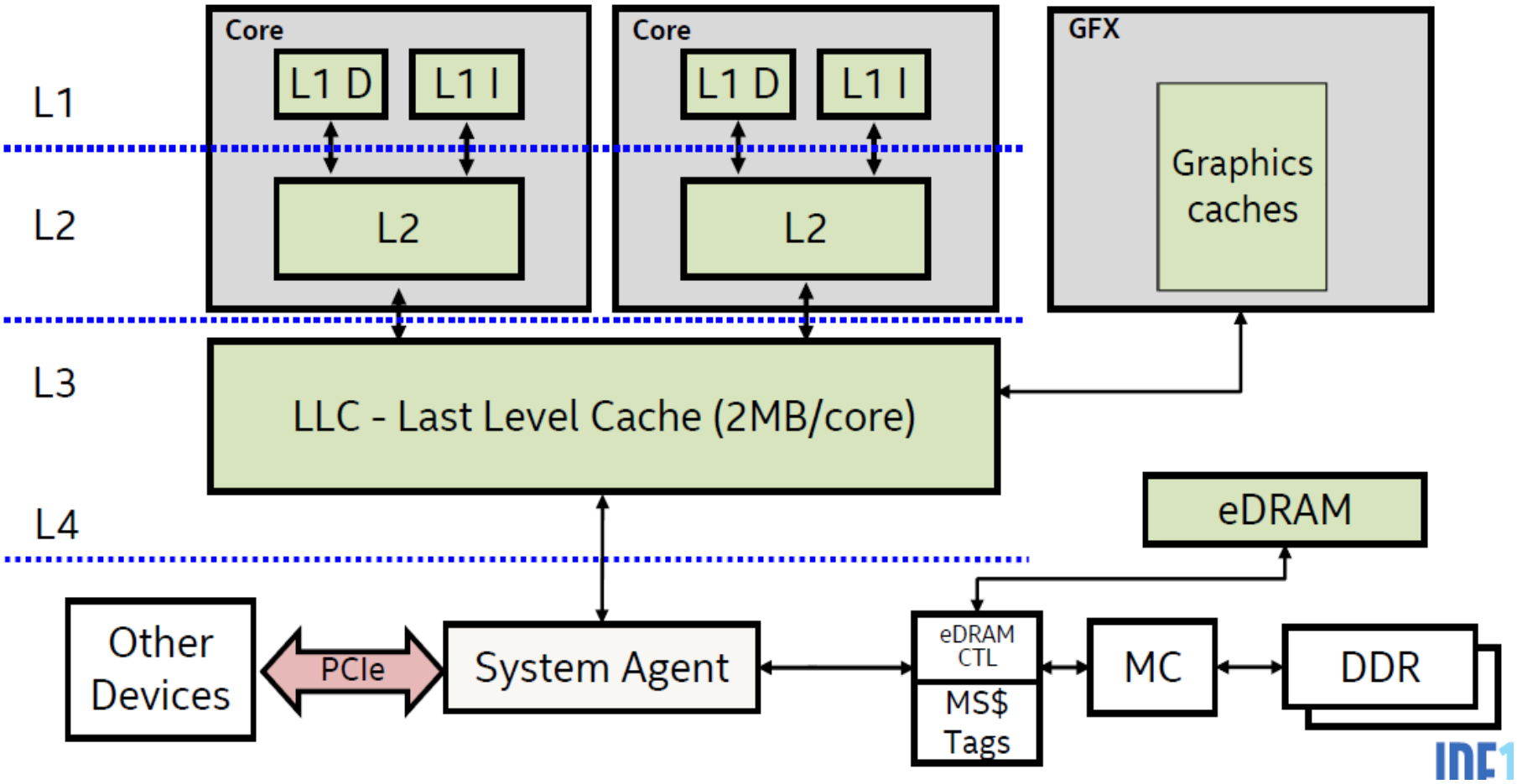
The eDRAM cache of Broadwell [200]



Note: The L4 eDRAM cache operates as a victim cache to the L3 (LLC).

*

Memory Side Cache of the Skylake [200]



MS$: Memory Side Cache
CTL: Control

*

6.3.2 Memory Side Cache (MSC) (3)

Benefits of the Memory Side Cache (MSC) [200]

- It is fully coherent.
- Available for use by I/O devices and the Display engine as well.

*

6.3.3 Innovations in power management

6.3.3.1 Speed Shift Technology

6.3.3.2 Duty cycle control of the cores

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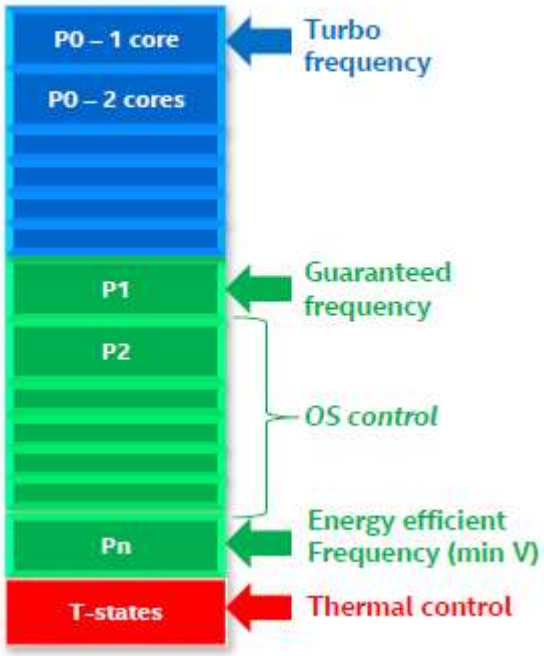
The legacy power management technology, called the DVFS (Dynamic Voltage and Frequency Scaling) -1



- On the other hand, when the workload demands a higher operating point than P1, the processor can take over the control over the power management by activating the turbo technology.

- Lower than Pn states are used only to manage critical conditions, like overheating the die.

*

6.3.3.1 Speed Shift Technology (2)

The drawback of the SpeedStep technology

- The basic drawback is slow responsiveness, e.g. 30 ms responsiveness, needed until the OS recognizes the change of operating conditions (e.g. workload) and responds by resetting the operating point [201].
- This is unfavorable for low residency workloads, like quickly changing video recording.

*

6.3.3.1 Speed Shift Technology (3)

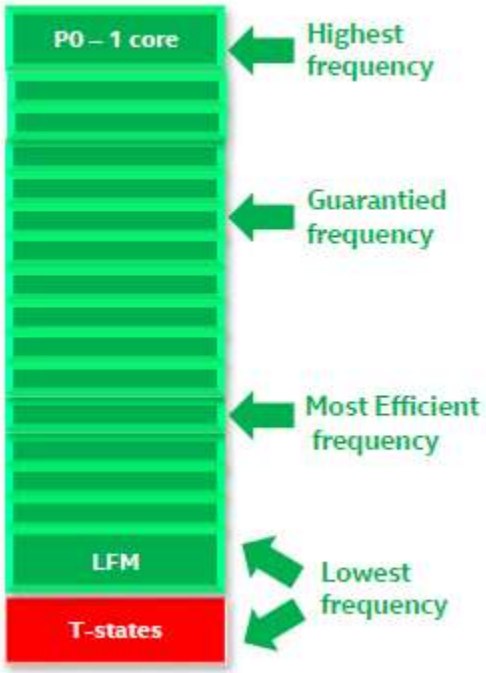
Principle of the Speed Shift Technology

- The OS passes the control over power management to the processor, more precisely to the PCU (Power Control Unit) of the processor, along with hints about the user preference concerning power management (like max. performance, max. battery life etc.).
- The PCU performs the actual P-state control, called Speed Shift Technology (Intel) or or Autonomous Control (Intel) or Hardware Controlled Performance States (ACPI).
- The Autonomous control can cover all P-states or a subset of the P-states, as indicated in the next Figures.

*

6.3.3.1 Speed Shift Technology (4)

Passing power management control for all P-states to the CPU [198]



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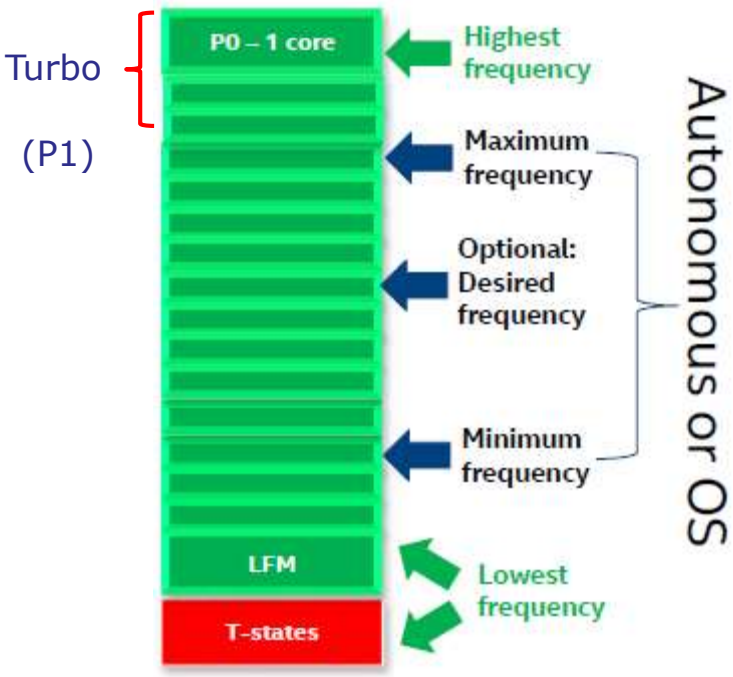
6.3.3.1 Speed Shift Technology (5)

Passing power management control for a subset of P-states to the CPU [198]



*

6.3.3.1 Speed Shift Technology (6)

Benefit of the Speed Shift Technology

It reduces the responsiveness of the power management from 30 ms to about 1 ms [201].

*

6.3.3.2 Duty cycle control [198]

While running applications

- dynamic dissipation: ~ f^3
- runtime: ~ $1/f$
- ⟹ total energy consumption originating from the dynamic dissipation: ~ f^2

  with f denoting the clock frequency.

As the performance is proportional with f, the energy consumption arising from the dynamic dissipation is proportional to the square of the frequency f, as indicated below.

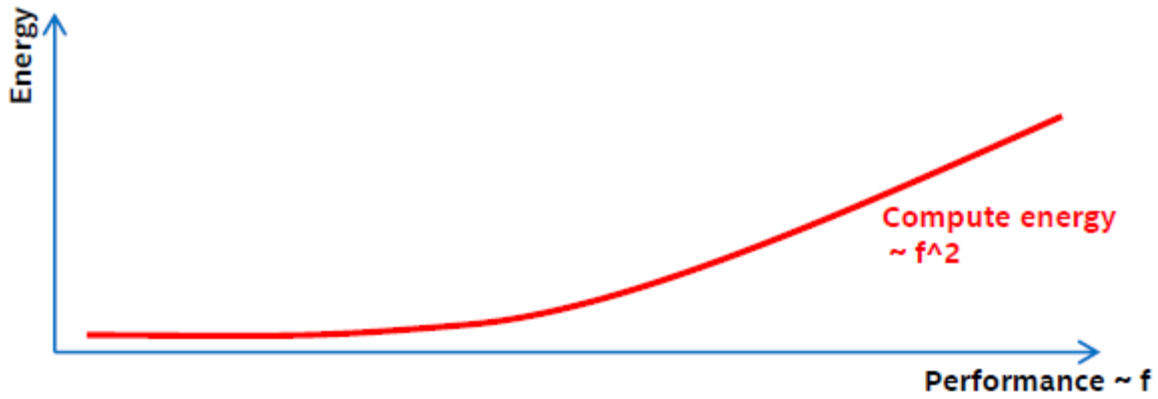


Figure: Dependence of energy consumption arising from the dynamic dissipation (designated as Compute energy in the Figure) on the performance (~ f)

*

6.3.3.2 Duty cycle control (2)

On the other hand

- the energy consumption originating from the static dissipation is proportional to the runtime.

  The runtime is inversely proportional to the frequency (f).

  Consequently, the energy consumption arising from the static dissipation is inversely proportional to the frequency (f) which is proportional to the performance, as indicated in the Figure below.

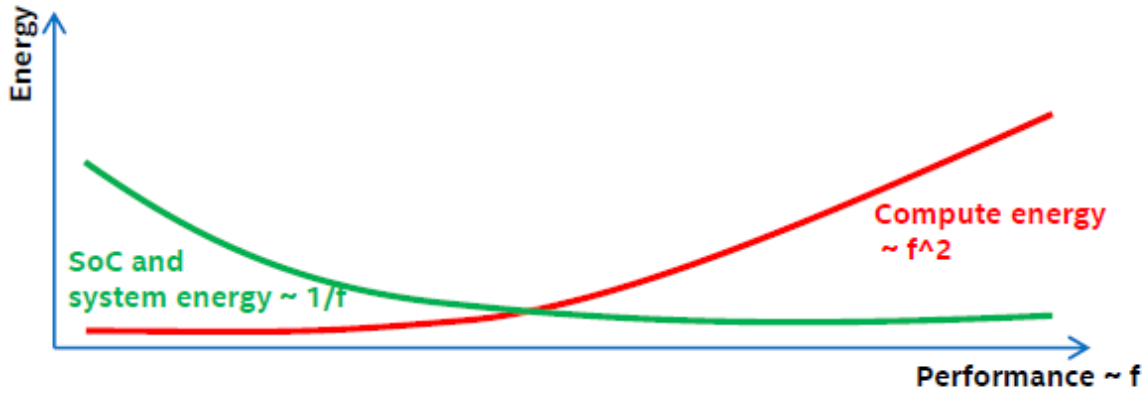


Figure: Dependence of energy consumption originating from the static dissipation and system power (designated as SoC and system energy in the Figure) on the performance (~ f) [198]

*

6.3.3.2 Duty cycle control (3)

As a consequence, the total energy consumption originating from both the

- dynamic dissipation and
- static dissipation as well as system power consumption

has a minimum, as indicated in the Figure below.

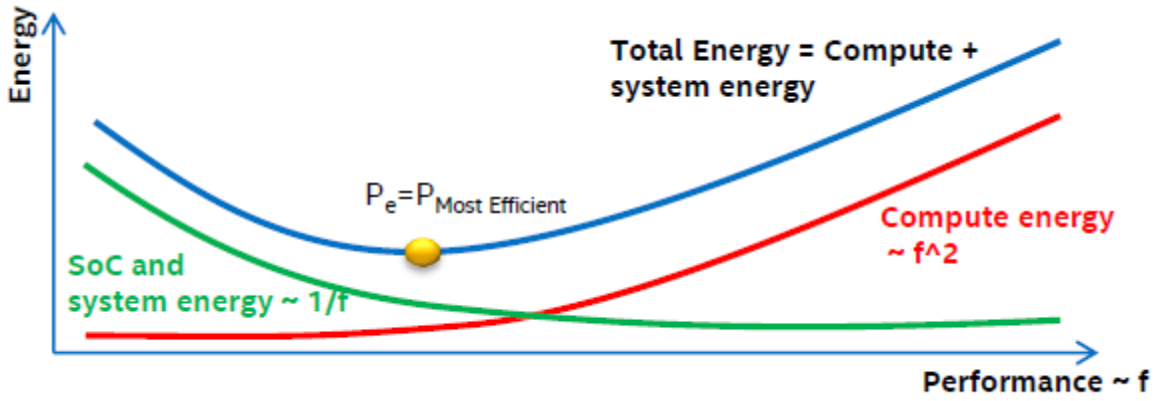


Figure: Dependence of energy consumption originating from both the dynamic dissipation (designated as the Compute energy in the Figure) and the static dissipation and system power (designated as SoC and system energy in the Figure) on the performance

Obviously, the min. energy consumption point (Pe) is the most efficient working point of a core of the processor.

*

6.3.3.2 Duty cycle control (4)

Power management with taking into account the most efficient Pe working point [198]

- Frequency will be lowered as far as possible until the Pe working point is reached.
- Pe will be calculated every ms based on the workload and system characteristics.
- There is no benefit when the system is clocked below the Pe point, as it would increase the energy consumption.
- Therefore, a so called EARtH algoritm overrides lower P requests and sets f according to Pe.

The EARtH algorithm is activated only if it is possible to enter the package sleep state.

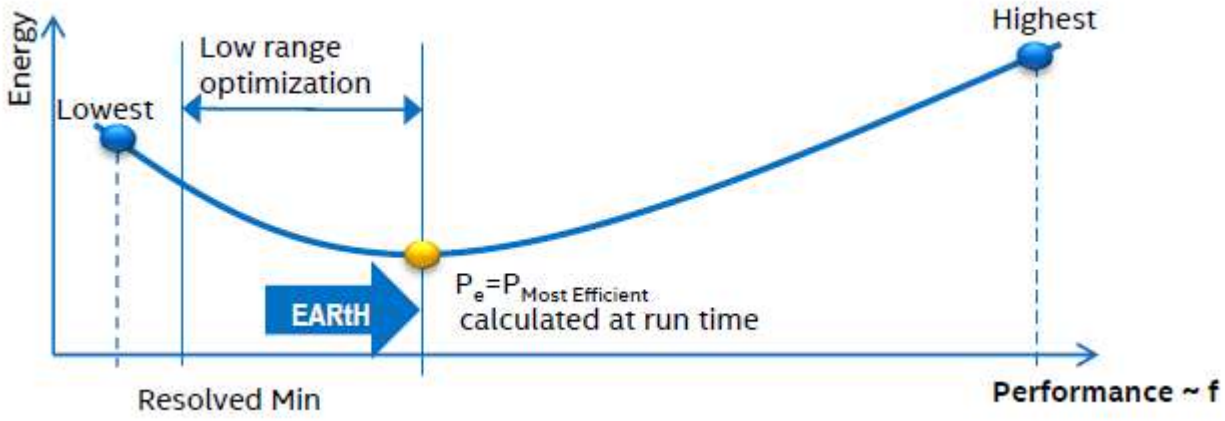


Figure: Power management with taking into account the most efficient Pe working point [198]

*

6.3.3.2 Duty cycle control (5)

Duty cycling [198]

- While managing power going below Pe would reduce energy consumption inefficiently due to the fixed power components.
- In this region turning the package on and off, called duty cycling, reduces power proportionally to run time, as shown in the Figure below, about 1000 times in a sec.

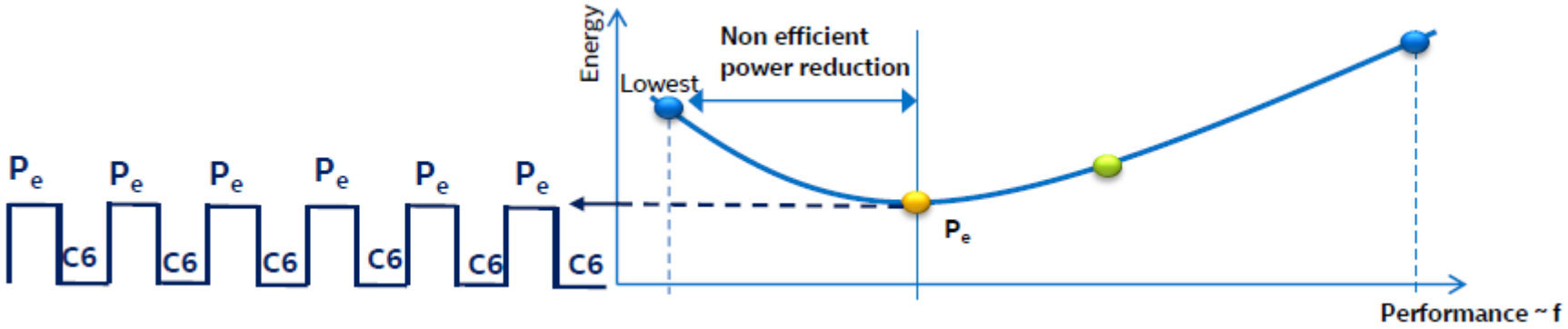


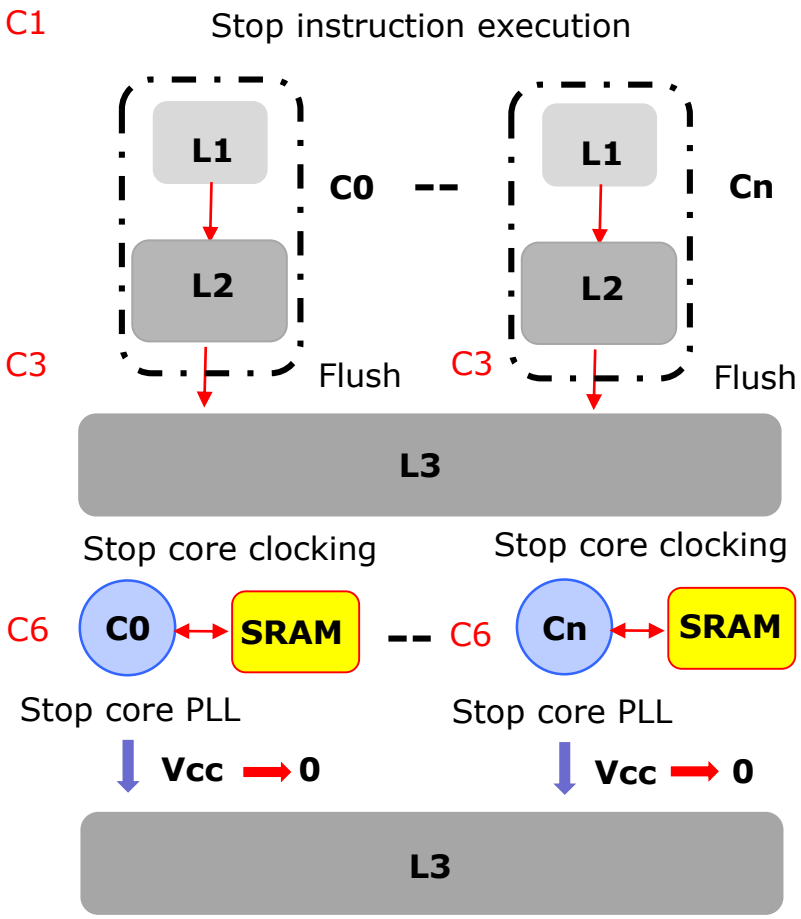
Figure: Principle of duty cycling used to reduce energy consumption in the region below Pe

- In the region below Pe duty cycling is a more effective technique to reduce power for low power demand than reducing frequency below Pe.

*

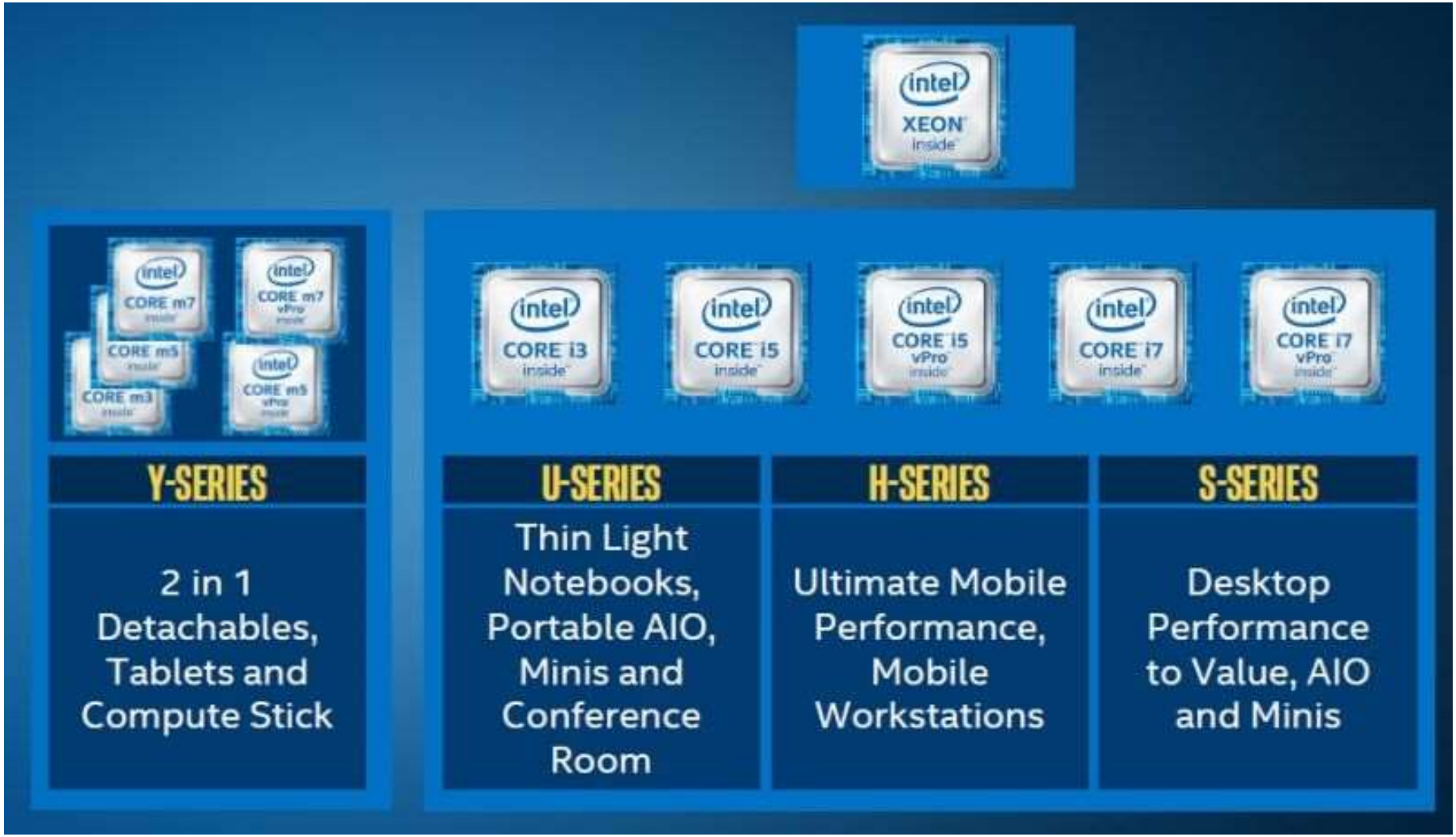
6.3.3.2 Duty cycle control (6)

Power saving measures in C1 to C6 idle states



6.4 Skylake-based mobile and desktop lines

Overview of the Skylake-based mobile and desktop series -1 [206]



4.5 W | 15/28 W | 45 W | 65/91 W

Overview of the Skylake-based mobile and desktop series -1 [202]

	2 in 1 Detachables, Tablets and Compute Stick	Thin Light Notebooks, Portable AIO, Minis and Conference Room		Ultimate Mobile Performance, Mobile Workstations		Desktop Performance to Value, AIO and Minis	
	Y-SERIES	U-SERIES		H-SERIES		S-SERIES	
5 Dies 4 Packages							
Dies	2+2	2+2	2+3e	4+2	4+4e	2+2	4+2
Package (mm)	BGA 1515	BGA 1356		BGA 1440		LGA 1151	
	20 x 16.5	42 x 24		42 x 28		37.5 x 37.5	
TDP (W)	4.5	15	15, 28	45		35, 65	35, 65, 91("K")
Chipset	Integrated 6th Gen Intel® Core™ Platform I/O			Intel® 100 Series chipset (23mm x 23mm)			

BGA: Ball Grid Array (to be soldered)
LGA: Land Grid Array (to be socketed)

Dies: No. of cores and GT levels, e.g. 2+2 means: 2 cores +GT 2 graphics, etc.

Key features of the Skylake-based mobile and desktop lines [190]

WCCFTech.com	Intel 14nm Tabla de configuración Skylake			
Variante	SKL-Y (BGA)	SKL-U (BGA)	SKL-H (BGA)	SKL-S (LGA)
Cores Configuraciones	2	2/2	4/4	4/2/4
Configuraciones gráficas	GT2	GT2 / GT3e	GT2 / GT4e	GT2 / GT2 / GT4e
eDRAM	-	64MB - GT3e	128MB - GT4e	64MB - GT4e
Memoria	LPDDR3 1600Mhz	LPDDR3 1600Mhz	DDR4 2133MHz	DDR3L / DDR3L-RS 1600Mhz, 2133MHz DDR4
TDP	4W	15-28W	35-45W	35-95W

Example 1: Main features of the models of the 4.5 W Skylake m mobile line [202]

6th Gen Intel® Core™ m Processor SKU Detail

Processor Number	Cores/ Threads	Base Freq (GHz)	Intel Turbo Boost Technology 2.0			Graphics	Graphics Base / Max Freq (MHz)	LPDDR3 /DDR3L Memory Speed Support (MHz)	L3 Cache	TDP	cTDP Up/ Down	Tj (deg)	SDP	Tj @ SDP (deg)	Intel SIPP	Intel Technologies					1ku Pricing
			Max Single Core Turbo (GHz)	Max Dual Core Turbo (GHz)	Max Quad Core Turbo (GHz)											Intel vPro	Intel TXT	Intel VT-d	Intel VT-x	AES-NI	
Intel® Core™ m7 Processors (Y-Processor Line)																					
6Y75	2/4	1.2	3.1	2.9	N/A	Intel® HD graphics 515	300/1000	1866/ 1600	4MB	4.5W	7W / 3.5W	100	3W	N/A	2016	✓	✓	✓	✓	✓	$393
Intel® Core™ m5 Processors (Y-Processor Line)																					
6Y57	2/4	1.1	2.8	2.4	N/A	Intel® HD graphics 515	300/900	1866/ 1600	4MB	4.5W	7W / 3.5W	100	3W		2016	✓	✓	✓	✓	✓	$281
6Y54	2/4	1.1	2.7	2.4	N/A	Intel® HD graphics 515	300/900	1866/ 1600	4MB	4.5W	7W / 3.5W	100	3W					✓	✓	✓	$281
Intel® Core™ m3 Processors (Y-Processor Line)																					
6Y30	2/4	0.9	2.2	2.0	N/A	Intel® HD graphics 515	300/850	1866/ 1600	4MB	4.5W	7W / 3.8W	100	3W					✓	✓	✓	$281
Intel® Pentium® Processors (Y-Processor Line)																					
4405Y	2/4	1.5	N/A	N/A	N/A	Intel® HD Graphics	300 / 800	1866/ 1600	2MB	6W	N/A/ 4.5W	100	N/A						✓	✓	TBD

6.4 The Skylake-based mobile and desktop lines (5)

Remark

cTDP down – when a cooler or more quiet mode of operation is desired, this mode specifies a lower TDP and lower guaranteed frequency versus the nominal mode.

cTDP up – when extra cooling is available, this mode specifies a higher TDP and higher guaranteed frequency versus the nominal mode.

6.4 The Skylake-based mobile and desktop lines (6)

Example 2: The unlocked Skylake S desktop line

Main features of the unlocked Skylake S desktop line [202]

Brand Name and Processor Number[1]	Base Frequency (GHz)	Max Turbo Frequency[2] (GHz)	Cores/ Threads	Cache	PCI Express* 3.0 Lanes	Memory Support	TDP	Socket (LGA)	Recommended Customer Pricing
Intel® Core™ i7-6700K	4.0	Up to 4.2	4/8	8MB	16	2 channels DDR4-2133 DDR3L-1600	91W	1151	$350
Intel® Core™ i5-6600K	3.5	Up to 3.9	4/4	6MB	16	2 channels DDR4-2133 DDR3L-1600	91W	1151	$243

Note that the 91 W unlocked Skylake S-line does not include integrated graphics, as most users of this high-end processor will attach discrete graphics cards.

Max. base frequency of Skylake models with different TDPs and configurations
(Based on data from [202])

TDP (W)	No. of cores	Graphics	No. of graphics EUs	eDRAM	Base frequency (GHz)
4.5	2	HD 515	18	--	1.2
15	2	HD 540	48	64 MB	2.2
15	2	HD 520	24	--	2.6
28	2	HD 550	48	64 MB	3.3
35	4	HD 530	24	--	2.8
45	4	HD 530	24	--	2.9
65	4	HD 530	24	--	3.4
91	4	--	--	--	4.2

Note that low TDP can be achieved first of all by reducing the core frequency and limiting the computer resources (cores, GPU EUs) provided.

Example Skylake-S platform: Intel Core i7-6700K desktop processor platform [203]