Intel's Core 2 family - TOCK lines
Sunny Cove

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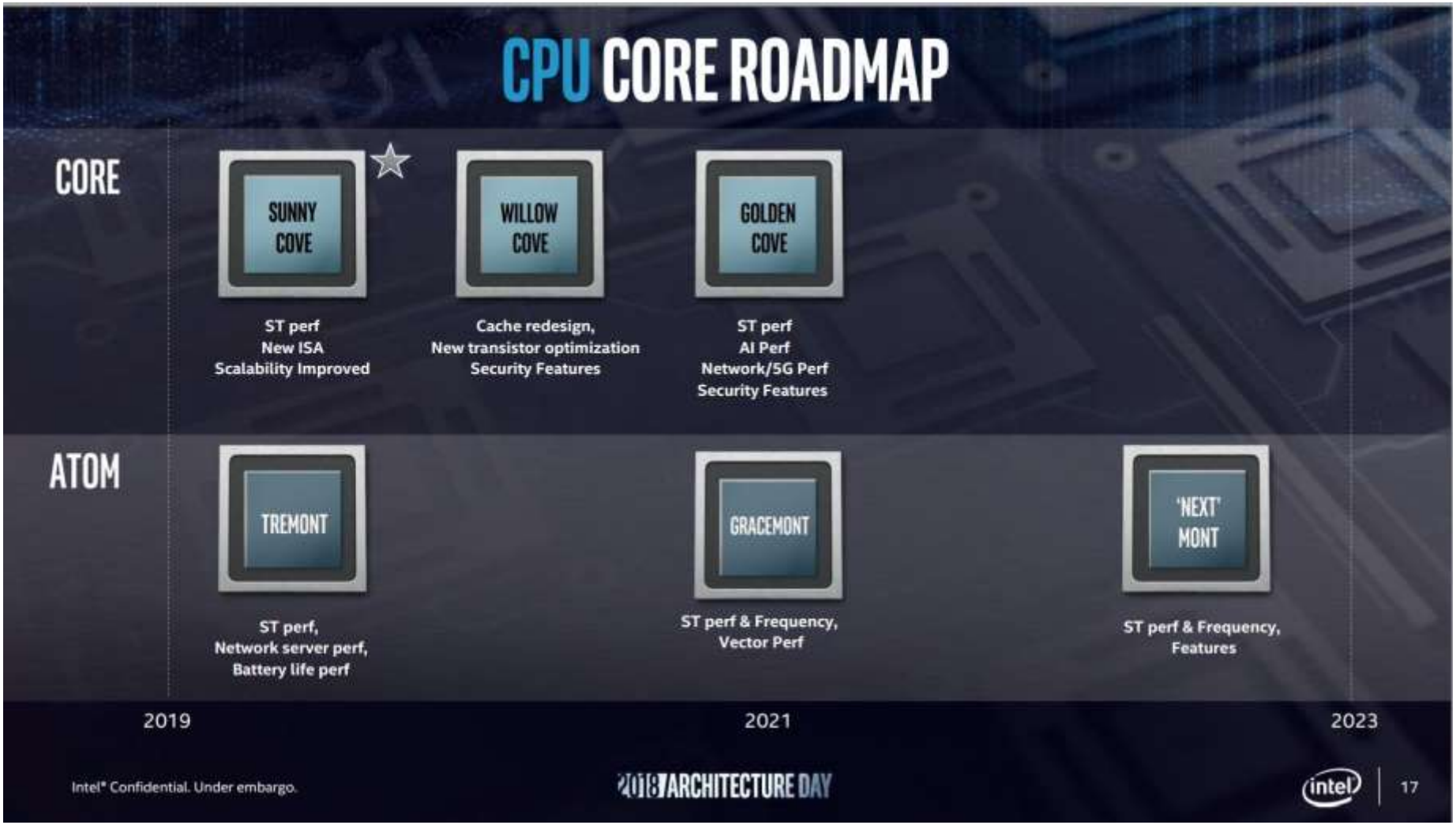
12.1 Introduction to the Sunny Cove

12.1 Introduction to the Sunny Cove [296]

- Announced in 12/2018 at Intel's Architecture Day, to be launched in 2019.
- Manufactured on Intel's 10 nm technology.
- Presumably, the Sunny Cove cores paired with Gen11 graphics will yield the Ice Lake processor.
- Sunny Cove cores offer increased single-threaded performance, new instructions, and 'improved scalability

Intel's CPU roadmap 2019 – 2022 [297]



12.1 Introduction to the Sunny Cove (3)

Evolution of Intel's manufacturing technology [296]

Intel Core Microarchitecture Roadmap			
Core Name	Year	Process Node	Improvements
Skylake	2015	14 nm	Single Threaded Performance Lower Power Other Optimizations
Kaby Lake	2016	14 nm+	Frequency
Coffee Lake	2017	14 nm++	Frequency
Coffee Refresh	2018	14 nm++	Frequency
Sunny Cove	2019	10 nm	Single Threaded Performance New Instructions Improved Scalability
Willow Cove	2020 ?	10 nm ?	Cache Redesign New Transistor Optimization Security Features
Golden Cove	2021 ?	7 / 10 nm ?	Single Threaded Performance AI Performance Networking / 5G Performance Security Features

The core generations -1

1. gen.				2. gen.	3. gen.	4. gen.	5. gen.
Core 2 New Microarch. 65 nm	Penryn New Process 45 nm	Nehalem New Microarch. 45 nm	West-mere New Process 32 nm	Sandy Bridge New Microarch. 32 nm	Ivy Bridge New Process 22 nm	Haswell New Microarchi. 22 nm	Broad-well New Process 14 nm
TOCK	***TICK***	***TOCK***	***TICK***	***TOCK***	***TICK***	***TOCK***	***TICK***
(2006)	*(2007)*	*(2008)*	*(2010)*	*(2011)*	*(2012)*	*(2013)*	*(2014)*

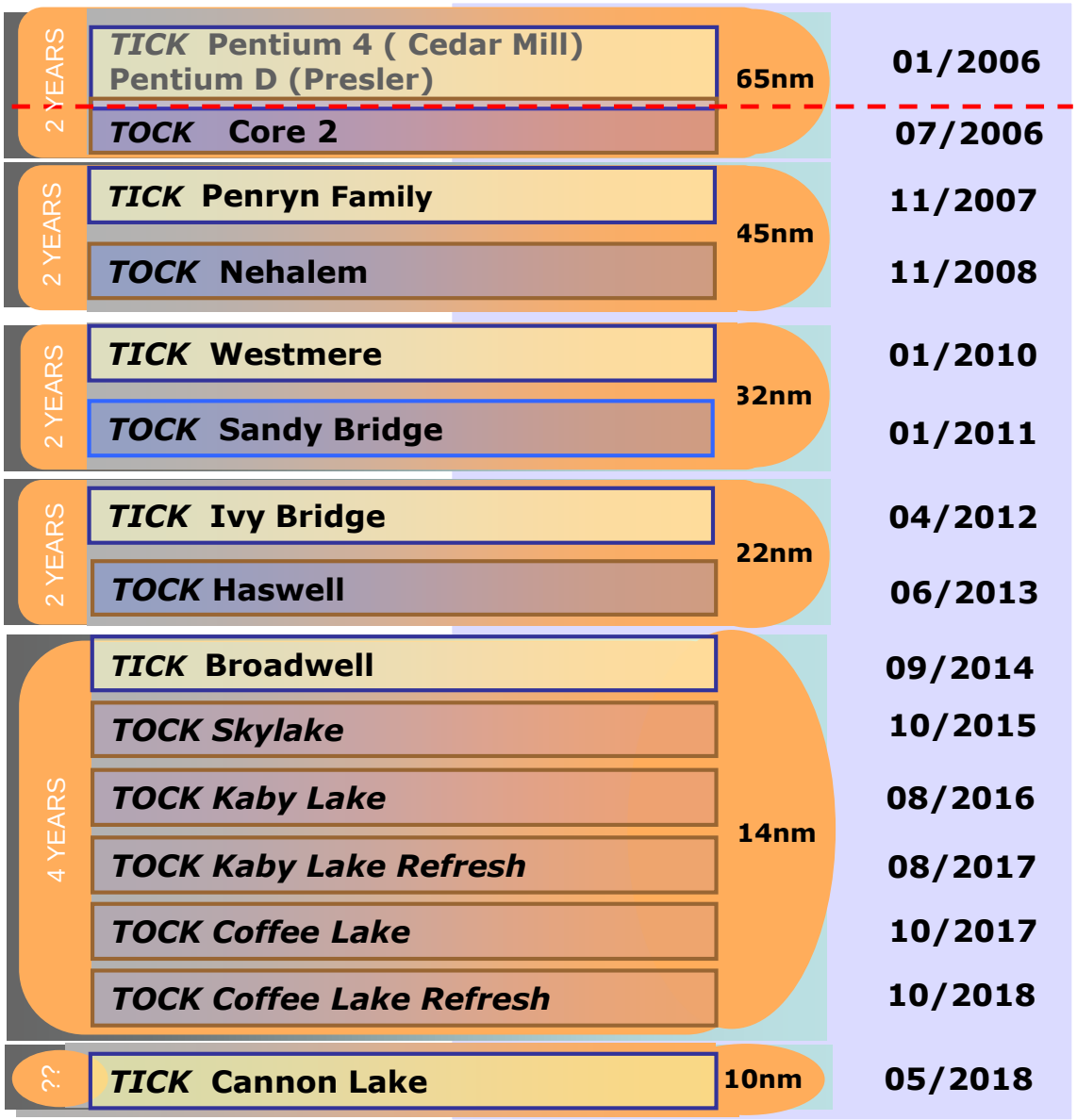
6. gen.	7. gen.	8. gen.[1]	9. gen.
Skylake New Microarch. 14 nm	Kaby Lake New Microarch. 14 nm	Kaby Lake R KL G-series Coffee Lake Cannon Lake 14/10 nm	Coffee Lake R New Mocroarch. 14 nm
TOCK	***TOCK***	***TOCK***	***TOCK***
(2015)	*(2016)*	*(2017/18)*	*(2018)*

[1]Astonishingly, the 8th generation encompasses four processor lines, as follows:

- Kaby Lake Refresh
- Kaby Lake G with AMD Vega graphics
- Coffee Lake (all 14 nm) and the
- 10 nm Cannon Lake designs [218].

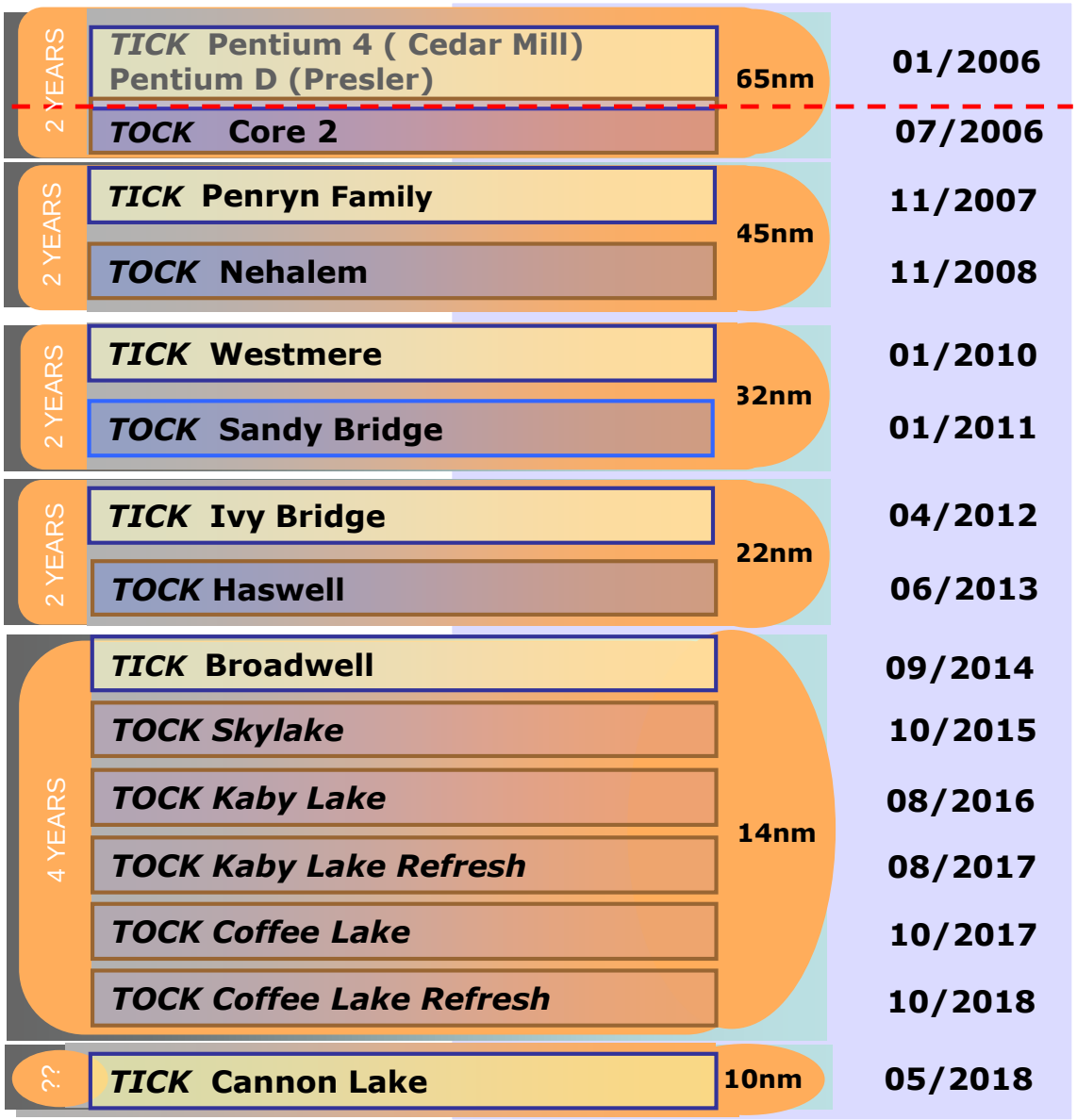
R: Refresh

The Core generations -2 (based on [3])



Key new features of the ISA and the microarchitecture

The Core generations (based on [3])



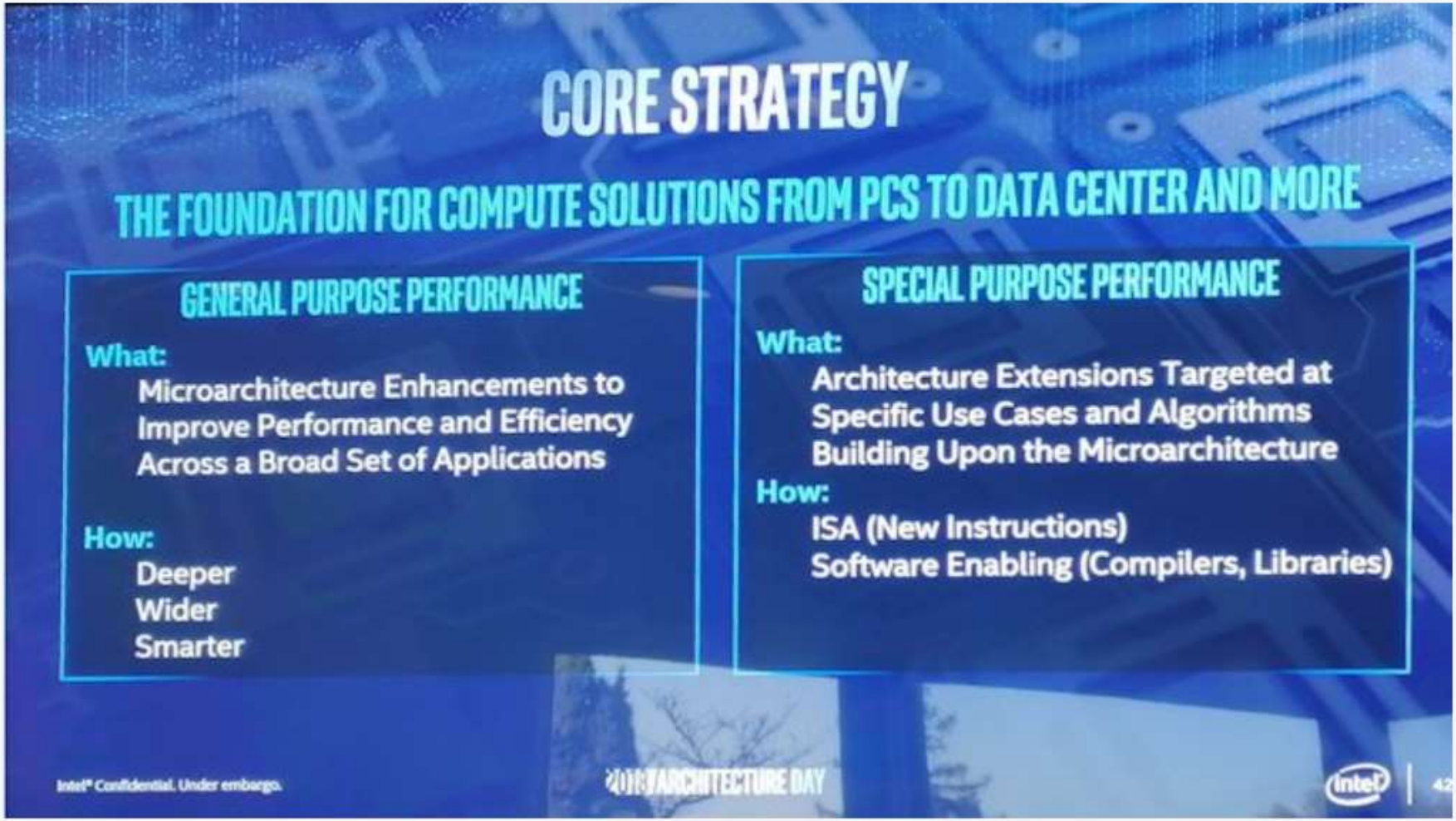
Key new features of the power management

- **Clock gating, PECI, Platform Thermal Control by 3. party controller**
- **EDAT**
- **Integrated Power Gates, PCU, Turbo Boost**
- **Turbo Boost 2.0**
- **FIVR**
- **2. gen. FIVR**
- **Speed Shift Technology, Duty Cycle control, No FIVR except Skylake X**
- **Speed Shift Technology v2**
- **In H-series: TVB (Thermal Velocity Boost)**
- **STIM**

12.2 Major enhancements of the Sunny Cove

12.2 Major enhancements of the Sunny Cove

Two main directions of increasing processor performance [296]

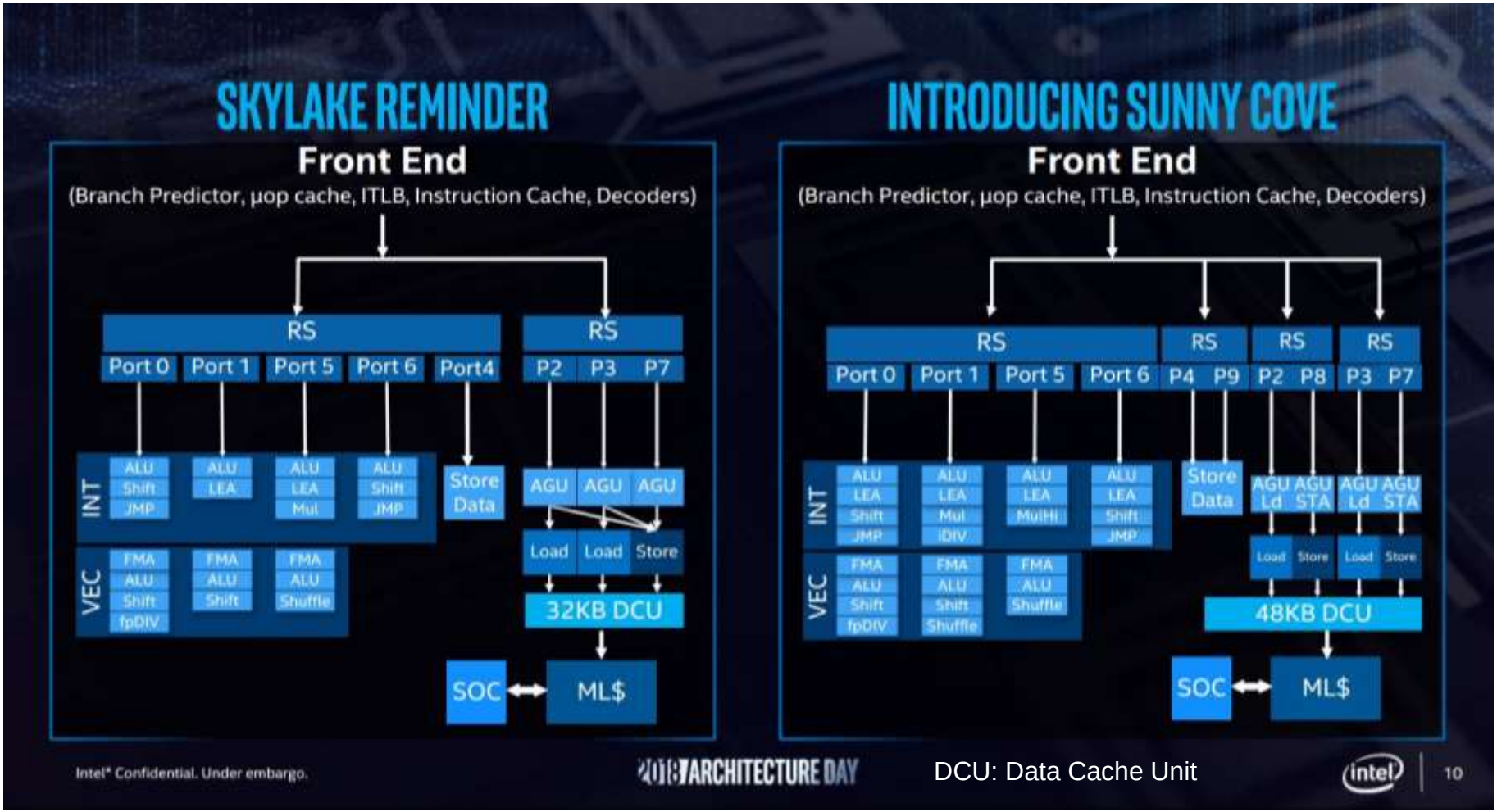


https://ww.anandtech.com/print/13699/intel-architecture-day-2018-core-future-hybrid-x86

12.2 Major enhancements of the Sunny Cove (2)

12.2.1 Microarchitecture enhancements to improve performance and efficiency across a broad range of applications in the Sunny Cove -1

Overview – Contrasting the back-ends of Skylake and Sunny Cove [297]-1



DCU: Data Cache Unit

12.2 Major enhancements of the Sunny Cove (3)

Overview – Contrasting the back-ends of Skylake and Sunny Cove -2

Note that Sunny Cove has 10 ports for issuing instructions (up from 8) implemented in the Skylake.

12.2 Major enhancements of the Sunny Cove (4)

Microarchitecture enhancements to improve performance and efficiency across a broad range of applications in the Sunny Cove -2

Main areas of enhancing the microarchitecture

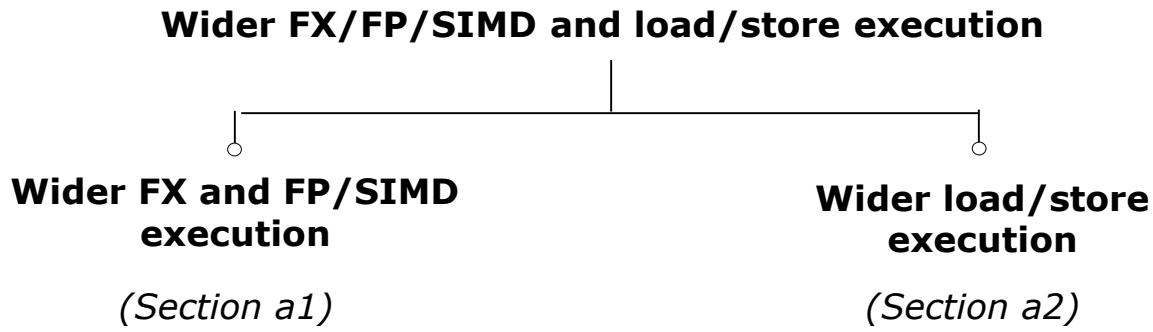
a) wider FX/FP/SIMD and load/store execution (executing more instructions per clock),

b) deeper key structures, including caches (providing more parallelism per clock cycle) and

c) smarter units (leading to processing more instructions or data)

12.2 Major enhancements of the Sunny Cove (5)

a) Wider FX/FP/SIMD and load/store execution (executing more instructions per clock)



12.2 Major enhancements of the Sunny Cove (6)

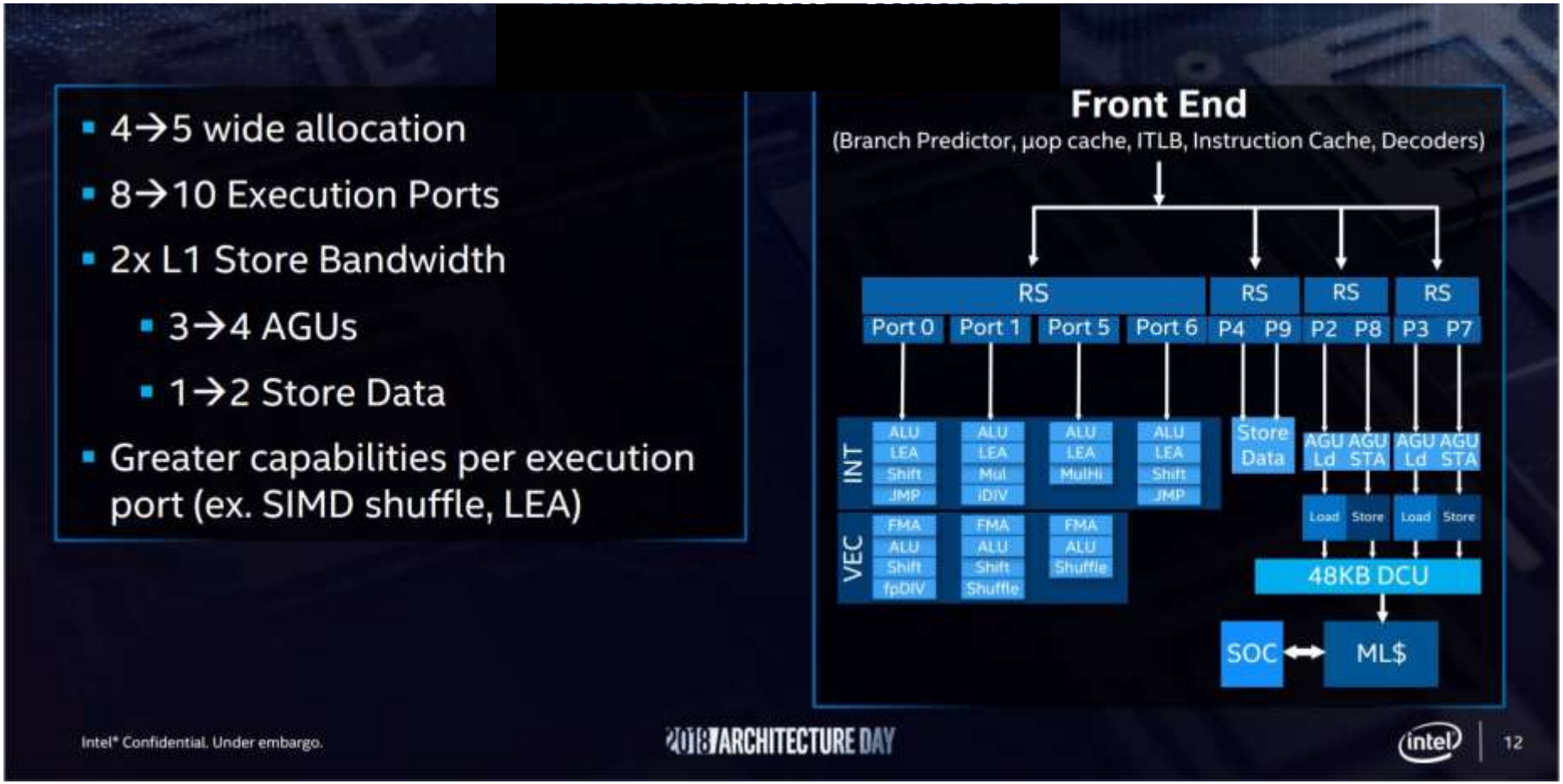
a1) Wider FX and FP/SIMD execution (over the ports 0, 1, 5, 6) [296]

Back-End Execution Resources								
Skylake				Port	Sunny Cove			
Integer								
	JMP	Shift	ALU	**0**	ALU	**LEA**	Shift	JMP
		LEA	ALU	**1**	ALU	LEA	**Mul**	**iDIV**
	Mul	LEA	ALU	**5**	ALU	LEA	**MulHi**	
	JMP	Shift	ALU	**6**	ALU	**LEA**	Shift	JMP
Vector / FP								
fpDIV	Shift	ALU	FMA	**0**	FMA	ALU	Shift	fpDIV
	Shift	ALU	FMA	**1**	FMA	ALU	Shift	**Shuffle**
	Shuffle	ALU	FMA	**5**	FMA	ALU	Shuffle	

https://www.anandtech.com/print/13699/intel-architecture-day-2018-core-future-hybrid-x86

12.2 Major enhancements of the Sunny Cove (7)

a2) Wider load/store execution (over the ports 2, 3, 4, 7, 8, 9) [297] -1



12.2 Major enhancements of the Sunny Cove (8)

Wider load/store execution (over the ports 2, 3, 4, 7, 8, 9) [296] -2

Compared with Skylake, Sunny Cove will be capable of issuing dual loads and dual stores per cycle, rather than dual loads and a single store per cycle, as in the Skylake.

12.2 Major enhancements of the Sunny Cove (9)

Wider load/store execution (over the ports 2, 3, 4, 7, 8, 9) [296] -2

Compared with Skylake, Sunny Cove will be capable of issuing dual loads and dual stores per cycle, rather than dual loads and a single store per cycle, as in the Skylake.

12.2 Major enhancements of the Sunny Cove (10)

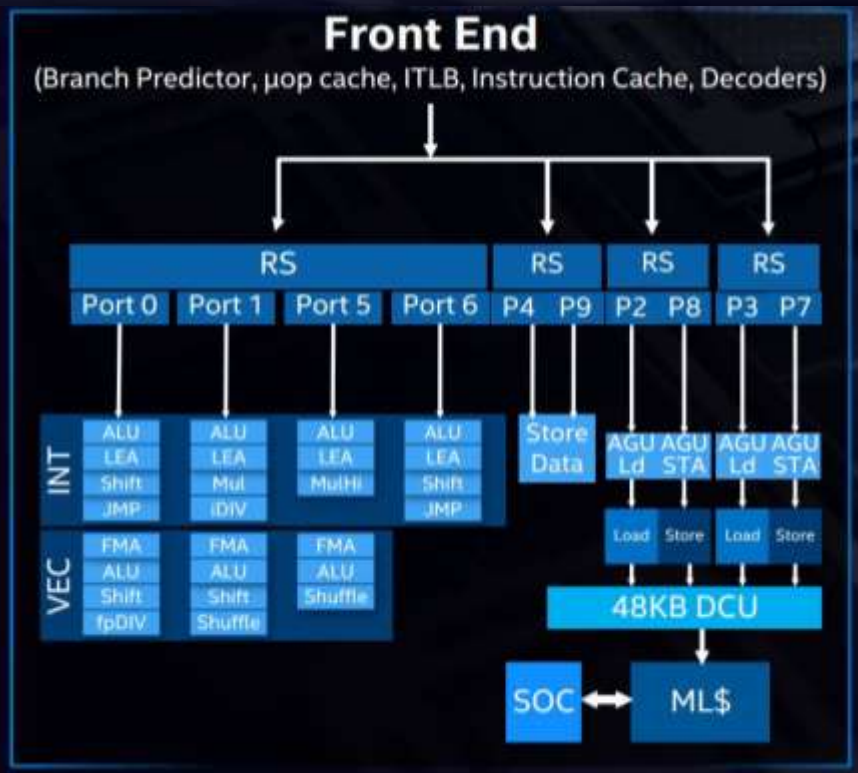
b) Deeper key structures, including caches (providing more parallelism per clock cycle) [297]

Significant increase in size of key structures

Reorder Buffer, Load Buffer, Store Buffer, Reservation Stations

Caches:

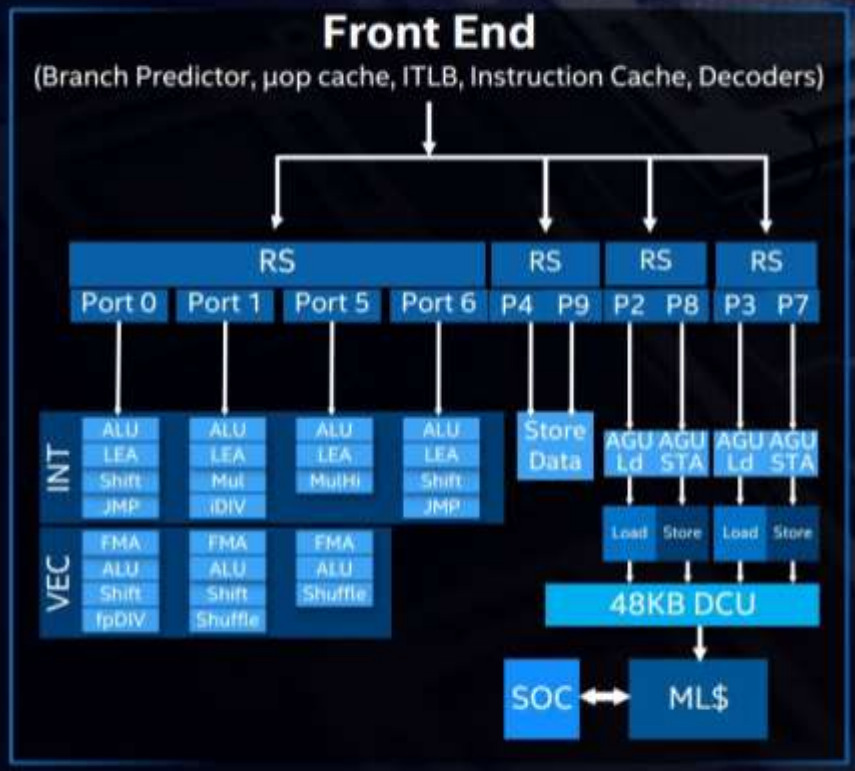
- 50% increase in size of the L1 Data Cache (now 48 KB vs 32 KB)
- Larger L2 cache (size is product dependent)
- Larger µop cache
- Larger 2nd level TLB



12.2 Major enhancements of the Sunny Cove (11)

c) Smarter units (leading to processing more instructions or data) [297] -1

- Larger Buffers
  - New algorithms required to scale
  - Branch prediction accuracy improvements critical
- Example Latency Improvements
  - Reduced Effective Load Latency
  - Integer Divider



12.2 Major enhancements of the Sunny Cove (12)

c) Smarter units (leading to processing more instructions or data) -2

In this respect Intel improved branch prediction accuracy, with additional latency improvements, like load latency and a implemented a new faster integer divider unit.

12.2 Major enhancements of the Sunny Cove (13)

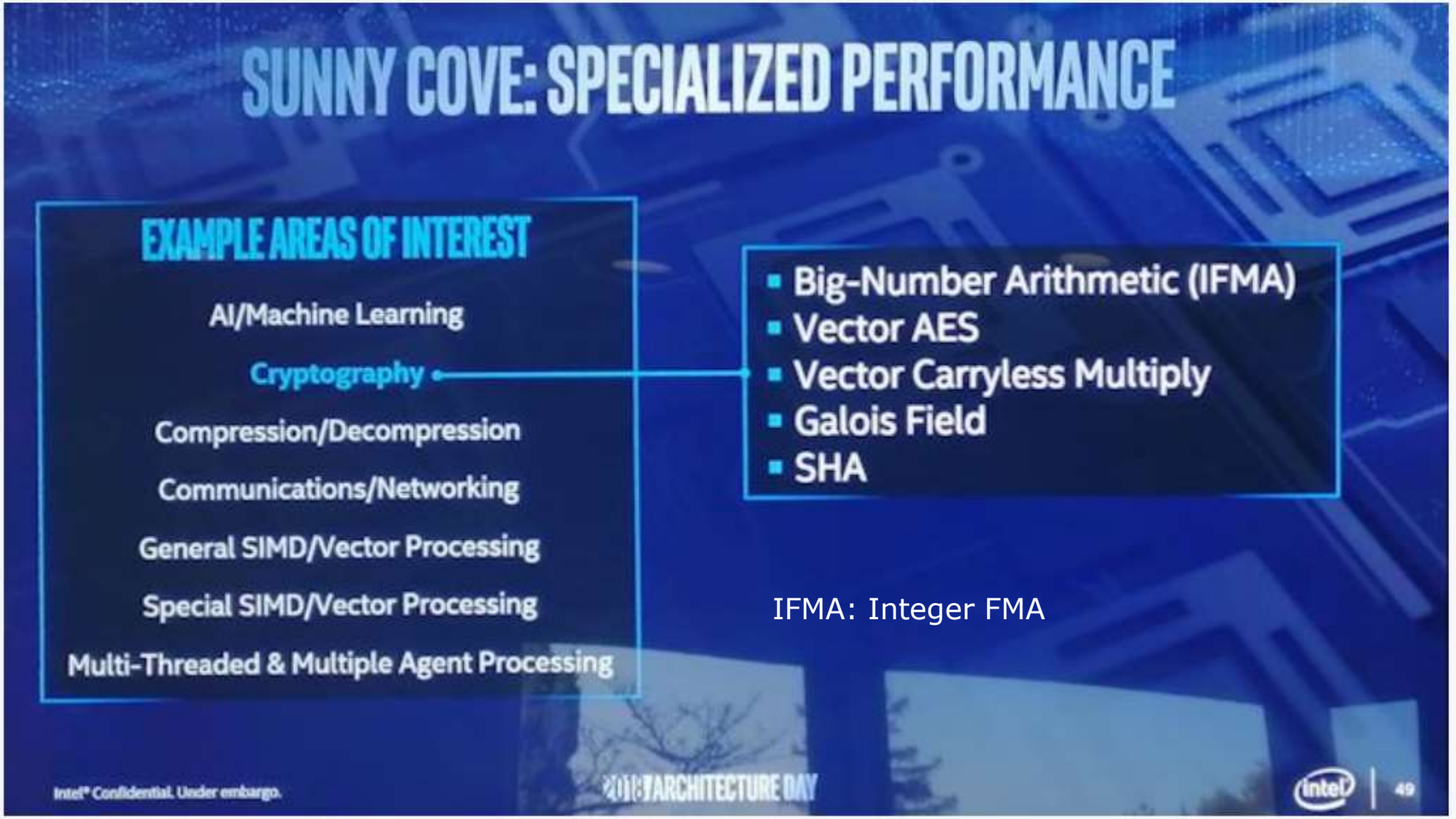
13.2.2 Architecture extensions targeting specific use cases and algorithms, building upon the microarchitecture [296], [297]

In addition to the microarchitecture enhancements Sunny Cove introduces the following architecture extensions:

- new instructions to speed up special fields of interest (see subsequently),
- 57 bits linear address space,
- 52-bits physical address space, allowing to address 4 PetaB per socket,
- five levels of paging tables, up from four, and
- new security modes, including User Mode Instruction Prevention, that forbids (if enabled) the execution of certain instructions if the Current Privilege Level (CPL) is greater than 0.

  Then user space applications can no longer access system-wide settings, such as the global and local descriptor tables, the task register and the interrupt descriptor table.

Special areas of interest for improving performance [296]



IFMA: Integer FMA