

# Intel's Core 2 family - TOCK lines Sunny Cove

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Vers. 1.0

Januar 2019

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## 12. Sunny Cove

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## 12.1 Introduction to the Sunny Cove

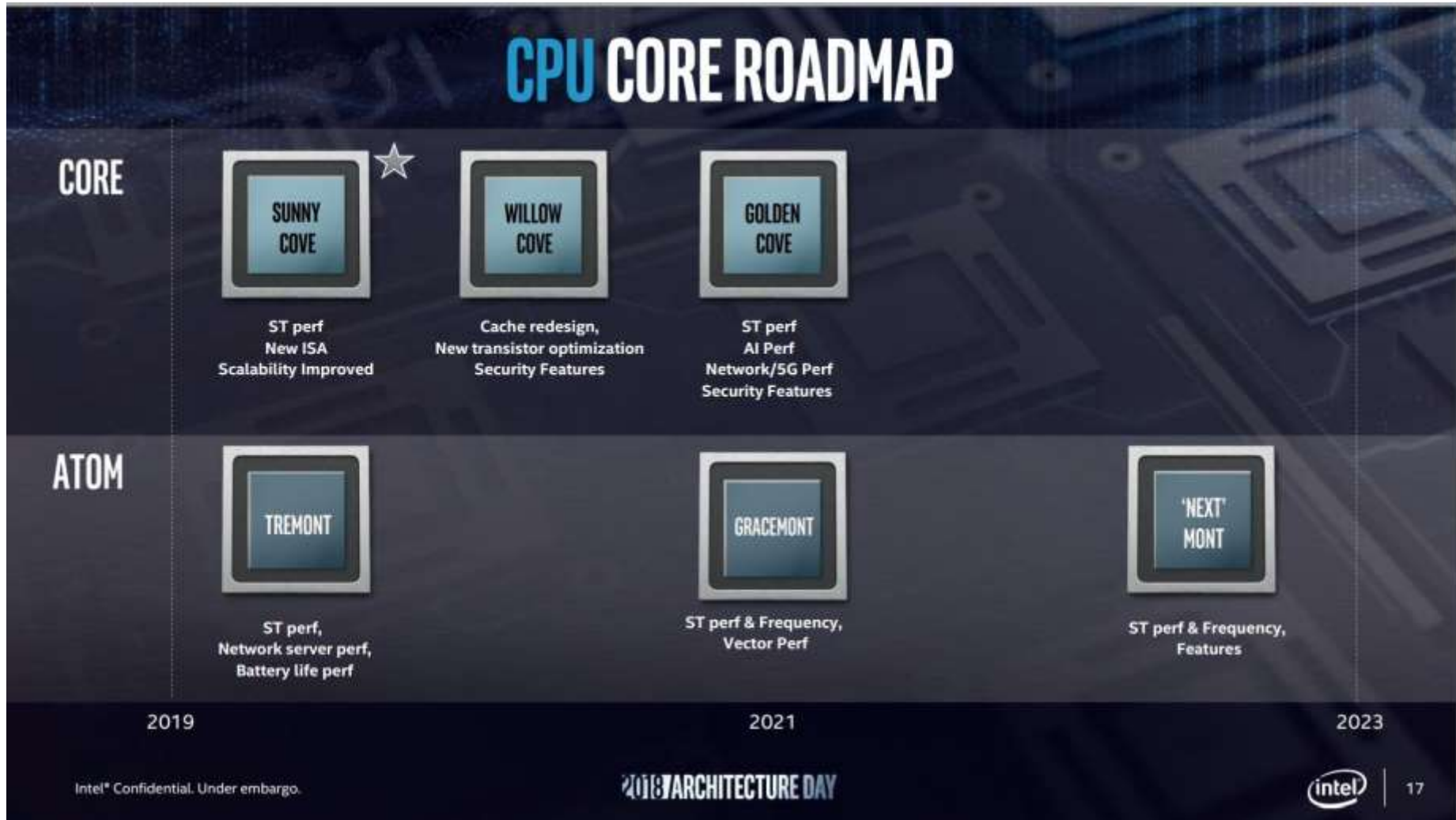
## 12.1 Introduction to the Sunny Cove (1)

### 12.1 Introduction to the Sunny Cove [296]

- Announced in 12/2018 at Intel's Architecture Day, to be launched in 2019.
- Manufactured on Intel's 10 nm technology.
- Presumably, the Sunny Cove cores paired with Gen11 graphics will yield the Ice Lake processor.
- Sunny Cove cores offer increased single-threaded performance, new instructions, and improved scalability

# 12.1 Introduction to the Sunny Cove (2)

Intel's CPU roadmap 2019 – 2022 [297]



# 12.1 Introduction to the Sunny Cove (3)

## Evolution of Intel's manufacturing technology [296]

Intel Core Microarchitecture Roadmap			
Core Name	Year	Process Node	Improvements
<b>Skylake</b>	2015	14 nm	Single Threaded Performance Lower Power Other Optimizations
<b>Kaby Lake</b>	2016	14 nm+	Frequency
<b>Coffee Lake</b>	2017	14 nm++	Frequency
<b>Coffee Refresh</b>	2018	14 nm++	Frequency
<b>Sunny Cove</b>	2019	10 nm	Single Threaded Performance New Instructions Improved Scalability
<b>Willow Cove</b>	2020 ?	10 nm ?	Cache Redesign New Transistor Optimization Security Features
<b>Golden Cove</b>	2021 ?	7 / 10 nm ?	Single Threaded Performance AI Performance Networking / 5G Performance Security Features



# 12.1 Introduction to the Sunny Cove (4)

## The core generations -1

1. gen.				2. gen.	3. gen.	4. gen.	5. gen.
<b>Core 2</b>	<b>Penryn</b>	<b>Nehalem</b>	<b>Westmere</b>	<b>Sandy Bridge</b>	<b>Ivy Bridge</b>	<b>Haswell</b>	<b>Broadwell</b>
New Microarch.	New Process	New Microarch.	New Process	New Microarch.	New Process	New Microarchi.	New Process
65 nm	45 nm	45 nm	32 nm	32 nm	22 nm	22 nm	14 nm
<b>TOCK</b>	<b>TICK</b>	<b>TOCK</b>	<b>TICK</b>	<b>TOCK</b>	<b>TICK</b>	<b>TOCK</b>	<b>TICK</b>
(2006)	(2007)	(2008)	(2010)	(2011)	(2012)	(2013)	(2014)

6. gen.	7. gen.	8. gen. <sup>1</sup>	9. gen.
<b>Skylake</b>	<b>Kaby Lake</b>	<b>Kaby Lake R</b> <b>KL G-series</b> <b>Coffee Lake</b> <b>Cannon Lake</b>	<b>Coffee Lake R</b>
New Microarch.	New Microarch.		New Mocroarch.
14 nm	14 nm	14/10 nm	14 nm
<b>TOCK</b>	<b>TOCK</b>	<b>TOCK</b>	<b>TOCK</b>
(2015)	(2016)	(2017/18)	(2018)

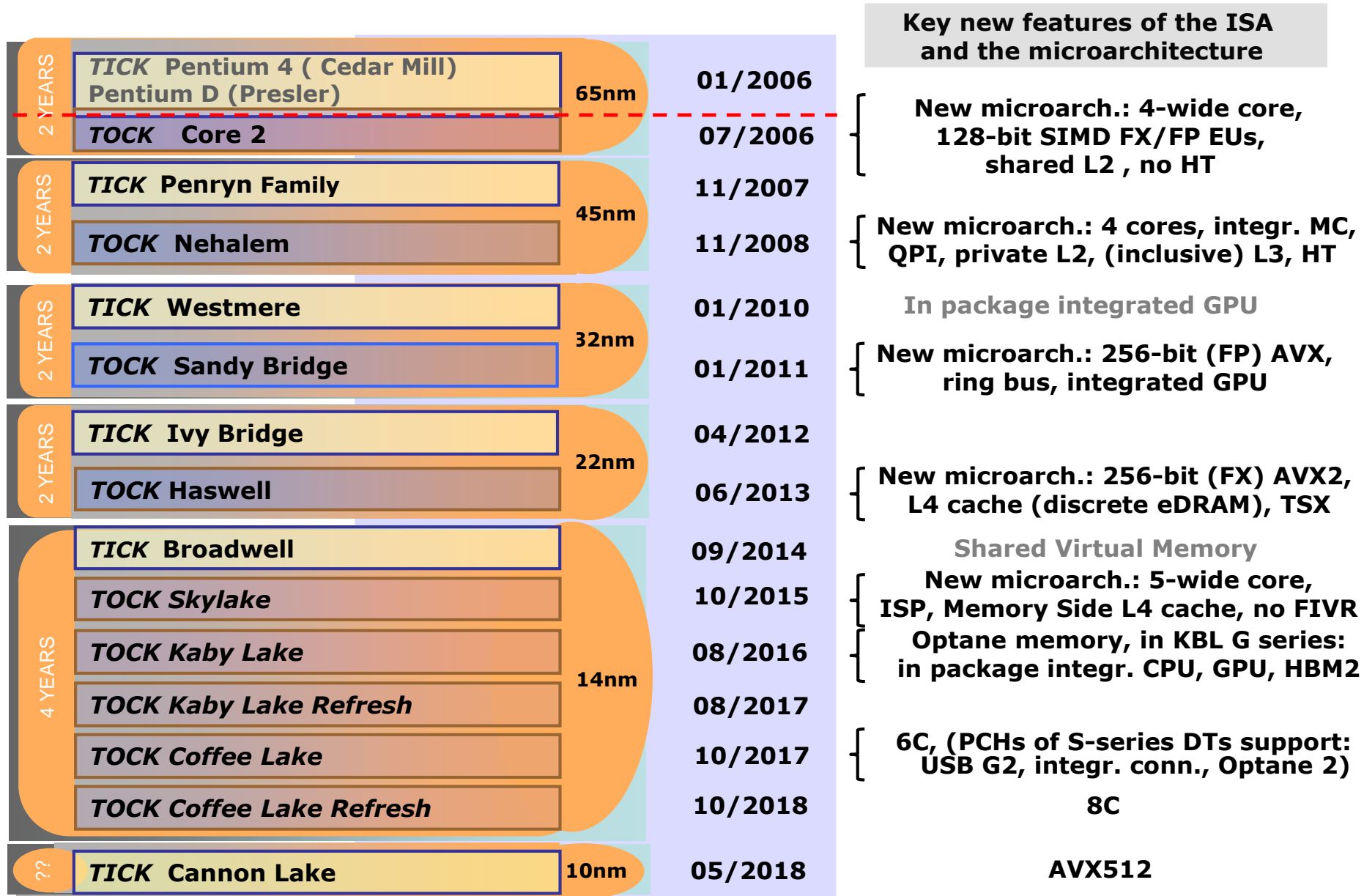
<sup>1</sup>Astonishingly, the 8th generation encompasses four processor lines, as follows:

- Kaby Lake Refresh
- Kaby Lake G with AMD Vega graphics
- Coffee Lake (all 14 nm) and the
- 10 nm Cannon Lake designs [218].

R: Refresh

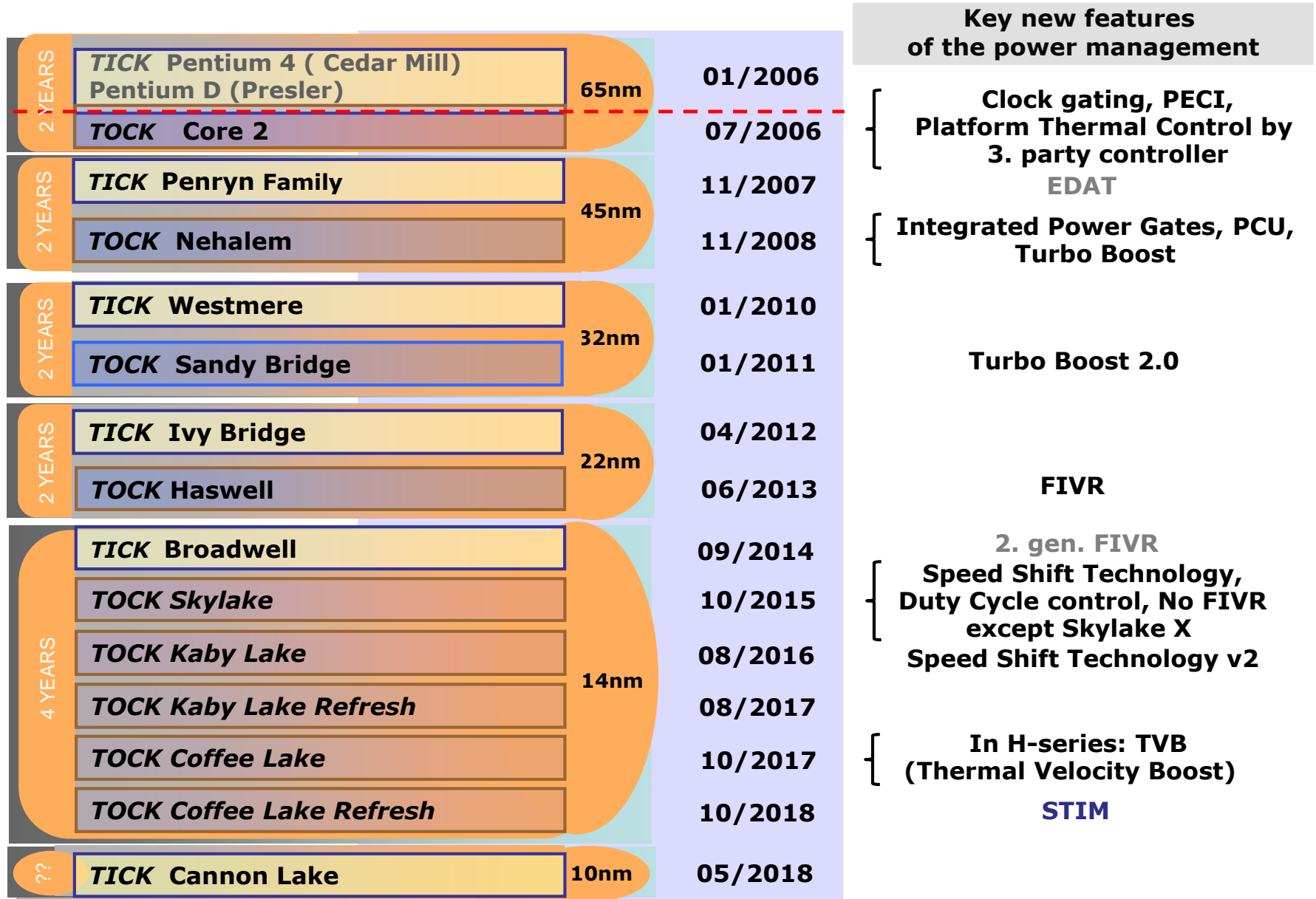
# 12.1 Introduction to the Sunny Cove (5)

## The Core generations -2 (based on [3])



# 12.1 Introduction to the Sunny Cove (6)

The Core generations ( based on [3])

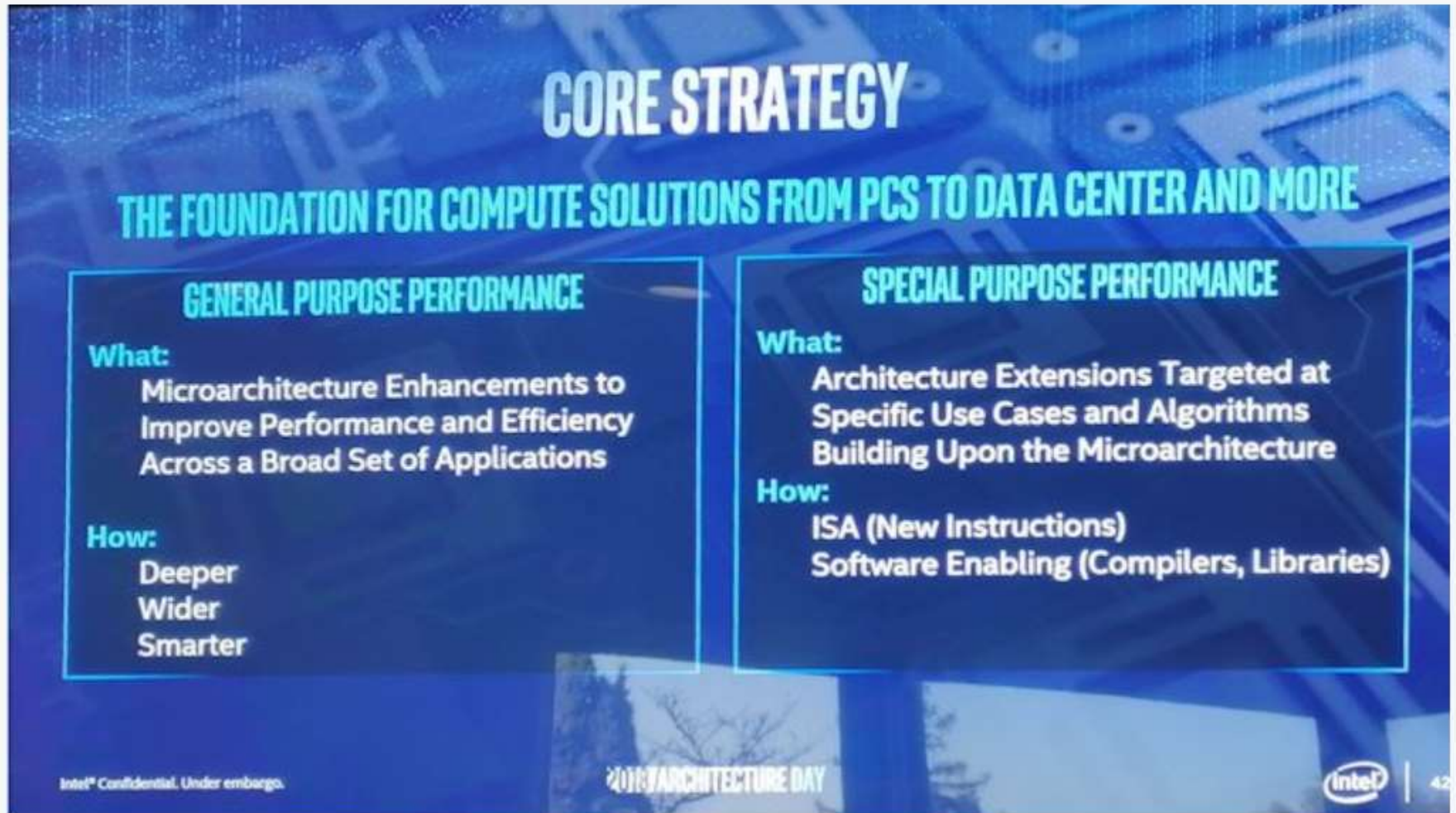


## 12.2 Major enhancements of the Sunny Cove

## 12.2 Major enhancements of the Sunny Cove (1)

### 12.2 Major enhancements of the Sunny Cove

Two main directions of increasing processor performance [296]



The slide features a blue background with a faint image of a microchip. At the top, the text 'CORE STRATEGY' is written in large, white, bold letters. Below it, 'THE FOUNDATION FOR COMPUTE SOLUTIONS FROM PCS TO DATA CENTER AND MORE' is written in smaller, light blue, bold letters. Two white-bordered boxes are positioned in the center, each containing text about performance. The left box is titled 'GENERAL PURPOSE PERFORMANCE' and the right box is titled 'SPECIAL PURPOSE PERFORMANCE'. At the bottom left, there is a small text 'Intel® Confidential. Under embargo.' At the bottom center, there is a logo for 'ARCHITECTURE DAY' and at the bottom right, the Intel logo and the number '42'.

# CORE STRATEGY

## THE FOUNDATION FOR COMPUTE SOLUTIONS FROM PCS TO DATA CENTER AND MORE

GENERAL PURPOSE PERFORMANCE	SPECIAL PURPOSE PERFORMANCE
<b>What:</b> Microarchitecture Enhancements to Improve Performance and Efficiency Across a Broad Set of Applications	<b>What:</b> Architecture Extensions Targeted at Specific Use Cases and Algorithms Building Upon the Microarchitecture
<b>How:</b> Deeper Wider Smarter	<b>How:</b> ISA (New Instructions) Software Enabling (Compilers, Libraries)

Intel® Confidential. Under embargo.

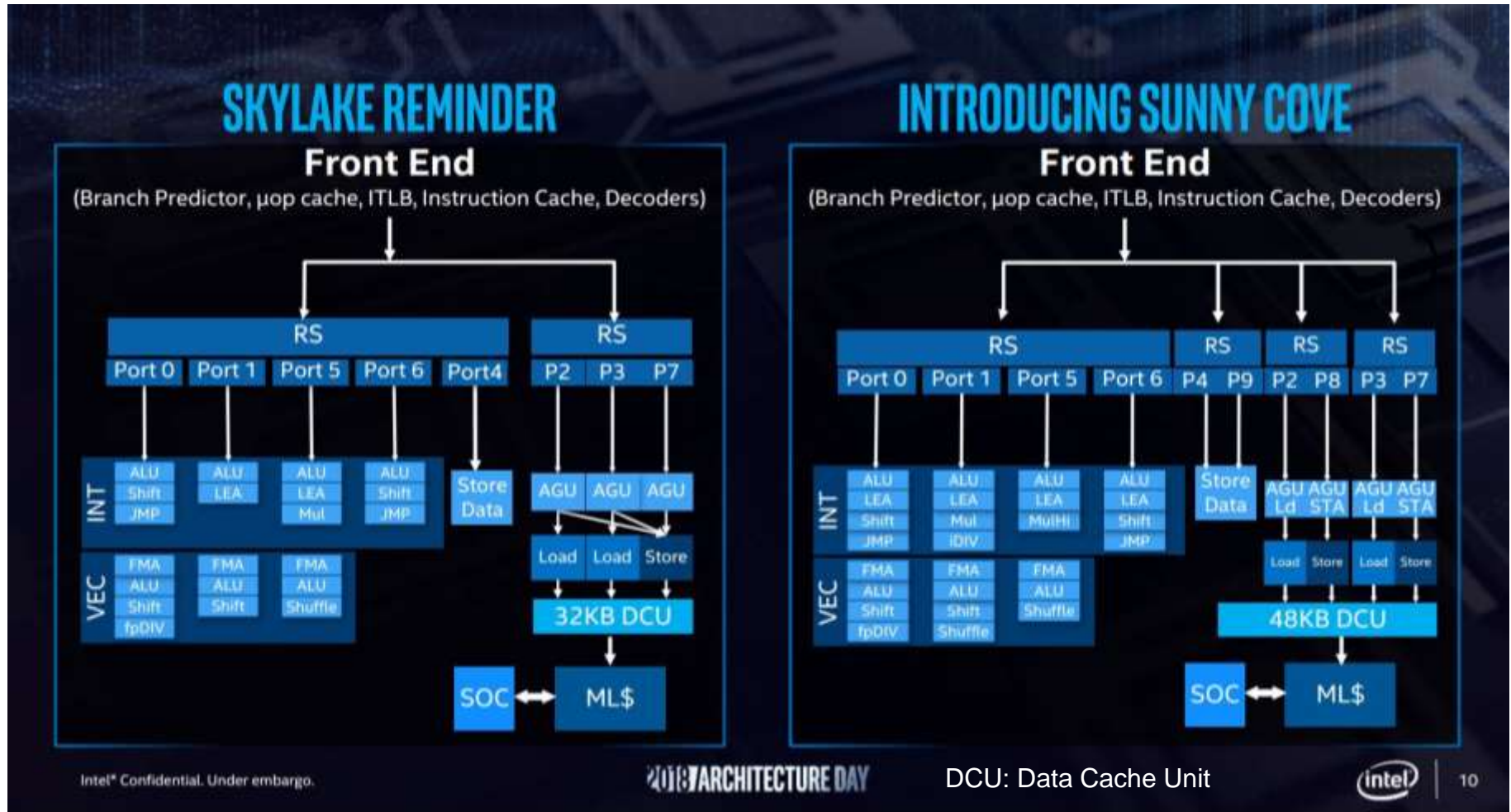
ARCHITECTURE DAY

Intel | 42

## 12.2 Major enhancements of the Sunny Cove (2)

### 12.2.1 Microarchitecture enhancements to improve performance and efficiency across a broad range of applications in the Sunny Cove -1

#### Overview – Contrasting the back-ends of Skylake and Sunny Cove [297 ]-1



## 12.2 Major enhancements of the Sunny Cove (3)

Overview – Contrasting the back-ends of Skylake and Sunny Cove -2

**Note** that Sunny Cove has **10 ports** for issuing instructions (**up from 8**) implemented in the Skylake.

## 12.2 Major enhancements of the Sunny Cove (4)

Microarchitecture enhancements to improve performance and efficiency across a broad range of applications in the Sunny Cove -2

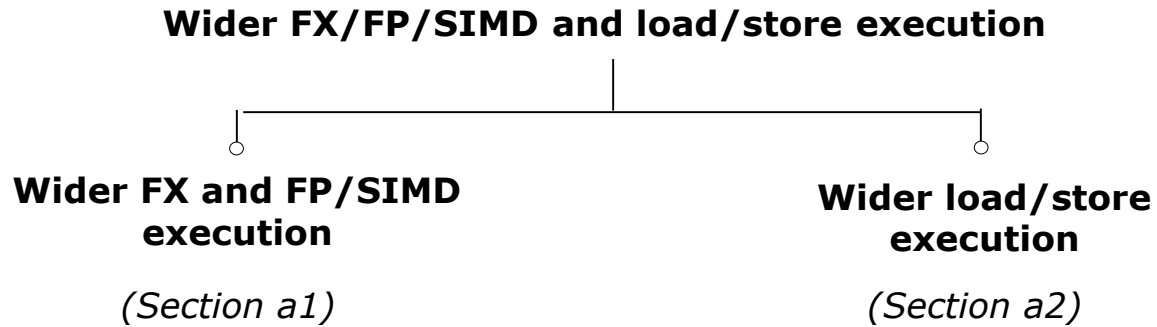
Main areas of enhancing the microarchitecture

- a) **wider** FX/FP/SIMD and load/store execution (executing more instructions per clock),
- b) **deeper** key structures, including caches (providing more parallelism per clock cycle) and
- c) **smarter** units (leading to processing more instructions or data)



## 12.2 Major enhancements of the Sunny Cove (5)

a) Wider FX/FP/SIMD and load/store execution (executing more instructions per clock)



## 12.2 Major enhancements of the Sunny Cove (6)

a1) Wider FX and FP/SIMD execution (over the ports 0, 1, 5, 6) [296]

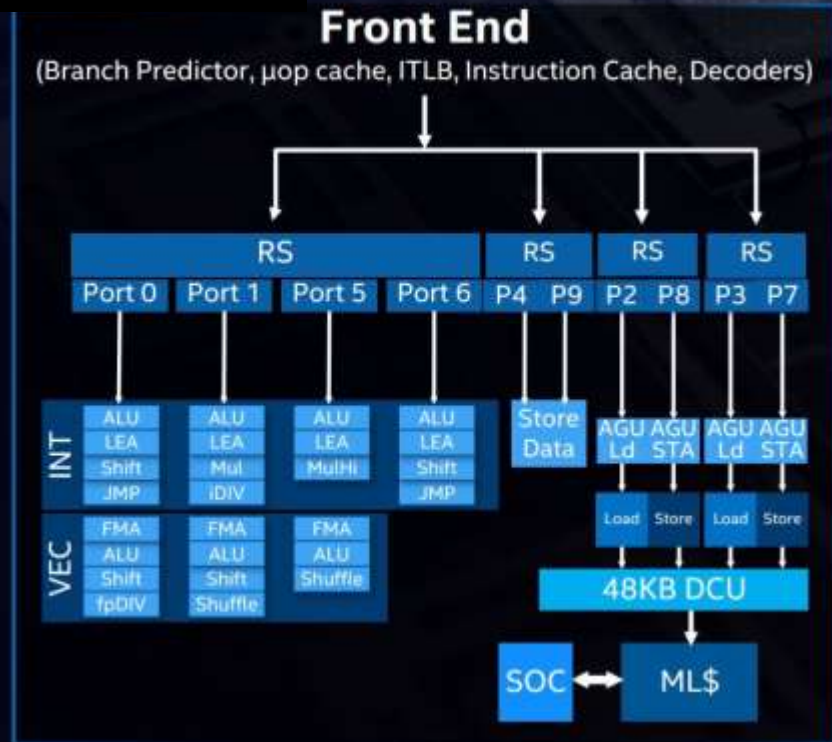
### Back-End Execution Resources

Skylake				Port	Sunny Cove			
<b>Integer</b>								
	JMP	Shift	ALU	<b>0</b>	ALU	<b>LEA</b>	Shift	JMP
		LEA	ALU	<b>1</b>	ALU	LEA	<b>Mul</b>	<b>iDIV</b>
	Mul	LEA	ALU	<b>5</b>	ALU	LEA	<b>MulHi</b>	
	JMP	Shift	ALU	<b>6</b>	ALU	<b>LEA</b>	Shift	JMP
<b>Vector / FP</b>								
fpDIV	Shift	ALU	FMA	<b>0</b>	FMA	ALU	Shift	fpDIV
	Shift	ALU	FMA	<b>1</b>	FMA	ALU	Shift	<b>Shuffle</b>
	Shuffle	ALU	FMA	<b>5</b>	FMA	ALU	Shuffle	

## 12.2 Major enhancements of the Sunny Cove (7)

a2) Wider load/store execution (over the ports 2, 3, 4, 7, 8, 9) [297] -1

- 4→5 wide allocation
- 8→10 Execution Ports
- 2x L1 Store Bandwidth
  - 3→4 AGUs
  - 1→2 Store Data
- Greater capabilities per execution port (ex. SIMD shuffle, LEA)



## 12.2 Major enhancements of the Sunny Cove (8)

Wider load/store execution (over the ports 2, 3, 4, 7, 8, 9) [296] -2

Compared with Skylake, Sunny Cove will be capable of issuing dual **loads and dual stores per cycle**, rather than dual loads and a single store per cycle, as in the Skylake.

## 12.2 Major enhancements of the Sunny Cove (9)

Wider load/store execution (over the ports 2, 3, 4, 7, 8, 9) [296] -2

Compared with Skylake, Sunny Cove will be capable of issuing dual **loads and dual stores per cycle**, rather than dual loads and a single store per cycle, as in the Skylake.

## 12.2 Major enhancements of the Sunny Cove (10)

- b) Deeper key structures, including caches (providing more parallelism per clock cycle) [297]

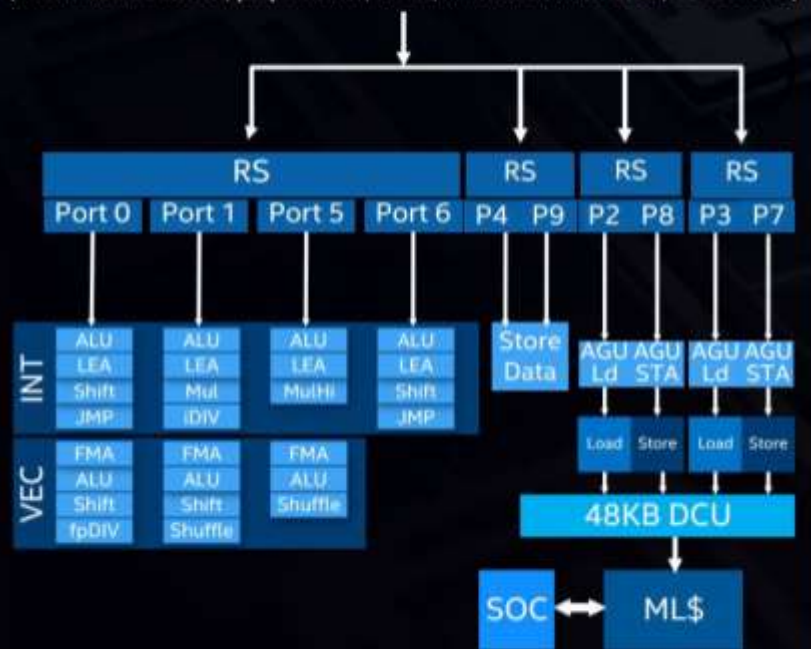
### Significant increase in size of key structures

*Reorder Buffer, Load Buffer, Store Buffer, Reservation Stations*

### Caches:

- 50% increase in size of the L1 Data Cache (now 48 KB vs 32 KB)
- Larger L2 cache (size is product dependent)
- Larger  $\mu$ op cache
- Larger 2nd level TLB

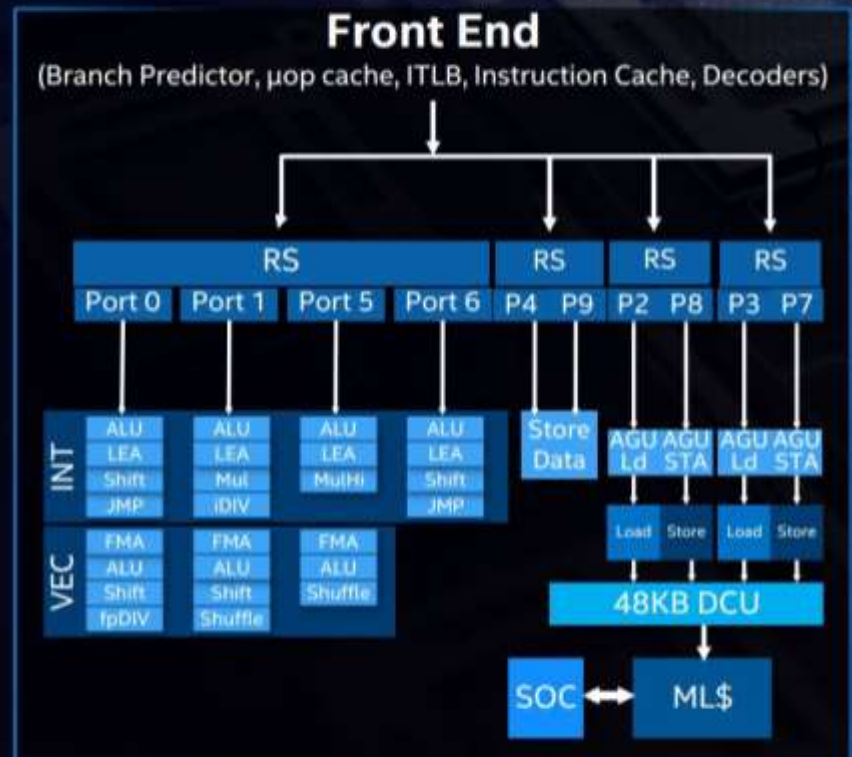
### Front End (Branch Predictor, $\mu$ op cache, ITLB, Instruction Cache, Decoders)



## 12.2 Major enhancements of the Sunny Cove (11)

c) Smarter units (leading to processing more instructions or data) [297] -1

- Larger Buffers
  - New algorithms required to scale
  - Branch prediction accuracy improvements critical
- Example Latency Improvements
  - Reduced Effective Load Latency
  - Integer Divider



## 12.2 Major enhancements of the Sunny Cove (12)

c) Smarter units (leading to processing more instructions or data) -2

In this respect Intel improved branch prediction accuracy, with additional latency improvements, like load latency and implemented a new faster integer divider unit.



## 12.2 Major enhancements of the Sunny Cove (13)

### 13.2.2 Architecture extensions targeting specific use cases and algorithms, building upon the microarchitecture [296], [297]

In addition to the microarchitecture enhancements Sunny Cove introduces the following **architecture extensions**:

- **new instructions** to speed up special fields of interest (see subsequently),
- **57 bits linear address space**,
- **52-bits physical address space**, allowing to address 4 PetaB per socket,
- **five levels of paging tables**, up from four, and
- **new security modes**, including User Mode Instruction Prevention, that forbids (if enabled) the execution of certain instructions if the Current Privilege Level (CPL) is greater than 0.

Then user space applications can no longer access system-wide settings, such as the global and local descriptor tables, the task register and the interrupt descriptor table.

## 12.2 Major enhancements of the Sunny Cove ()

Special areas of interest for improving performance [296]

# SUNNY COVE: SPECIALIZED PERFORMANCE

## EXAMPLE AREAS OF INTEREST

AI/Machine Learning

**Cryptography**

Compression/Decompression

Communications/Networking

General SIMD/Vector Processing

Special SIMD/Vector Processing

Multi-Threaded & Multiple Agent Processing

- Big-Number Arithmetic (IFMA)
- Vector AES
- Vector Carryless Multiply
- Galois Field
- SHA

IFMA: Integer FMA