Intel’s Atom lines

- 1. Introduction to Intel’s Atom lines
- 2. Intel’s low-power oriented CPU micro-architectures
- 3. Atom-based platforms targeting entry level desktops and notebooks
- 4. Atom-based platforms targeting tablets
- 5. Atom-based platforms targeting smartphones
- 6. Intel’s withdrawal from the mobile market
- 7. References

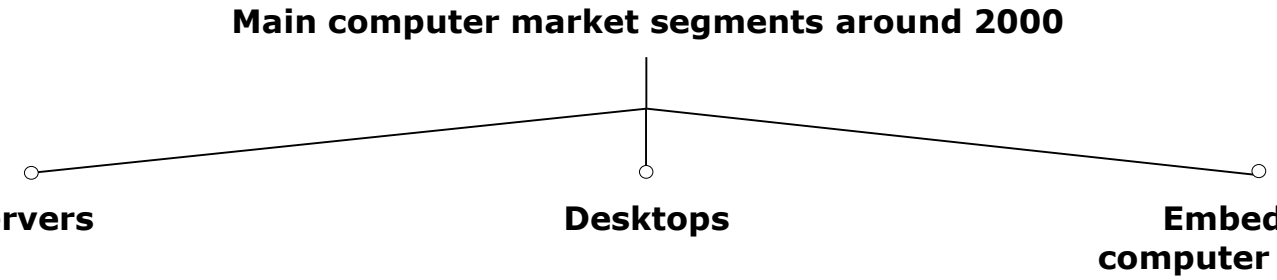
1. Introduction to Intel's Atom lines

- 1.1 The rapidly increasing importance of the mobile market space
- 1.2 Related terminology
- 1.3 Introduction to Intel's low-power Atom series

1.1 The rapidly increasing importance of the mobile market space

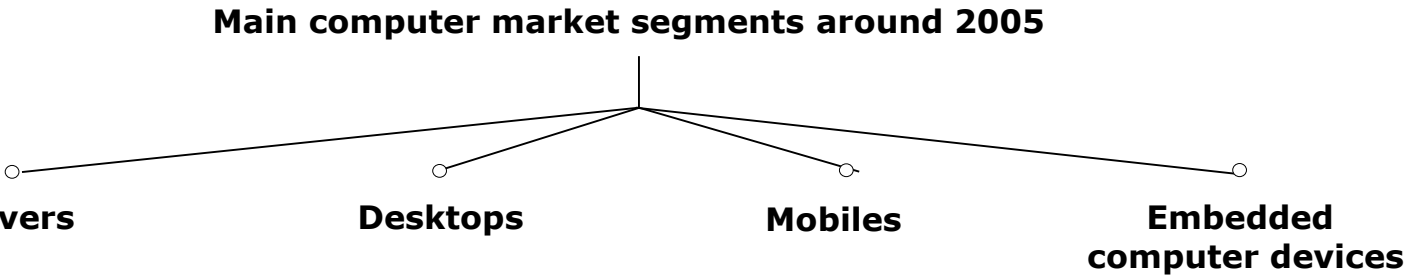
1.1 The rapidly increasing importance of the mobile market space

Diversification of computer market segments in the 2000's



E.g.	*Intel's Xeon lines* *AMD's Opteron lines*	*Intel's Pentium 4 lines* *AMD's Athlon lines*	*ARM's lines*

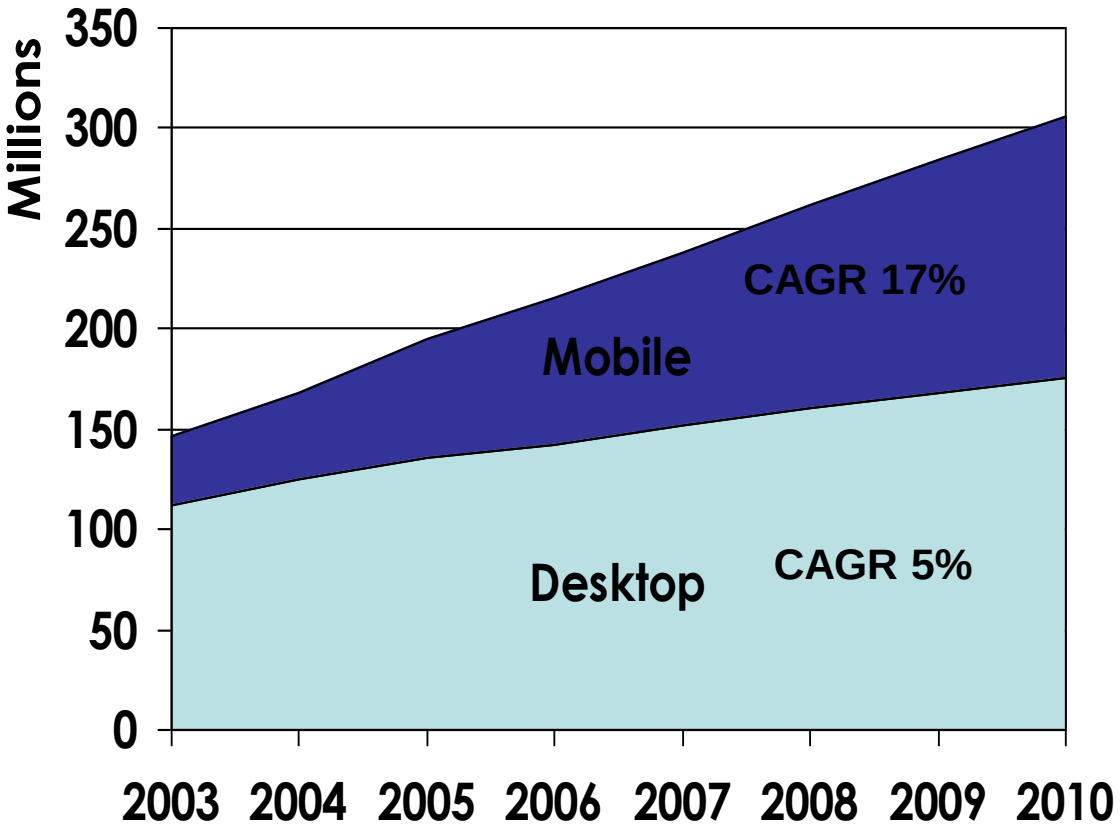
Major trend in the first half of the 2000's: spreading of mobile devices (laptops)



E.g.	*Intel's Xeon lines* *AMD's Opteron lines*	*Intel's Pentium 4 lines* *AMD's Athlon64 lines*	Intel's Celeron lines AMD's Duron lines	*ARM's lines*

1.1 The rapidly increasing importance of the mobile market space (2)

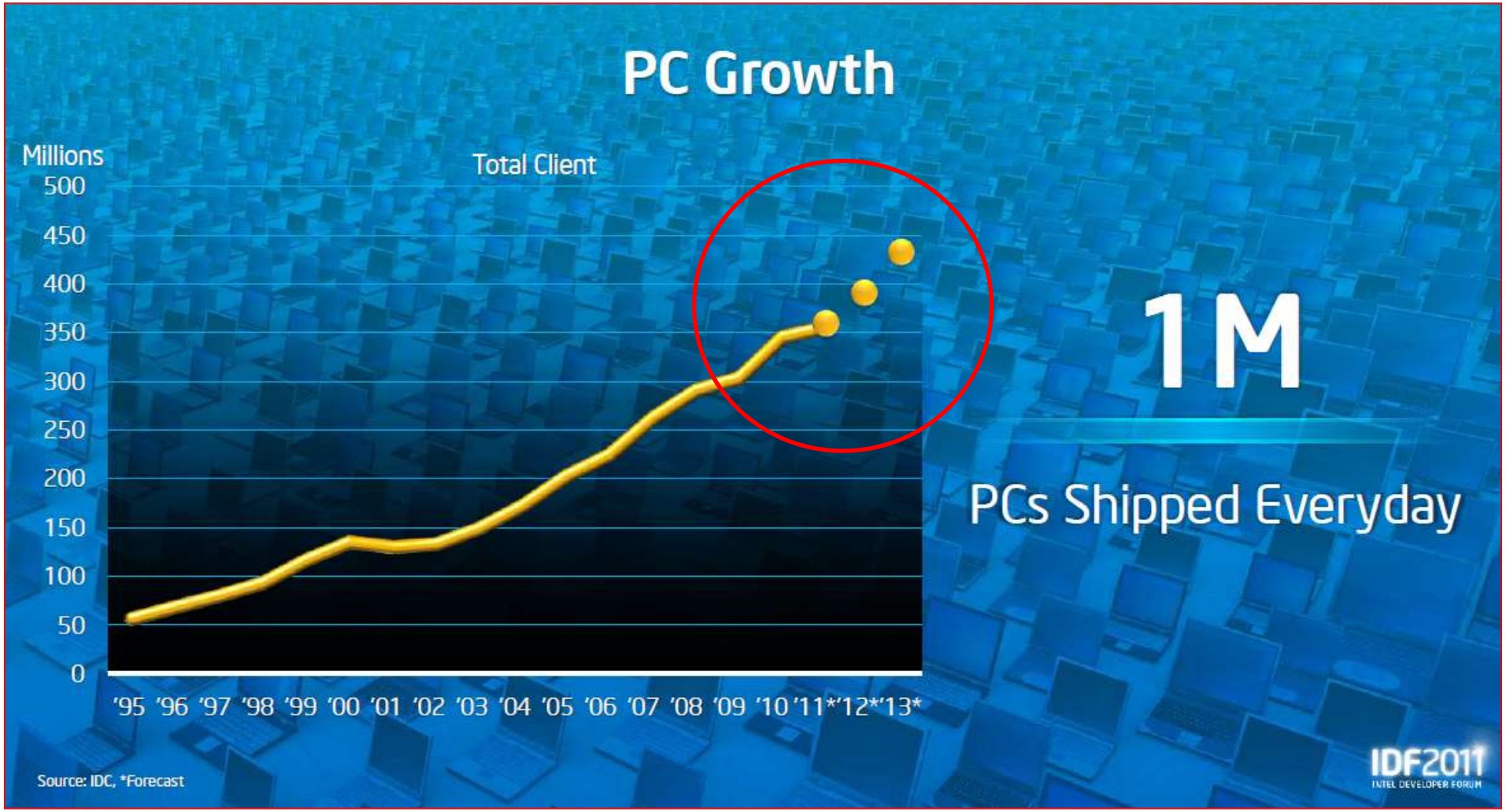
Yearly worldwide sales and Compound Annual Growth Rates (CAGR) of desktops and mobiles (laptops) around 2005 [1]



Source: IDC March 2006

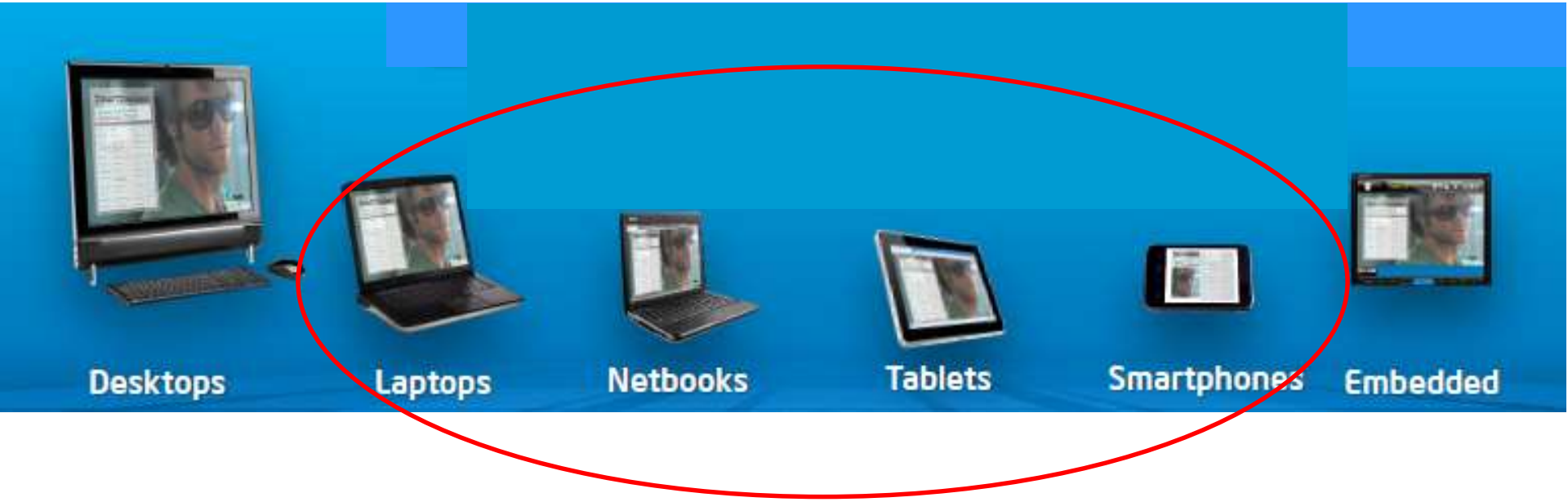
1.1 The rapidly increasing importance of the mobile market space (3)

Desktop and notebook sales figures and forecast from 2011 [2]



1.1 The rapidly increasing importance of the mobile market space (4)

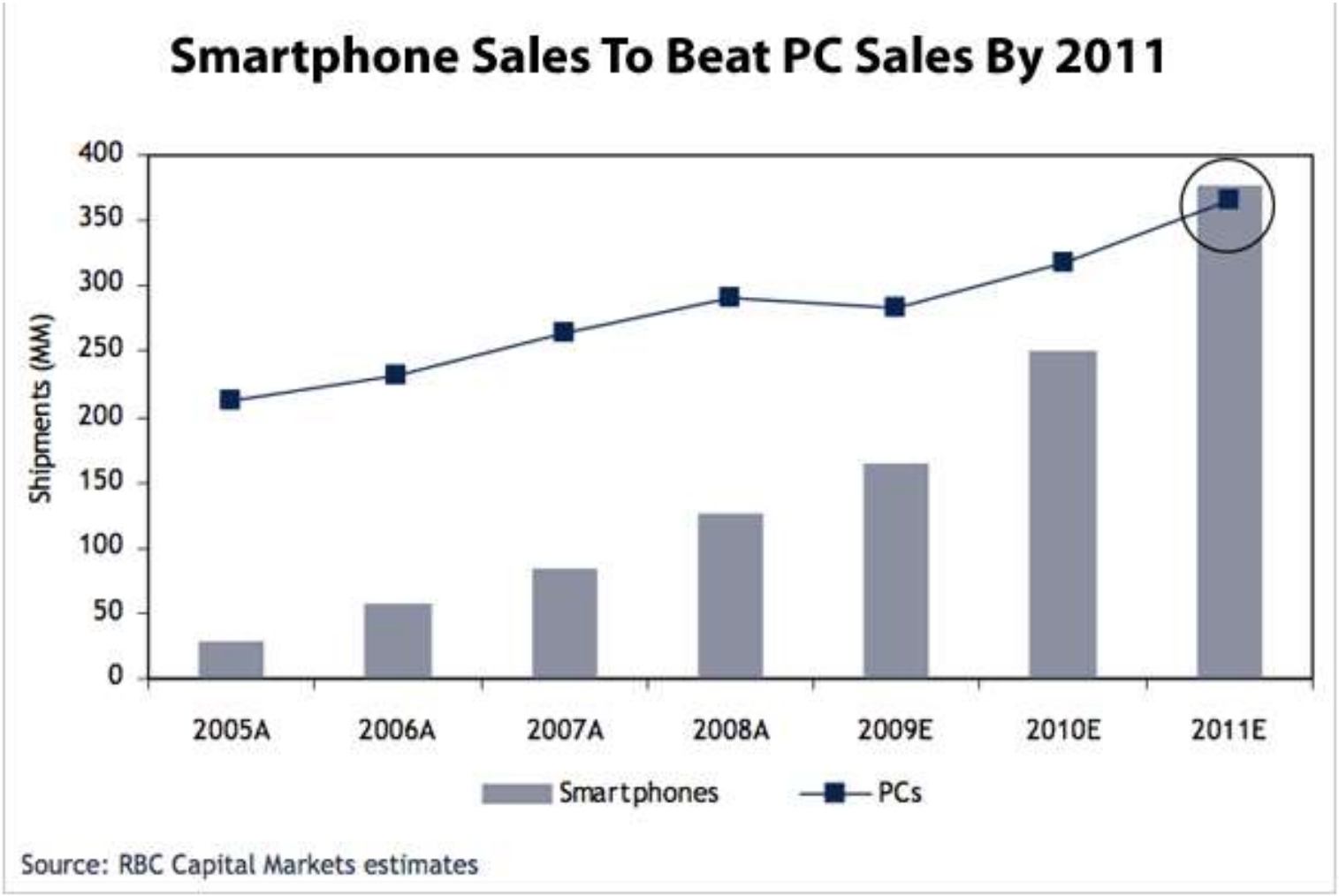
Diversification of the mobile market sector about 2005 [3]



The mobile market segment

1.1 The rapidly increasing importance of the mobile market space (5)

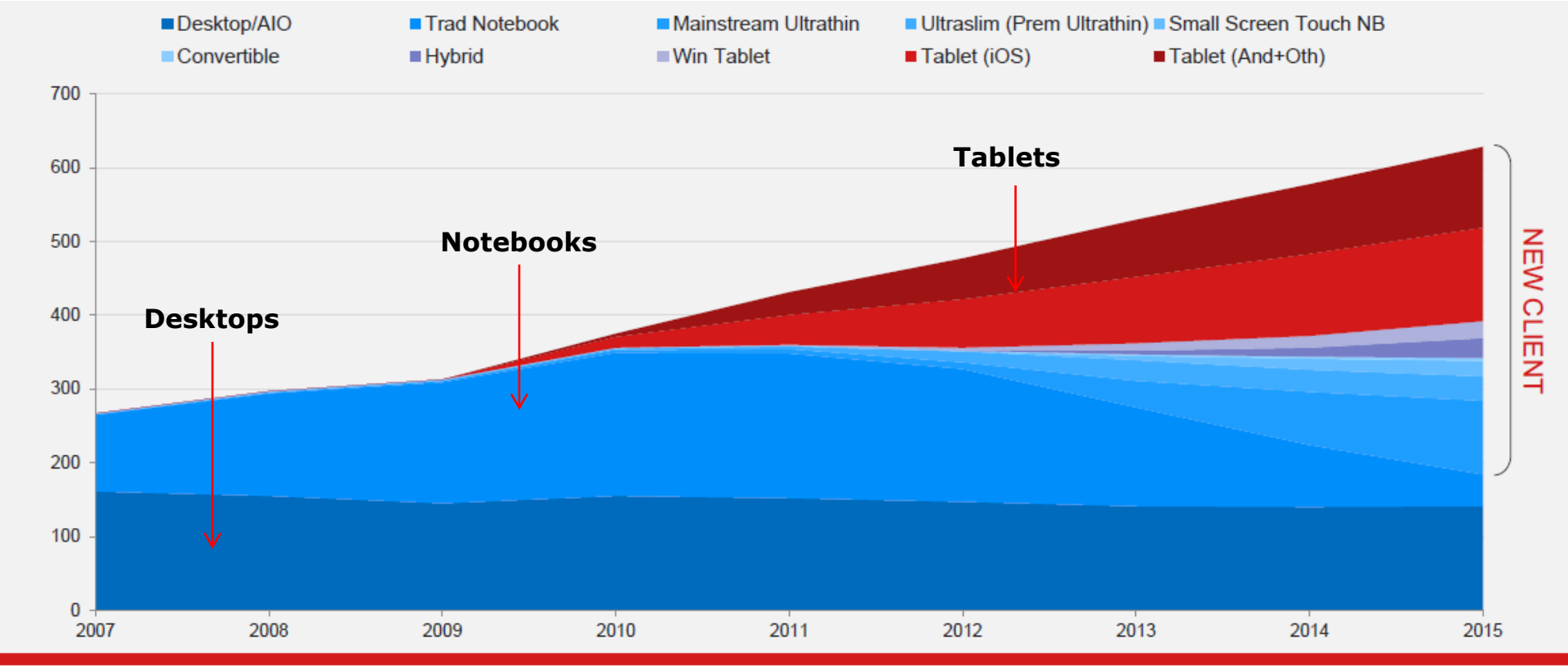
Rapid increase of smartphone sales in the first decade of 2000 [5]



1.1 The rapidly increasing importance of the mobile market space (6)

Rapid increase of tablet sales in the first half of the 2010 decade [4]

Besides smartphones, touchscreen tablets and all their alternative designs that provide also keyboard/mouse input (such as convertibles and hybrids) have recently the highest growth potential, as indicated e.g. in an AMD sales forecast from 12/1012 [4].



Sources: IDC AMD Extended Forecast Client World Wide by Country March 2013, IDC AMD Extended Forecast Tablet December 2012

Figure: Yearly worldwide sales figures of desktops, notebooks and tablets [4]

1.1 The rapidly increasing importance of the mobile market space (7)

Intel's and AMD's attitude to the changing market situation

- Low growth rates of desktops and also of traditional notebooks noticed in the middle of the 2000's forced both Intel and AMD to focus on the emerging mobile market sector that promised a high market potential with devices, such as netbooks, tablets, convertibles and smartphones.
- The new mobile sector was however dominated by low power 32-bit ARM-based processors.
- Concerning this point, both Intel and AMD felt that their performance/power oriented 4-wide 64-bit x86 CISC processors are not competitive with ARM's low power oriented 32-bit RISC processors.

Thus both Intel and AMD diversified their processor portfolio and started to design low power oriented two wide processor lines, as discussed in the Sections 1.3 and 1.4.

1.2 Related terminology

1.2 Related terminology

Intel's Atom-based product series and their designations

A t o m b a s e d p r o d u c t s e r i e s

Entry-level desktops	Notebooks (Subnotebooks)	Convertibles	Tablets	Smartphones	Embedded	Microservers
D/J-Series *(First D, then J)*	***N-Series***		***Z-Series*** *Zx6xx/x7xx*	***Z-Series*** *Zx4xx/x5xx*	***E/CE-Series***	***S-Series***

1.2 Related terminology (2)

Designation of the underlying microarchitecture in Intel's tablet/smartphone processors

Model designation	Underlying microarchitecture
Zxxx	Bonnell
Z2xxx	Saltwell
Z3xxx	Silvermont
Z4xxx	Airmont
Z5xxx	Goldmont

1.2 Related terminology (3)

Device type designations used along with Atom processors and their assignment to the terms used in these slides

Entry-level desktops	Notebooks	Convertibles	Tablets	Smartphones	Embedded
AIOs, All-in-one desktops/PCs, nettops	Sub-notebooks, (A related term Ultrabook designates thin notebooks)		UMPCs MIDs		

Next we give some explanations to the terms written in red.

1.2 Related terminology (4)

The terminology used in connection with Atom-based platforms

There is a couple of new terms used in connection with Atom-based devices that were coined and made use of by a number of manufacturers mainly along with the introduction of mobile devices from the beginning of the 1990's until now, such as

all-in-one PCs, nettops, netbooks, ultrabooks, UMPCs, MIDs, tablets, convertibles, smartphones.

1.2 Related terminology (5)

AIOs/all-in-one desktops/all-in-one PCs

This term was coined already at the end of the 1990's, probably in connection with Apple's Power Macintosh G3 AIO (All-In-One) computer introduced in 1998 [7].

Figure: Apple's Power Macintosh G3 AIO (All-In-One) from 1998 [7]

Apple understood the AIO term as a desktop with integrated display but detached keyboard and mouse.

Recent use of the terms all-in-one desktops/PCs

The term all-in-one desktops/PCs seems now to have a renaissance by Intel used for entry-level desktops with integrated display, as a slide presented in Intel's 2012 investor meeting shows [8].

Figure: Recent ultrabooks and all-in-ones [8]

1.2 Related terminology (7)

Nettops

A term introduced by Intel in 2008 for low cost, thus entry level desktops, as indicated in the next slides.

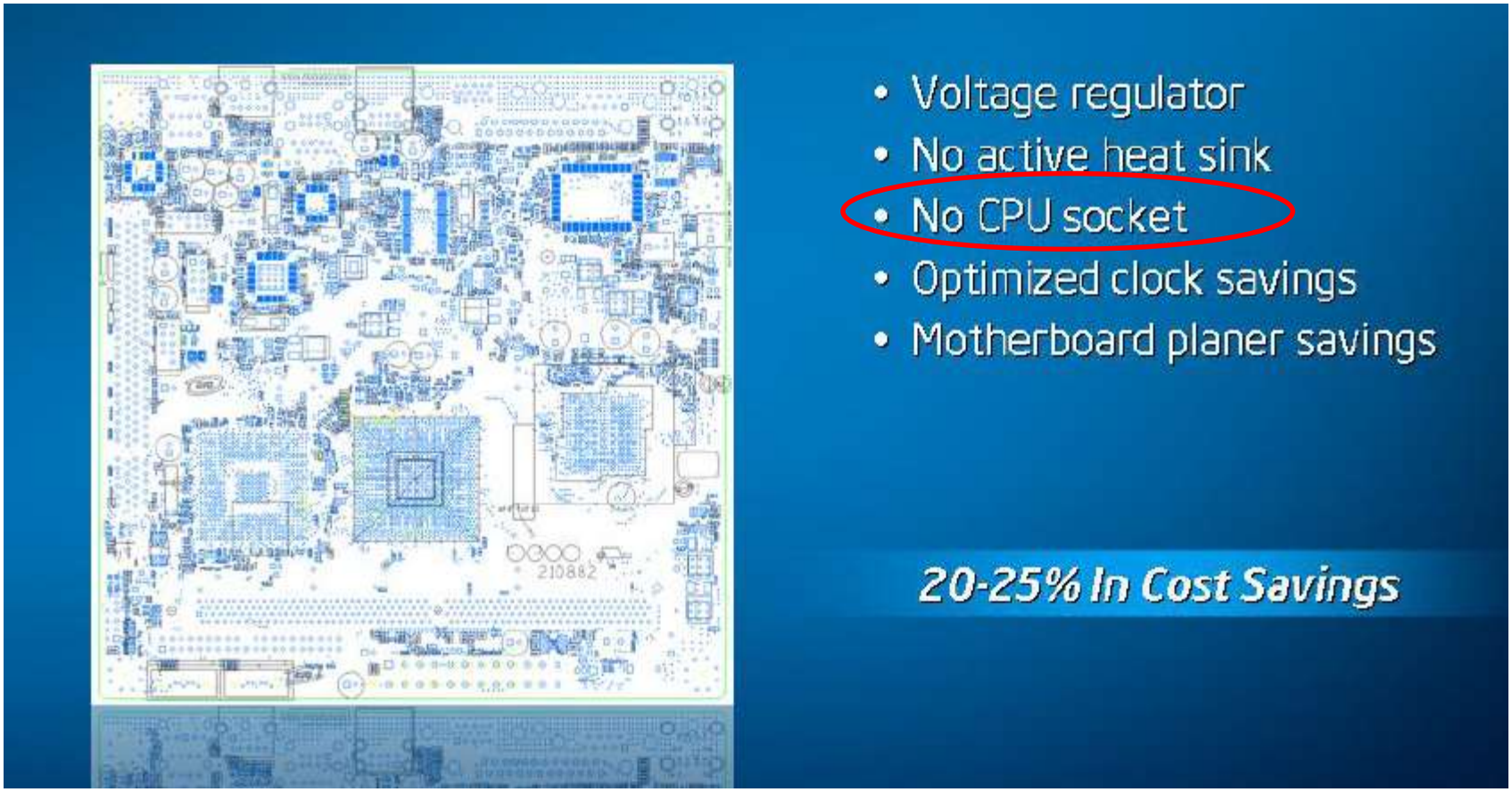
Intel's introductory slide for nettops (and netbooks) at the IDF 4/2008 [9]

Key features of Netbooks and Nettops

- Internet connectivity is a key usage
- Platform is optimized for low BOM cost (Bill Of Material cost)
- Running under Windows and Linux

1.2 Related terminology (9)

Nettop motherboard savings compared to standard desktop cost [9]



Additional nettop BOM savings [9]

PSU: Power Supply Unit

Netbooks

This term was conceived by Intel and introduced in their 2008 IDF /4/2008) to designate small notebooks with a screen size of < 10 " [9], as indicated below.

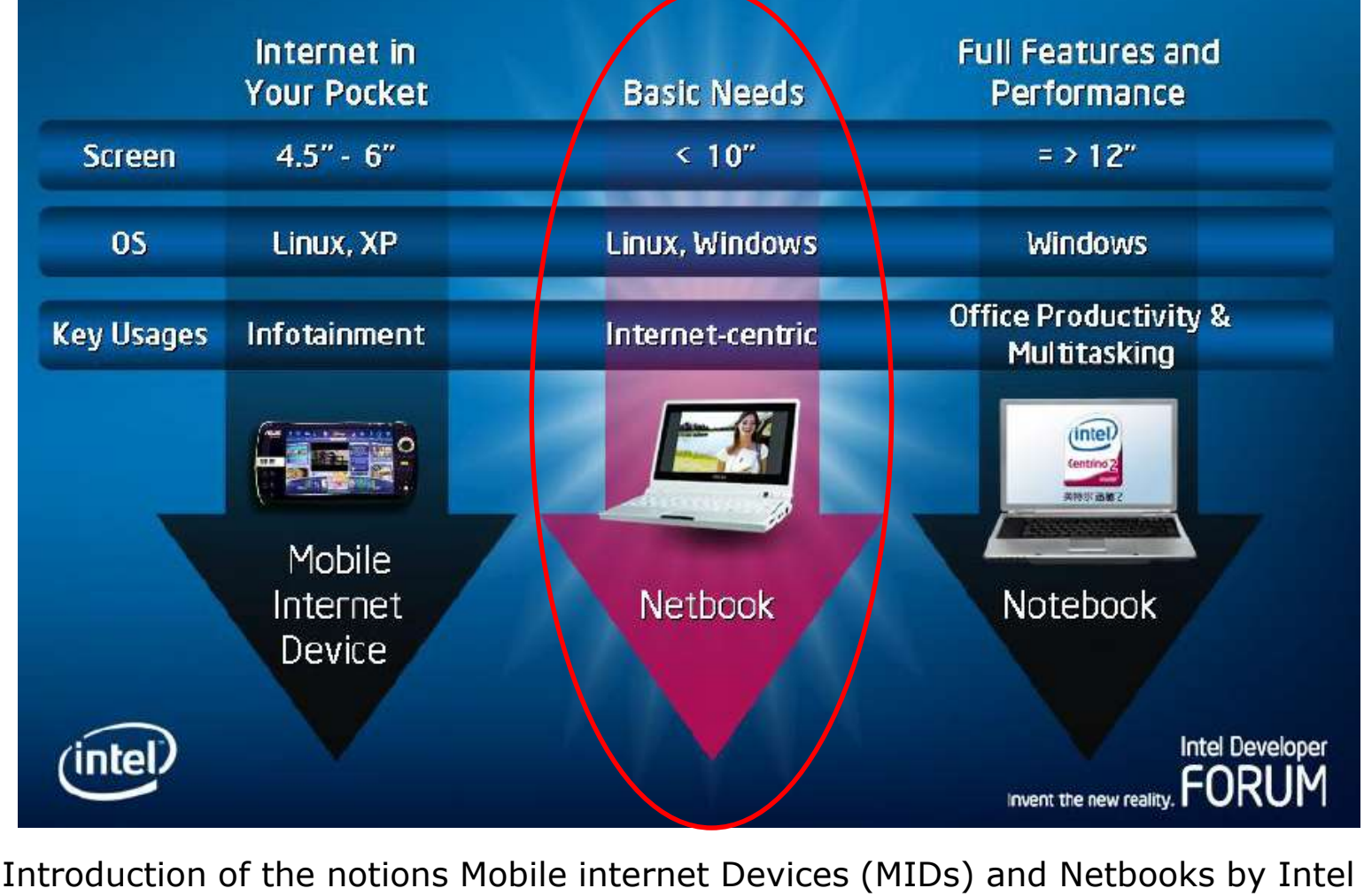


Figure: Introduction of the notions Mobile internet Devices (MIDs) and Netbooks by Intel (2008) [9]

1.2 Related terminology (12)

Subnotebooks

This is a term introduced in the 1990's, presumable along with the Toshiba T3400 Series small sized notebook having a 7.8 " screen, designated as "the first subnotebook computer with the functionality of a much larger computer" [10], shown below.

Figure: The first subnotebook (Toshiba T3400) (1993)

Recent interpretation of the term subnotebook

Recent subnotebooks are interpreted usually as small notebooks having a display size of 7 - 10 " and weighting about 1 kg [11], as indicated in the next Figure.

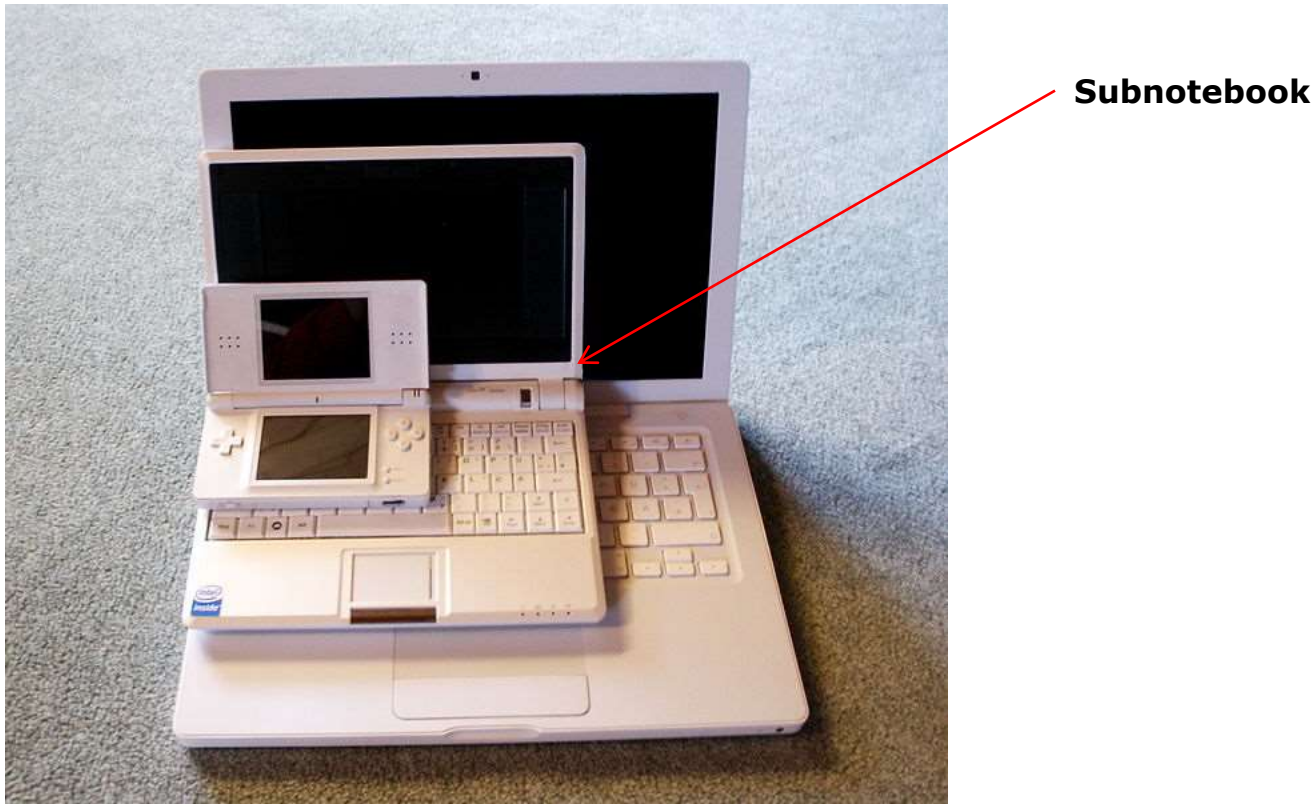


Figure: Contrasting traditional notebooks, subnotebooks and handheld notebooks [12]

Ultrabooks

Intel introduced this term at the Computex 2011 (5/2011) for ultra thin notebooks any kind, as indicated in the next Figures [8].

Figure: Recent ultrabooks and all-in-ones [8]

1.2 Related terminology (15)

Intel's example of an "ultra thin notebooks" i.e. "ultrabooks" [8]

Traditional notebooks vs. ultrabooks in Intel's interpretations [8]

Market positioning of Ultrabooks by Intel [8]

Convertibles

Convertibles may be used both as touch screen tablets and regular laptops with a keyboard.

There are different implementations of convertibles, as shown below [13].

Implementation alternatives of convertibles-1 [13]

Main types of convertibles

Convertible notebook

Regular laptops with a screen that can be swiveled around to turn the display into a tablet. This will be achieved by rotating the screen around and slipping it over the keyboard which is hidden in tablet mode.

Sliders

These convertibles have the display slide toward the user to form a tablet. The display covers (hides) the keyboard for use as a tablet.

Hybrids

These are two separate parts, a tablet (screen) and a keyboard (dock) that can be used together like a laptop. E.g. the tablet snaps onto a keyboard dock to form a single laptop device.

Implementation alternatives of convertibles-2 [35]

A wide range of convertibles

UMPC (Ultra Mobile PC)

This term was introduced by Microsoft in 3/2006 (originally named as the Origami project).

Microsoft designated by UMPC a touch screen tablet PC with a 7 " screen size and a weight of about 1 kg, as shown in the Figure.

Microsoft's tablet run under Microsoft Windows XP TabletPC Edition [147].

Figure: An UMPC, practically a touch screen tablet, as introduced by Microsoft in 2006 [147]

Mobile Internet Devices (MIDs)

This term was also coined and introduced in their 2008 IDF /4/2008) for touch scree tablets with a screen size of 4.5 – 6 " [9], as indicated below.

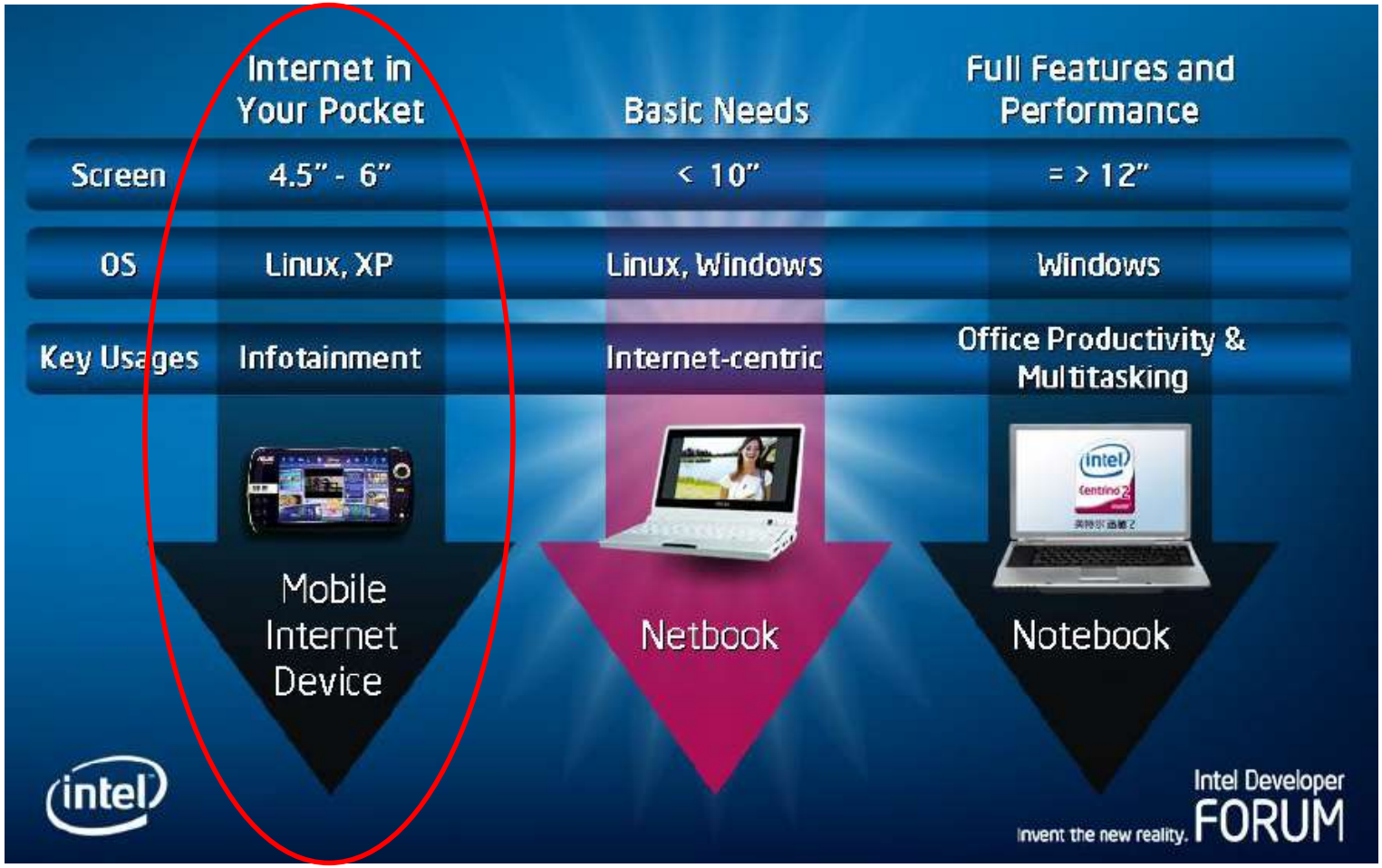


Figure: Introduction of the notions Mobile internet Devices (MIDs) and Netbooks by Intel (2008) [9]

1.3 Introduction to Intel’s low-power Atom series

1.3 Introduction to Intel's low power Atom series -1

Before 2008 Intel covered all high volume market segments by the same design, as indicated below [14].

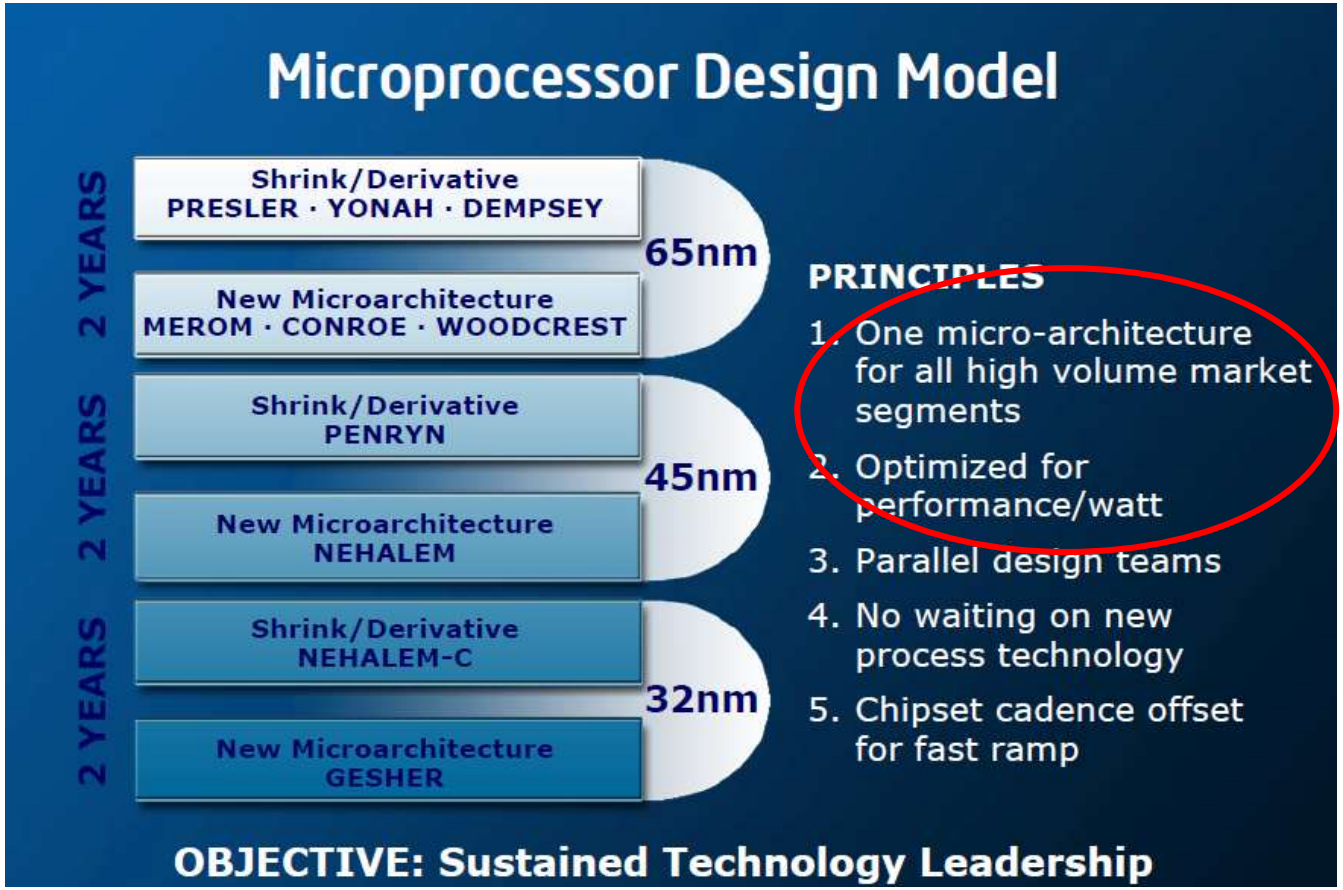


Figure: Intel's design principles for developing microprocessors, as revealed at their shareholder's meeting in 4/2006 [14]

1.3 Introduction of the low-power oriented Atom series by Intel (2)

Introduction to Intel's low power Atom series -2

Intel recognized quite early the immense importance of the emerging mobile computer segment, as indicated in the following part of a speech of Sean Maloney, Intel's general manager for the Mobility Group, held at the 2006 Intel Developer Forum already in 3/2006 [15]:

> So there is a huge effort underway to shrink down that PC architecture and put it into a smaller and smaller space. That initiative is called the Ultra Mobile PC – that's the most common name for it. Here's an example of one of those devices. You're going to see a tremendous wave of experimentation, in the next year-and-a-half or two years, taking a lesson from the cell phone industry, with new types of form factors, keyboards that swivel out, keyboards that clamshell open, all kinds of different form factors and sizes, as the PC industry races to get this flexible architecture into a smaller and smaller space. You won't have to wait long at all for the announcements of the first ones of those devices.

1.3 Introduction of the low-power oriented Atom series by Intel (3)

Introduction to Intel's low power Atom series -3

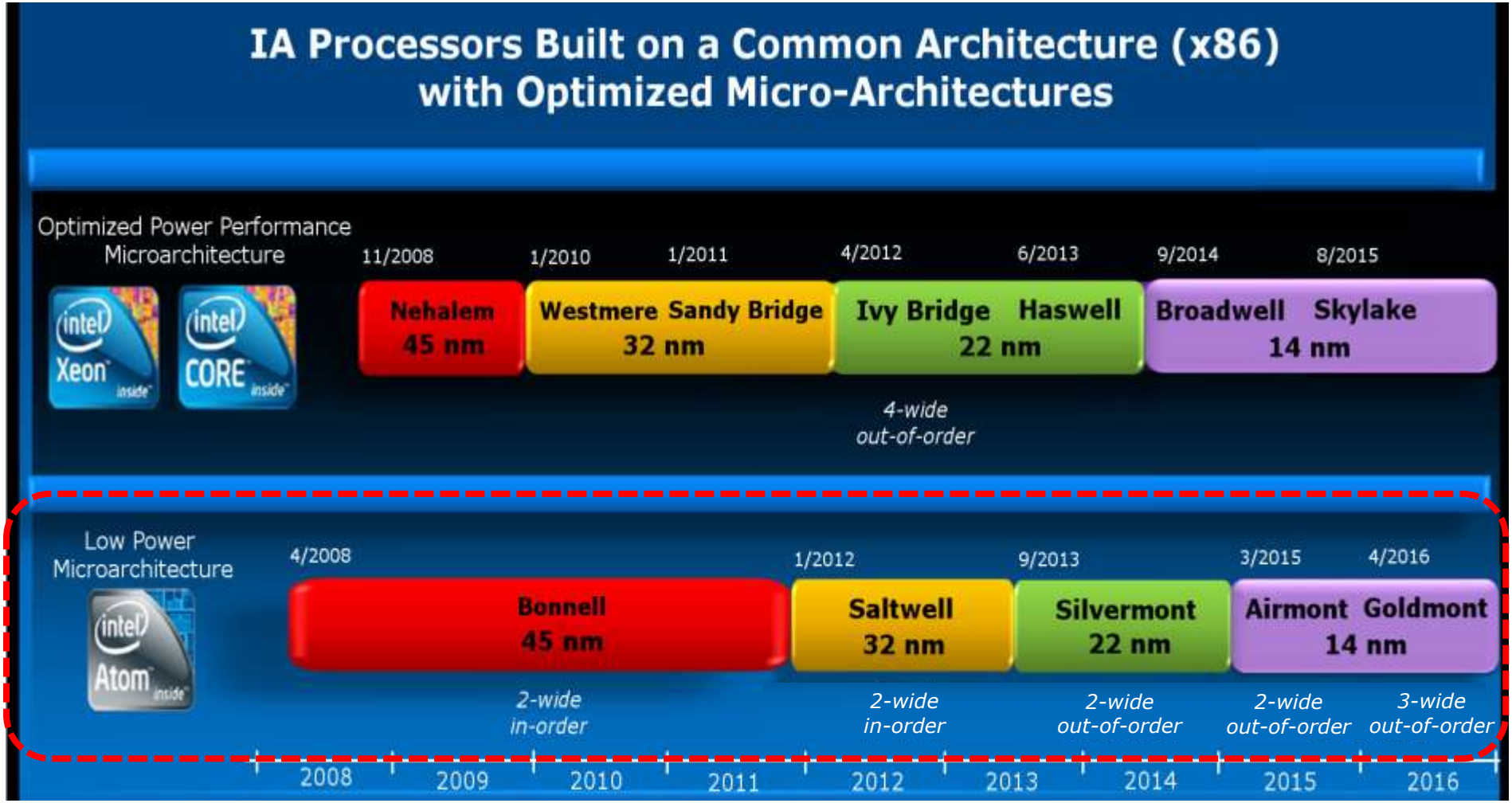
In fact, about two years later Intel introduced first the Atom brand in 3/2008 and then in 4/2008 their low-power oriented two-wide Atom line of processors as an alternative design approach to their four-wide performance/power oriented Core 2 processor lines.

From now on Intel supported three major processor designs

- the high reliability and high performance IA64 Itanium lines,
- the power/performance oriented 4-wide x86 Core2 lines and
- the low-power oriented 2-wide x86 Atom lines.

1.3 Introduction of the low-power oriented Atom series by Intel (4)

Evolution of Intel's basic architectures (based on [3])



1.3 Introduction of the low-power oriented Atom series by Intel (5)

Introduction of low power oriented Atom-based devices

Low power, Atom-based devices were introduced from Intel in three steps, as follows:

a) At the IDF Spring in 4/2008: - entry level desktops (called nettops) and
- netbooks (small notebooks, practically notebooks with 10 " or smaller seen size [9].

Netbook

Nettop

Source: Gartner, Global PC Forecast and Shipments Quarterly Statistics: Database, February 2008 Update

1.3 Introduction of the low-power oriented Atom series by Intel (6)

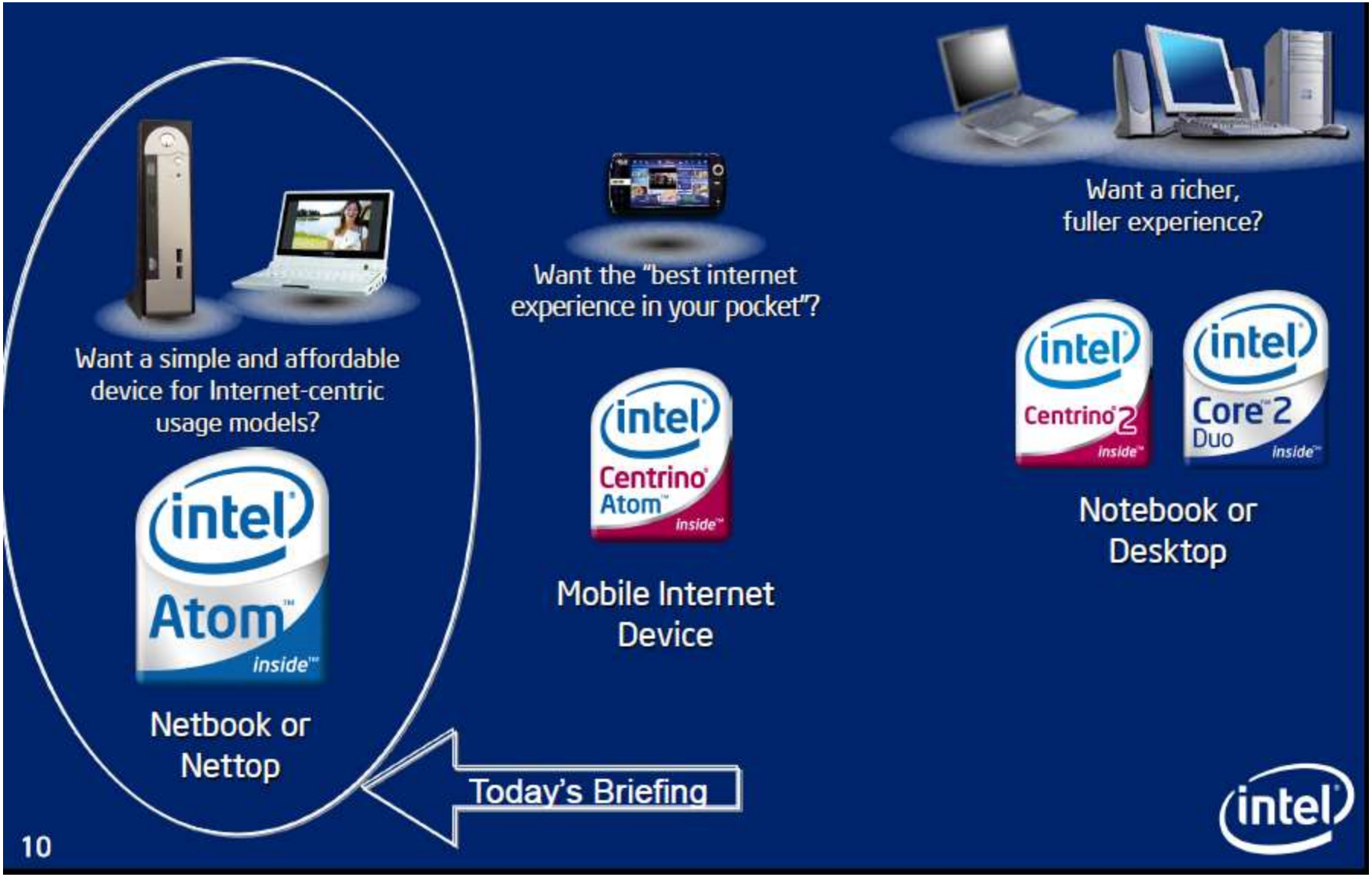
b) At the IDF Fall in 8/2008: Tablets (called MIDs) [17]

MIDs: Mobile internet Devices, in Intel's 2008 understanding, practically all kinds of tablets.

1.3 Introduction of the low-power oriented Atom series by Intel (7)

c) At the IDF Fall in 9/2009: Smartphones (actually high-end smartphones) [18]

Intel's 2008 concept for using the Atom line [19]



1.3 Introduction of the low-power oriented Atom series by Intel (9)

Intel's 2011 concept to cover the continuum of compute devices [3]

1.3 Introduction of the low-power oriented Atom series by Intel (10)

Introduction of microservers

After 2011 in 4/2012 Intel announced and launched (12/2012) also Atom-based low-power oriented microservers (termed as the S1200 (Centerton) line).

1.3 Introduction of the low-power oriented Atom series by Intel (11)

Presentation of Intel's Atom-based product series in these slides

A t o m b a s e d p r o d u c t s e r i e s

Entry-level desktops	Notebooks (Subnotebooks)	Convertibles	Tablets	Smartphones	Embedded	Microservers
D/J-Series *(First D, then J)*	***N-Series***		***Z-Series*** *Zx6xx/x7xx*	***Z-Series*** *Zx4xx/x5xx*	***E/CE-Series***	***S-Series***
Section 3	*Section 3*		*Section 4*	*Section 5*	*Not discussed*	*Not discussed*

1.3 Introduction of the low-power oriented Atom series by Intel (12)

Main competitors to Intel's Atom-based products (not considered microservers)

Desktops | **Laptops** | **Entry-level desktops** | **Notebooks (Subnotebooks)** | **Convertibles** | **Tablets** | **Smartphones** | **Embedded**

i3-i7 Series | ***D/J-Series*** *(First D, then J)* | ***N-Series*** | ***Z-Series*** *Zx6xx/x7xx* | ***Z-Series*** *Zx4xx/x5xx* | ***E/CE-Series***

x86 | ***Atom*** | ***processors***

A M D

A large number of vendors using ARM-ISA based ARM, Apple, Qualcomm or Samsung designed processors

NVIDIA, Freescale

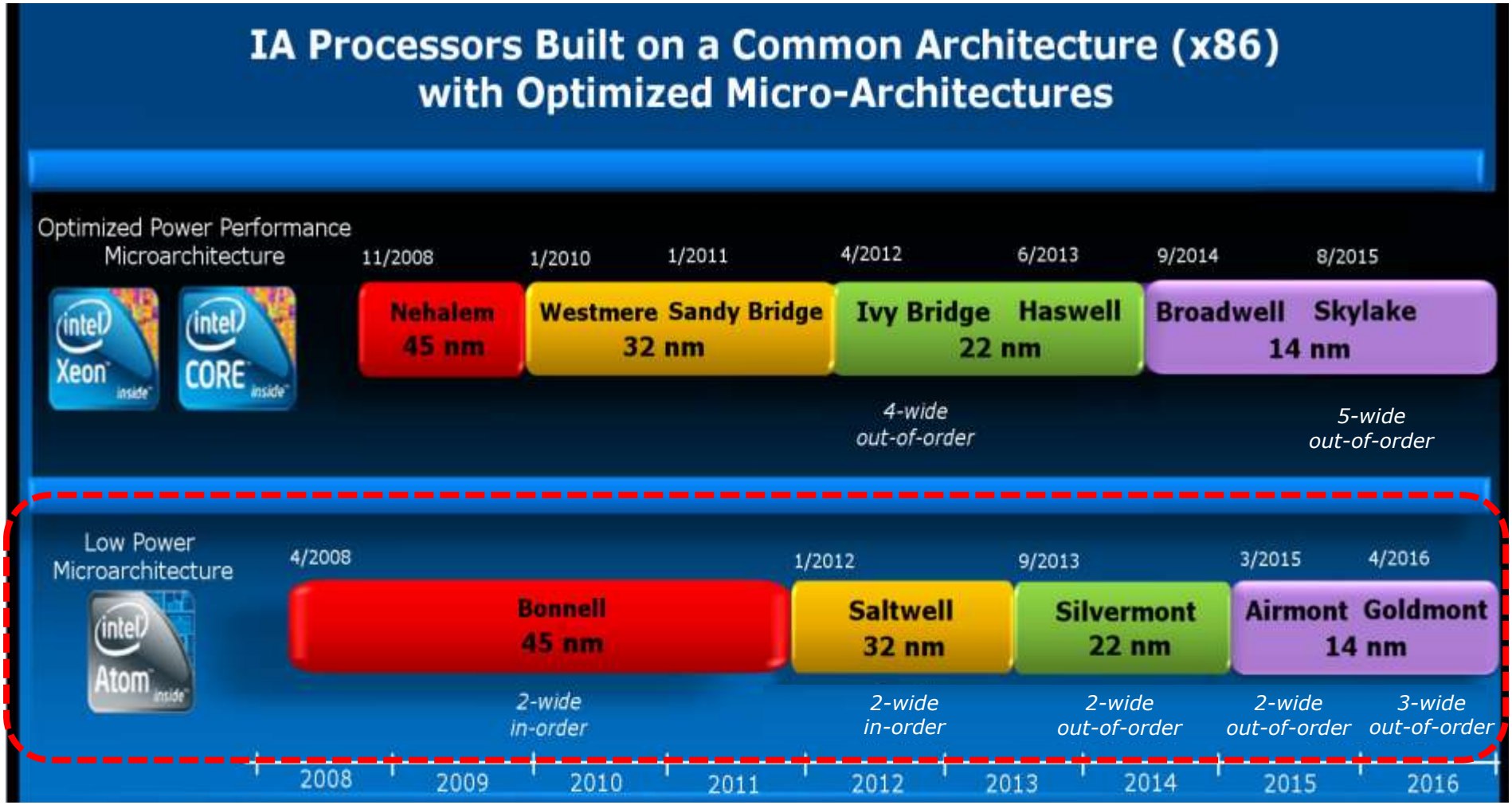
2. Intel’s low-power oriented CPU microarchitectures

- 2.1 Introduction
- 2.2 The 45 nm Bonnell CPU
- 2.3 The 32 nm Saltwell CPU
- 2.4 The 22 nm Silvermont CPU
- 2.5 The 14 nm Airmont CPU core
- 2.6 The 14 nm Goldmont CPU
- 2.7 The 14 nm Goldmont Plus CPU

2.1 Introduction

2.1 Introduction

Evolution of Intel's basic CPU microarchitectures (based on [3])



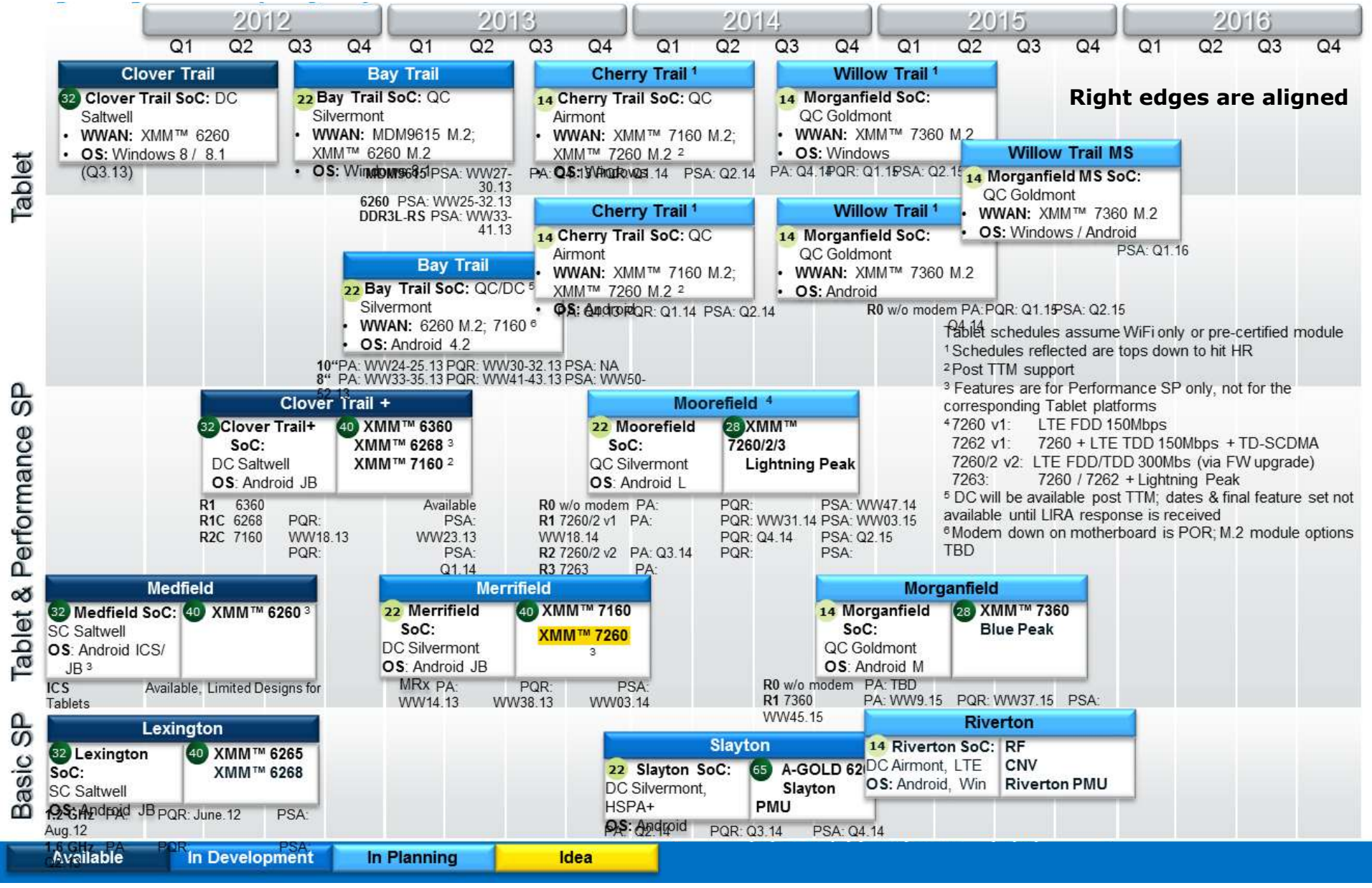
2.1 Introduction (2)

Intel's mobile devices based on their CPU microarchtectures as named in Q2/2013 [145]

Category	Platform	Acronym	Form Factor Reference Design (FFRD)	Atom Processor Name	AP Name (SoC)		AP Core			Clock Freq. (up to)	Node
					Old	New	Core	#C	#T		
High End Tablet	Willow Trail	WLT	Willow Trail FFRD	Z5series	Willowview	Willow Trail SoC	Goldmont	4	4		14 nm
	Cherry Trail	CHT	Cherry Trail FFRD	Z4series	Cherryview	Cherry Trail SoC	Airmont	4	4	2.7 GHz	14 nm
	Bay Trail	BYT	Bay Trail FFRD	Z37x0 (D)	Valleyview 2	Bay Trail SoC	Silvermont	4	4	2.4&1.8 GHz	22 nm
				Z3680 (D)				2	2	1.8 GHz	
	Clover Trail	CLT	Clover Trail FFRD	Z2760	Cloverview	Clover Trail SoC	Saltwell	2	4	1.8 GHz	32 nm
Android Tablet / Performance Smartphone	Morganfield	MGF	Morganfield tablet/ phone FFRD	Z5series	Broxton	Morganfield SoC	Goldmont	4	4	2.7 GHz	14 nm
	Moorefield	MOF	Moorefield tablet/ phone FFRD	Z3series	Anniedale	Moorefield SoC	Silvermont	4	4	2.3&1.8 GHz	22 nm
	Merrifield	MEF	Merrifield tablet/ phone FFRD	Z34x0	Tangier	Merrifield SoC	Silvermont	2	2	2.1&1.6 GHz	22 nm
	Clover Trail+	CTP	Clover Trail+ tablet/ phone FFRD	Z25x0	Cloverview+	Clover Trail+ SoC	Saltwell	2	4	2 & 1.6 & 1.2 GHz	32 nm
	Medfield	MDF	Medfield tablet/ phone FFRD	Z24x0	Penwell	Medfield SoC	Saltwell	1	2	2&1.6 GHz	32 nm
Android Tablet / Entry Smartphone	Binghamton	BHM	Binghamton tablet/ phone FFRD	Z4series	n.a.	Binghamton SoC	Airmont	2	2	1.2 GHz	14 nm
	Riverton	RVN	Riverton tablet/ phone FFRD	Z3series	n.a.	Riverton SoC	Airmont	2	2	1.6 GHz	14 nm
	Slayton	SLN	Slayton tablet/ phone FFRD	Z3series	n.a.	Slayton SoC	Silvermont	2	2	1.2 GHz	22 nm

No more external usage

Intel's internal smartphone (SP) and tablet roadmap from Q2/2013 [145]



2.2 The 45 nm Bonnell CPU

2.2 The 45 nm Bonnell CPU

Developed at Intel's Austin Design Center by the team that was working on the Tejas core, which was Intel's next Pentium 4 core following the Prescott core, but became canceled due to too high dissipation.

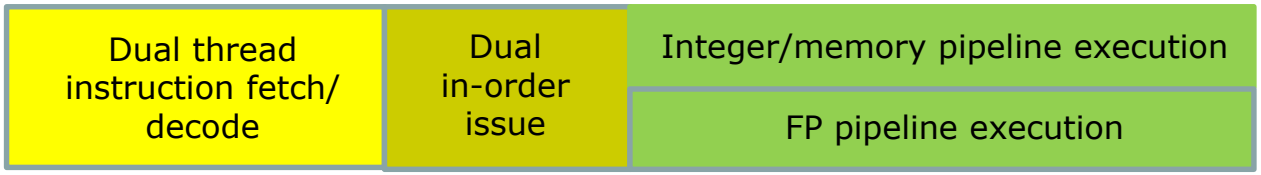
Key features of the microarchitecture of the Bonnell CPU

- The Bonnell CPU supports the 32/64-bit x86 ISA.
- It underlies Intel's first generation Atom processors, such as the Silverthorne or Lincroft processors of the Menlow, Oak Trail or Moorestown platforms targeting tablets and smartphones.
- Introduced in 4/2008 as part of the Silverthorne processor of the Menlow platform.
- It was manufactured using a 45 nm process.
- The Bonnell CPU has a two-wide, in-order supperscalar microarchitecture.
- It supports hypertreading such that the scheduler can issue up to dual microinstructions from each thread or a single instruction from each thread in an in-order manner, as indicated in the next Figure.

2.2 The microarchitecture of the 45 nm Bonnell CPU (2)

Simplified principle of operation of the Bonnell microarchitecture

Dual threaded, dual, in-order issue microarchitecture to dual pipelines



16-stage integer pipeline (all stages)

The scheduler can issue up to two microinstructions from either thread per clock to either pipeline with given instruction pairing restrictions arising from the available execution resources. in an in-order manner.

Note

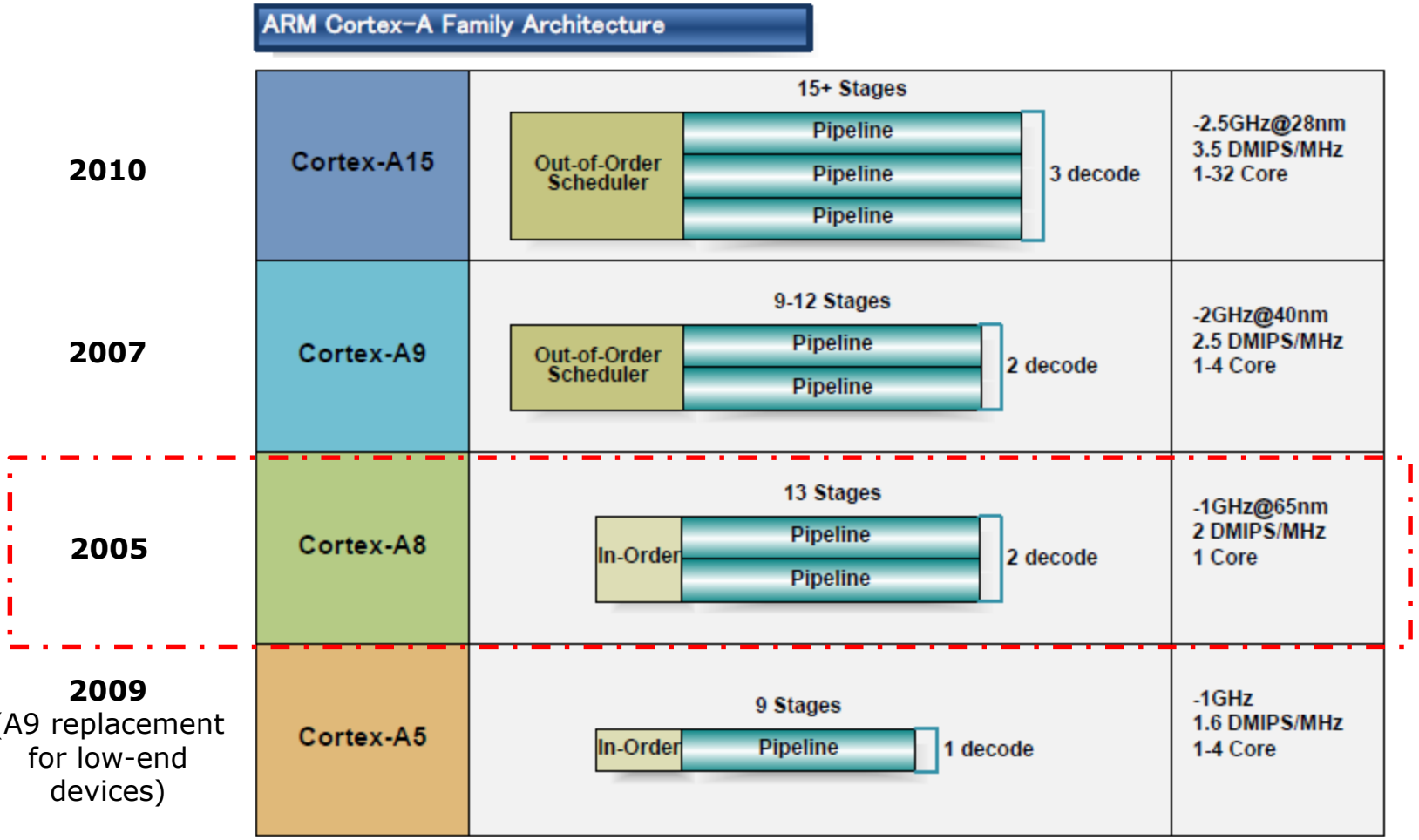
Despite performance degradation Intel has chosen an in-order issue scheme and a two-wide microarchitecture to drastically reduce power consumption.

By contrast, Intel's performance/power optimized processors are out-of-order superscalars (from the Pentium II on (1996)) and are 4-wide (from the Core 2 on (2006).

On the other hand, the Bonnell microarchitecture is hyperthreaded, this features provides typically 36 % increase in performance for 19 % cost in power [44].

2.2 The microarchitecture of the 45 nm Bonnell CPU (3)

Comparing the principle of operation of Intel's Bonnell microarchitecture with the that of ARM's Cortex line of processors [45]



The number of pipeline stages relates to the integer/memory pipeline

2.2 The microarchitecture of the 45 nm Bonnell CPU (4)

Remark

DMIPS/MHz in the previous Figure means DMIPS (Dhrystone MIPS) per MHz, i.e. a score that reflects the efficiency of the microarchitecture.

DMIPS on the other hand is a Drystone benchmark that is obtained when the synthetic Drystone result is divided by 1757 (the number of Drystones per second obtained on the VAX 11/780 machine, nominally a 1 MIPS machine [46].

2.2 The microarchitecture of the 45 nm Bonnell CPU (5)

Block diagram of the Bonnell CPU core [47]

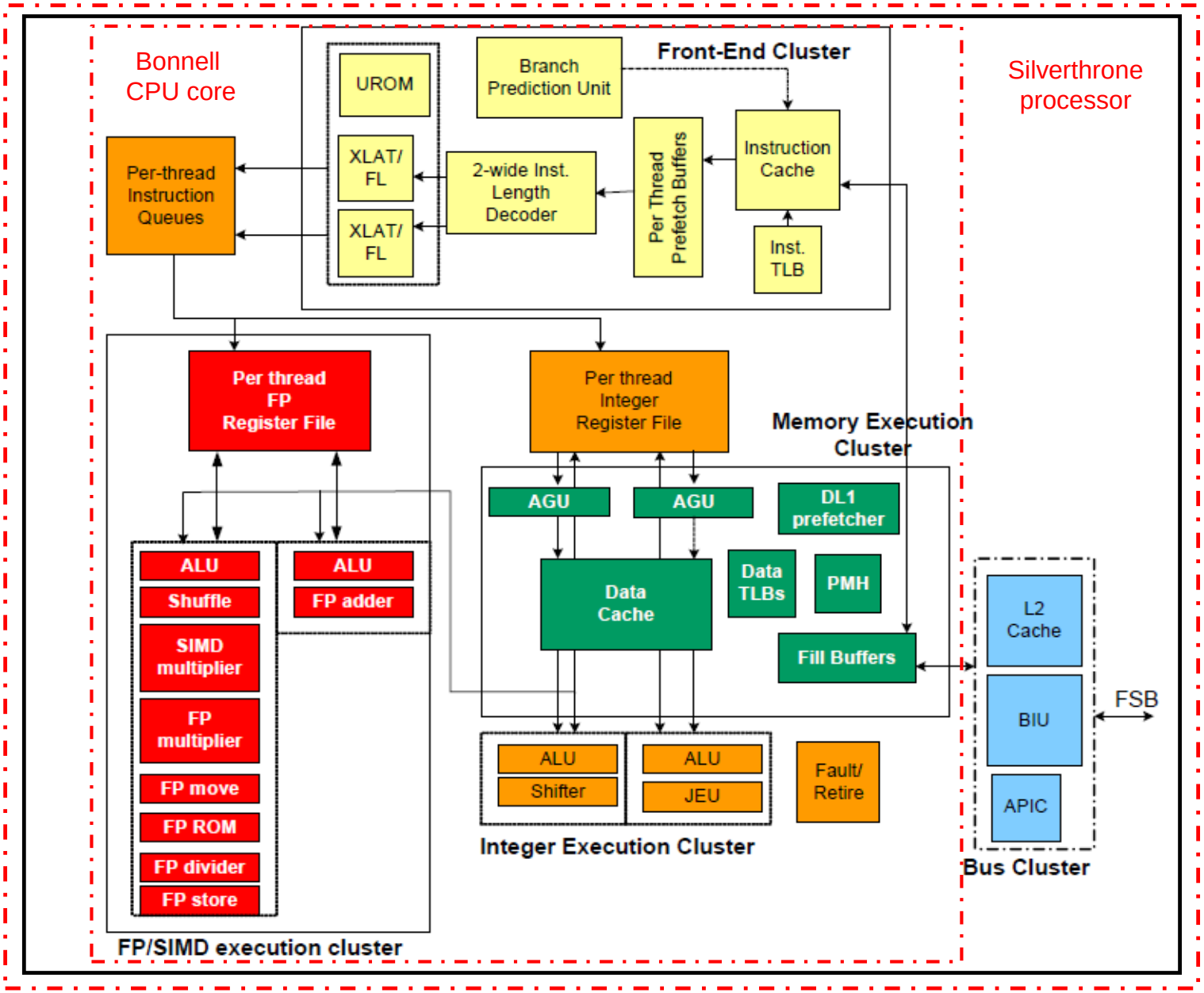
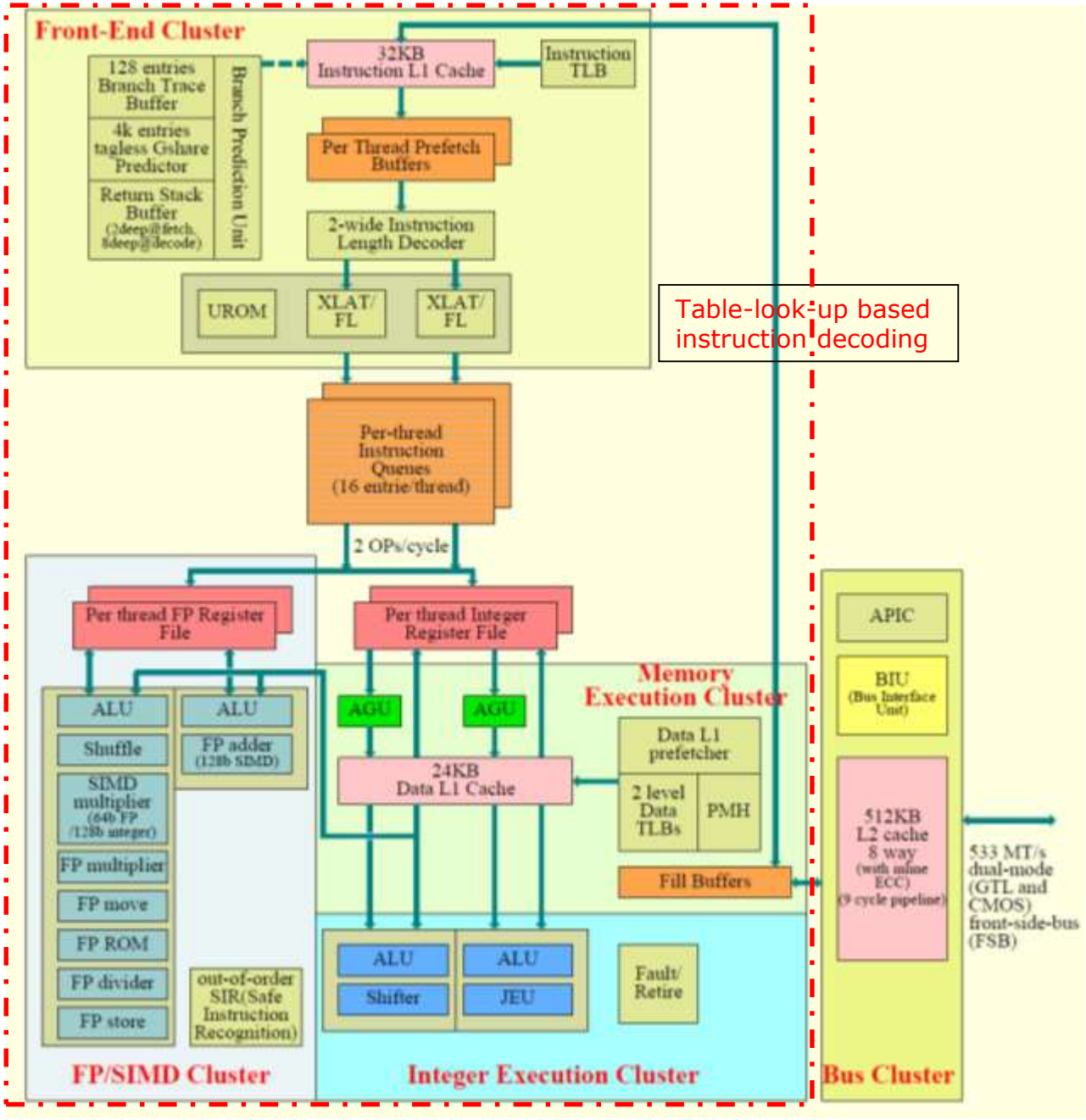


Figure: Block diagram of the Bonnell CPU core

2.2 The microarchitecture of the 45 nm Bonnell CPU (6)

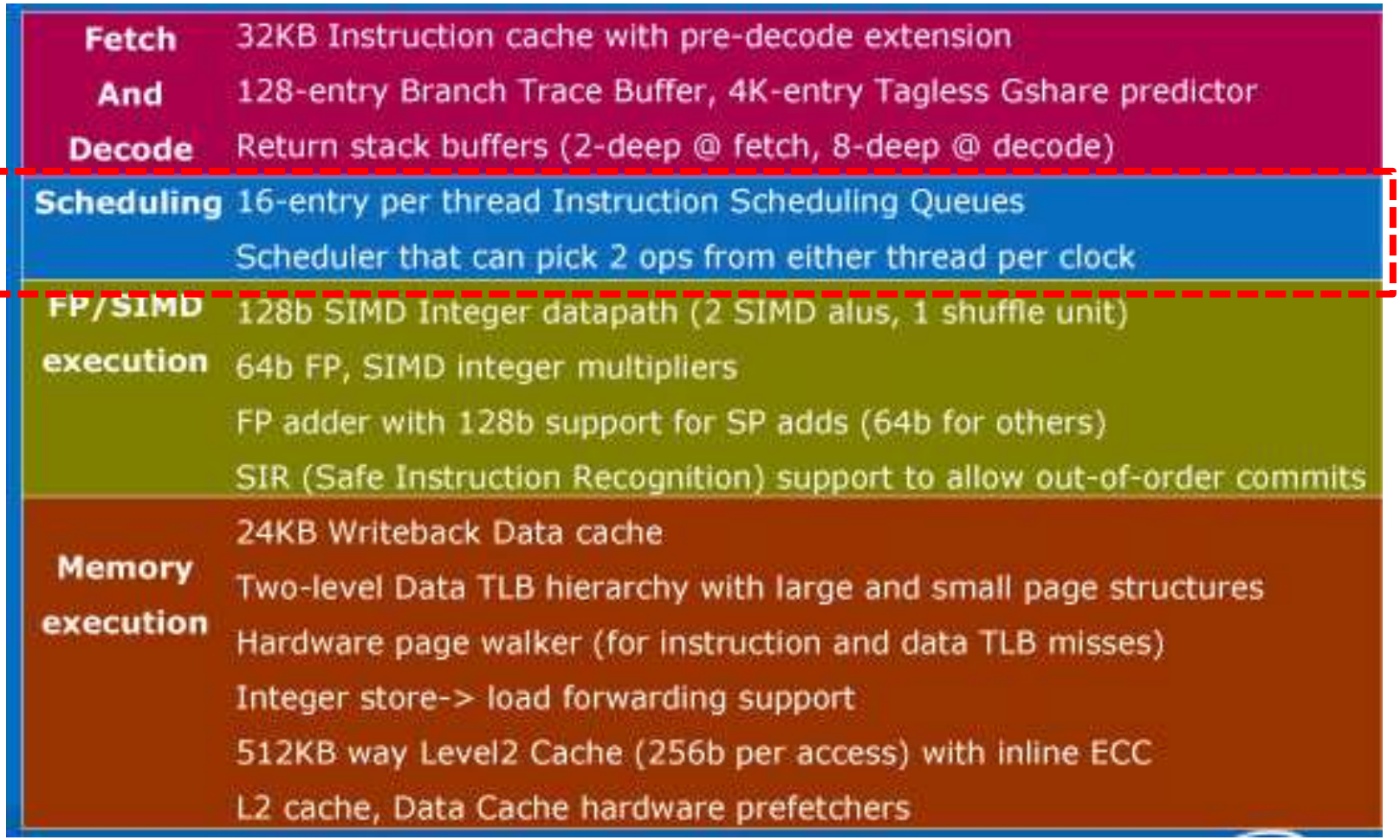
A more detailed block diagram of the Bonnell CPU [48]

Dual in-order issue



2.2 The microarchitecture of the 45 nm Bonnell CPU (7)

Features of the microarchitecture of the Bonnell CPU [49]



2.2 The microarchitecture of the 45 nm Bonnell CPU (8)

Remark

Safe Instruction Recognition (SIR)

This is feature of an in-order microarchitecture that allows to relief in part the restrictions of the in-order issue.

SIR was introduced already in the Pentium processor (1993) that is also an in-order two-wide superscalar.

SIR is basically an early check for possible FP exceptions, such as overflow or underflow.

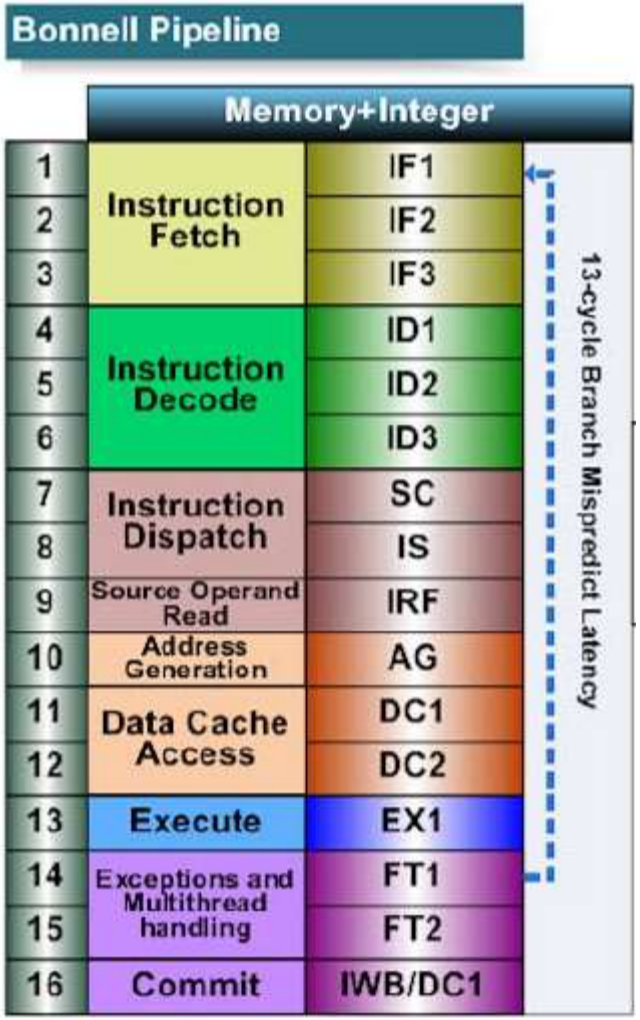
If the instruction execution is “safe” a subsequent instruction can commit (write the result into the register file or memory) out-of-order and can leave the instruction slot for another instruction.

If the inspected instruction is not “safe”, the subsequent instruction will be committed in-order, i.e. along with or after the previous instruction.

Actually, SIR is based on a patent filed during the design of the Pentium processor [50].

2.2 The microarchitecture of the 45 nm Bonnell CPU (9)

The memory and integer pipeline of the Bonnell CPU [51]



16-stage memory/integer pipeline

2.2 The microarchitecture of the 45 nm Bonnell CPU (10)

The range of power management techniques used in the Bonnell CPU [52]

- Deep power down (C-6) architecture
- Non-grid clock distribution
- Optimized register-file and cache 6T bit-cells for lowest power-supply operation
- Pervasive clock gating, word-line driver gating, floating bitlines and programmable L2 array retention supply
- CMOS mode on quad-pumped FSB IO
- Split IO power supply to further reduce IDLE leakage power
- Throttling when processor is overheating
  - Hardware Auto-throttle mechanisms based on internal Thermal Sensor (Thermal Monitoring 1 and 2 supported)
  - ACPI Software controlled thermal management through OS/User policy based to prevent overheating

2.2 The microarchitecture of the 45 nm Bonnell CPU (11)

The Deep Power Down state (C6 state)

The C6 state was introduced in Intel's Core 2 Penryn processor (2007) to reduce leakage current und thus power consumption.

The Process of entering the C6 Tread state and the C6 Package state [53]

In case of a long time of inactivity the OS lets enter a threads into the Thread C6 state by issuing an appropriate IO instruction (e.g. the MWAIT(C6) instruction.

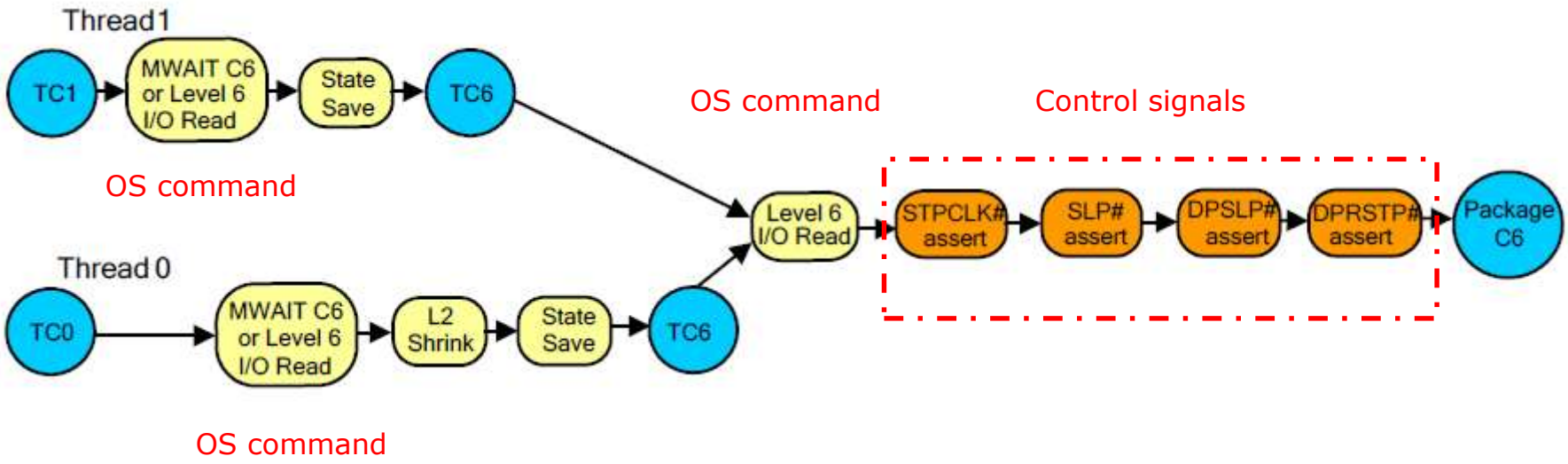
Then the microprogram that controls the execution of the MWAIT instruction lets save the program state of the thread in question into an on-die SRAM of 10 kB that resides on a separate power plane (V_{CCP}).

When also the second thread enters the Thread C6 state, the microprogram lets save the processor state belonging to the second thread as well into the on-die SRAM and also lets flush L2, the processor enters the Package C6 state.

After the processor enters the Package C6 state the core voltage can be lowered to a very low voltage, this allows a significant reduction of the leakage current.

The related process is illustrated in the next Figure.

The sequence of entering the C6 Package state [53]



The exit sequence of the C6 Package state [53]

It is triggered by the chipset when it detect a break event, such as an interrupt.

In this case the microprogram de-asserts the related signals to return to the C0 state (active state) by first letting ramp up the core voltage V_{cc} to the LFM value and starting up its internal PLLs (at the de-assertion of DPSL#), and then restoring the thread states from the on-die SRAM (at the de-assertion of SLP# signal), as indicated below.

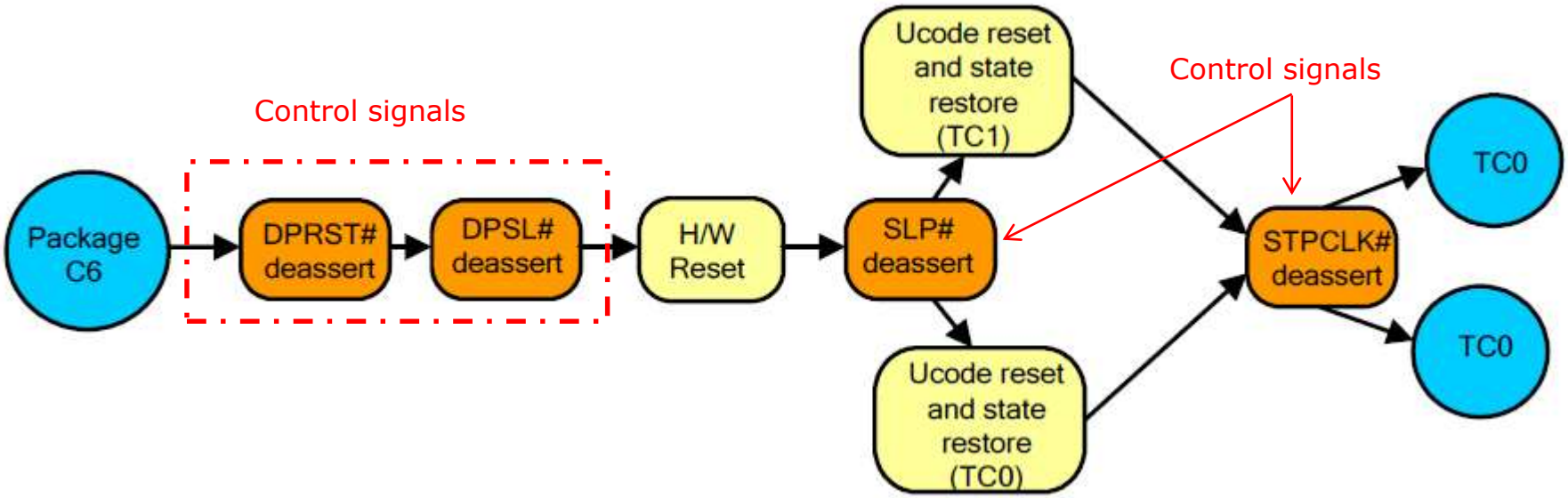
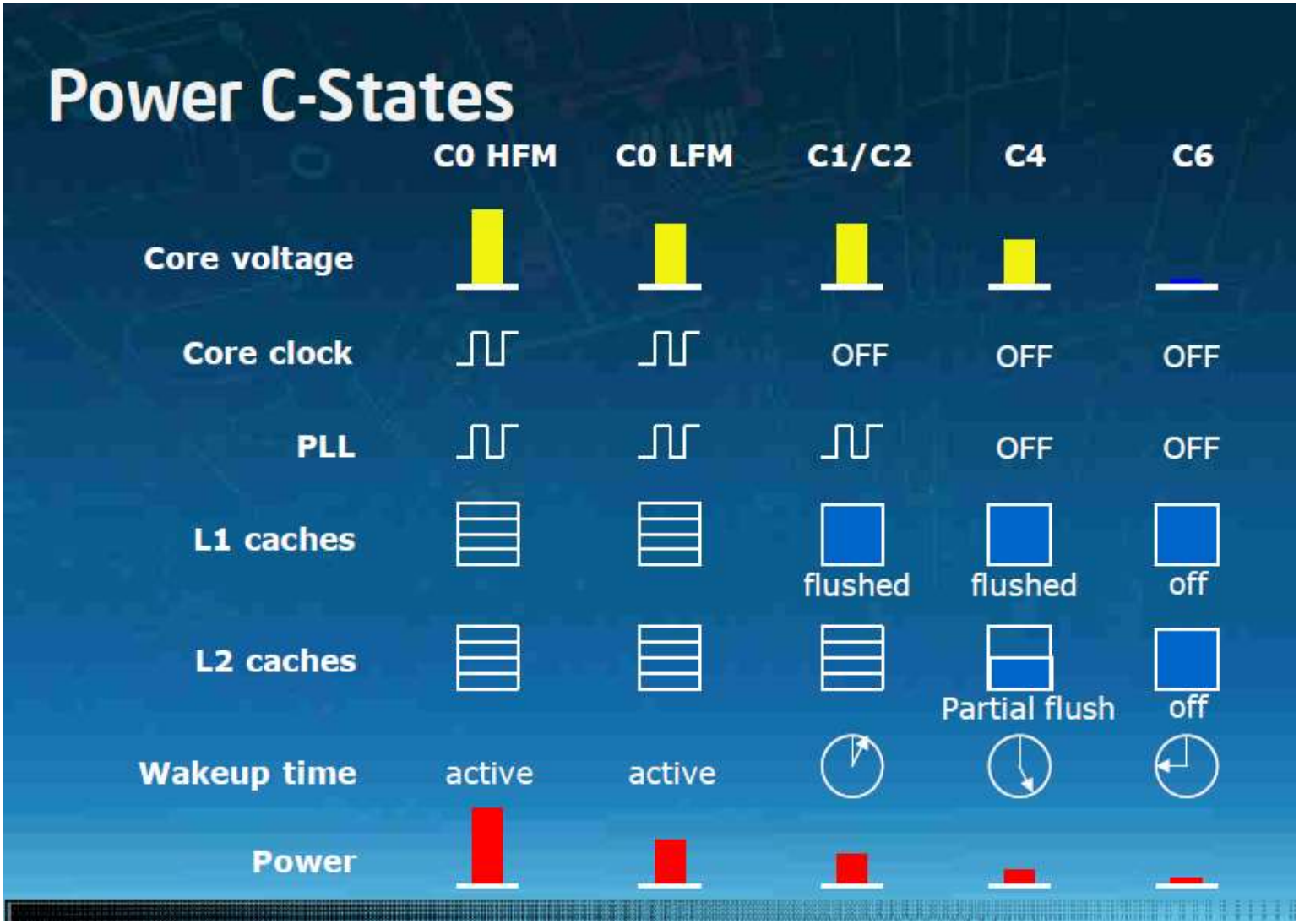


Figure: The exit sequence of the C6 Package state [53]

The Package C6 state as one of the processor C states [52]

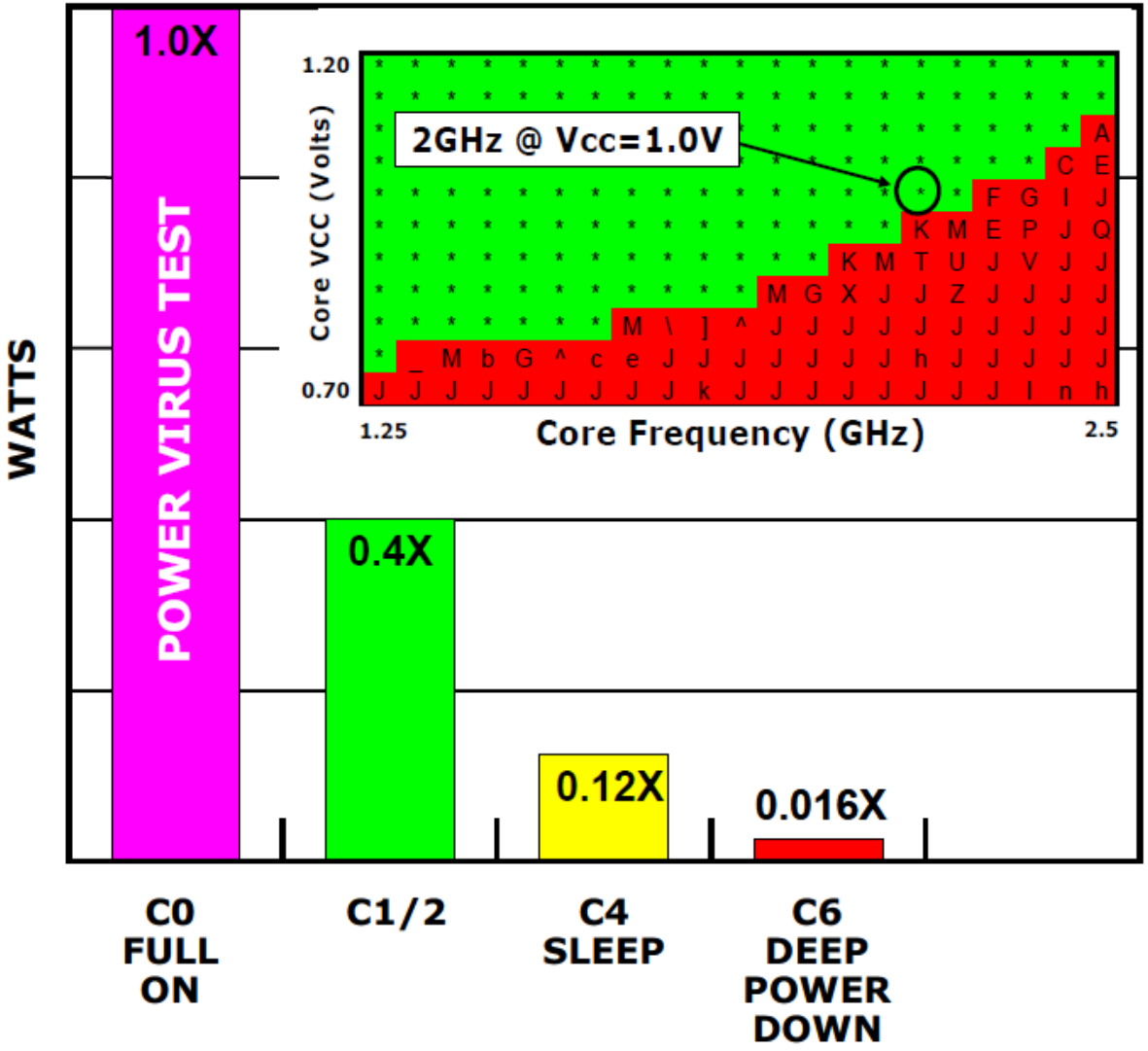


2.2 The microarchitecture of the 45 nm Bonnell CPU (15)

Main features of the C6 Package state [44]

- Exit latency of the C6 state of the Bonnell microarchtecture: ≈ 100 μs.
- C6 residency: ≈ 80 – 90 %.
- Average power consumption in the C6 state: ≈ 220 mW.

C state power consumption of the Bonnell CPU-based Silverthorne processor [47]



Introduction of the Burst Mode in the Bonnell CPU-based Lincroft processor of the Moorestown smartphone platform (5/2010) [54]

- About two years after the introduction of the Bonnell CPU Intel introduced the Burst mode technology in their Atom line.
- With the Burst Mode introduced additional P-states are exposed for the OS such that if there is a power headroom available, e.g. after an idle period, performance can be increased over the TDP limited performance for a short time.
- The Burst Mode introduced is controlled by the OS such that all available P-states (f_c/V_{core} states), including the p-states belonging to the Burst mode, are enumerated by the BIOS for the OS as available P-states.
- The OS directs the P-state usage according to the utilization grade of the CPU.

  This means that if there is a power headroom, e.g. after an idle period, and there is need for high performance, the OS requests the highest P-state (Burst frequency) and lets operate the processor in the Burst Mode until the chip or the external case becomes too hot, i.e. until the chips junction temperature (Tj) or the case temperature (Tskin) becomes higher than a predefined value (assuming that there is need for the highest P-state.

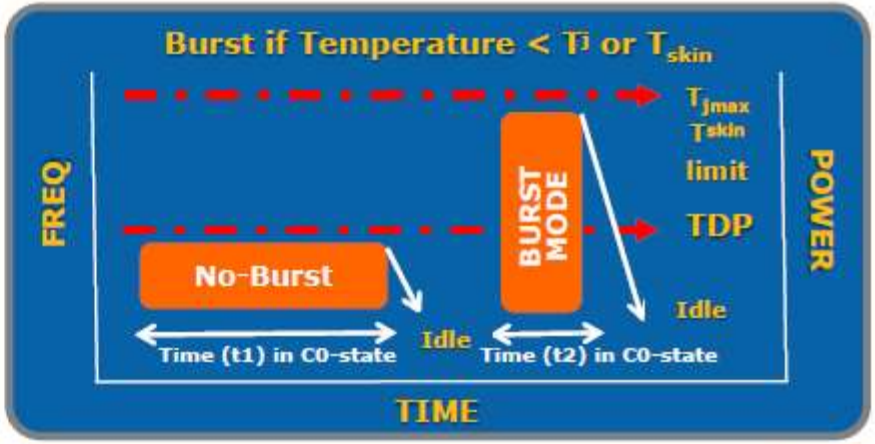
  In these cases the processor will be throttled to a lower operating point (P-state).

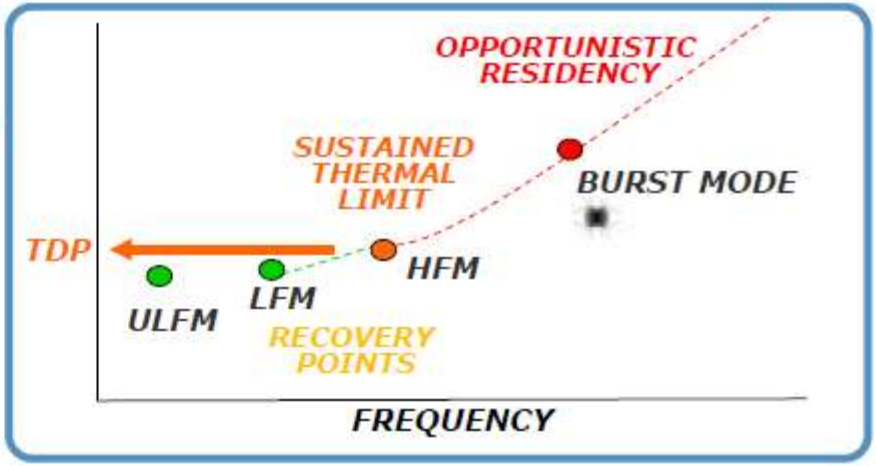
The next Figure illustrates the operation of the Burst Mode, as introduced in the Lincroft processor.

Intel's Burst mode technology as introduced into the Lincroft processor (5/2010) [18]

It is designated also as the Burst Performance Technology (BPT).

- Takes advantage of Thermal headroom on T_J and T_{Skin} for short duration
- System reduces frequency to Recovery points when T_{Skin} thresholds are exceeded





Intel® BPT provides on-demand performance and Battery Life Saving without impacting thermal design

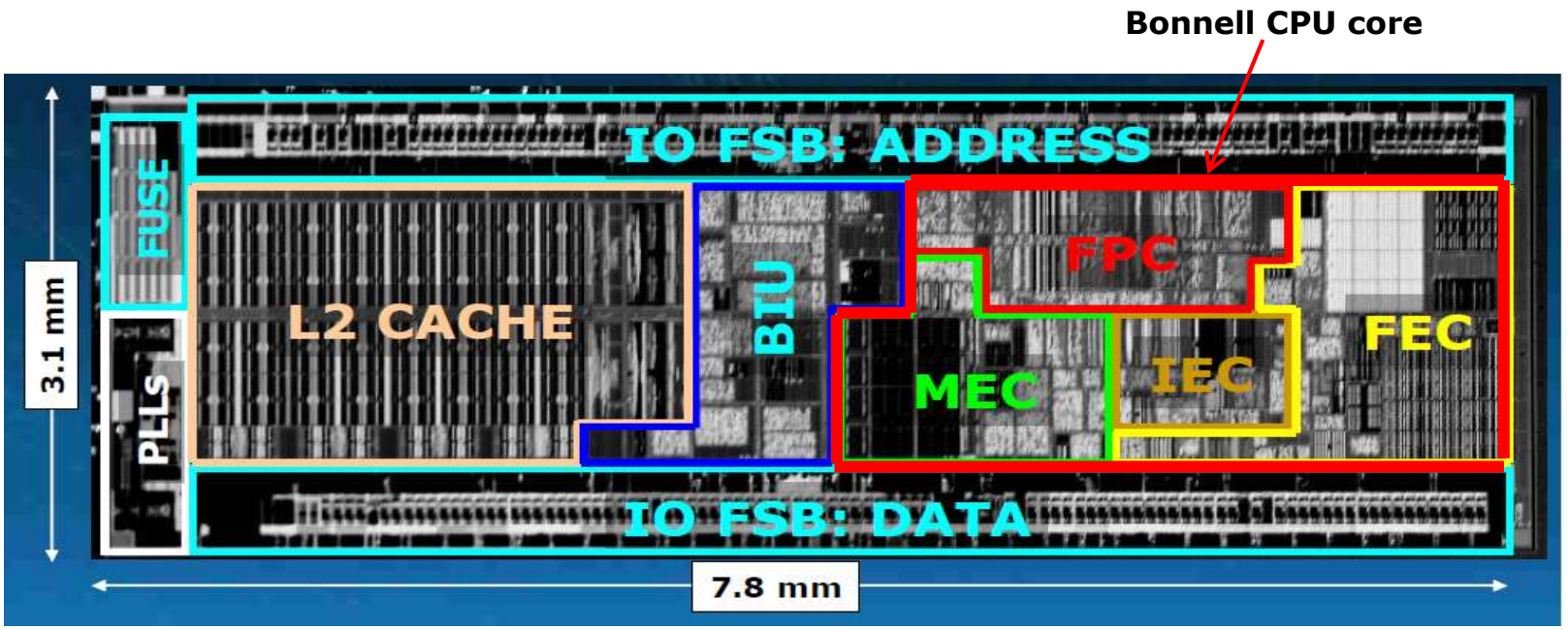
Remark

Skin temperature t_{skin} is the temperature of the computer case, like the case of a laptop.

If the laptop case becomes hotter than a given temperature it can be unpleasant for the user having the laptop on his or her lap.

2.2 The microarchitecture of the 45 nm Bonnell CPU (20)

Die plot of the Bonnell microarchitecture as part of the Silverthorne Atom processor [52]



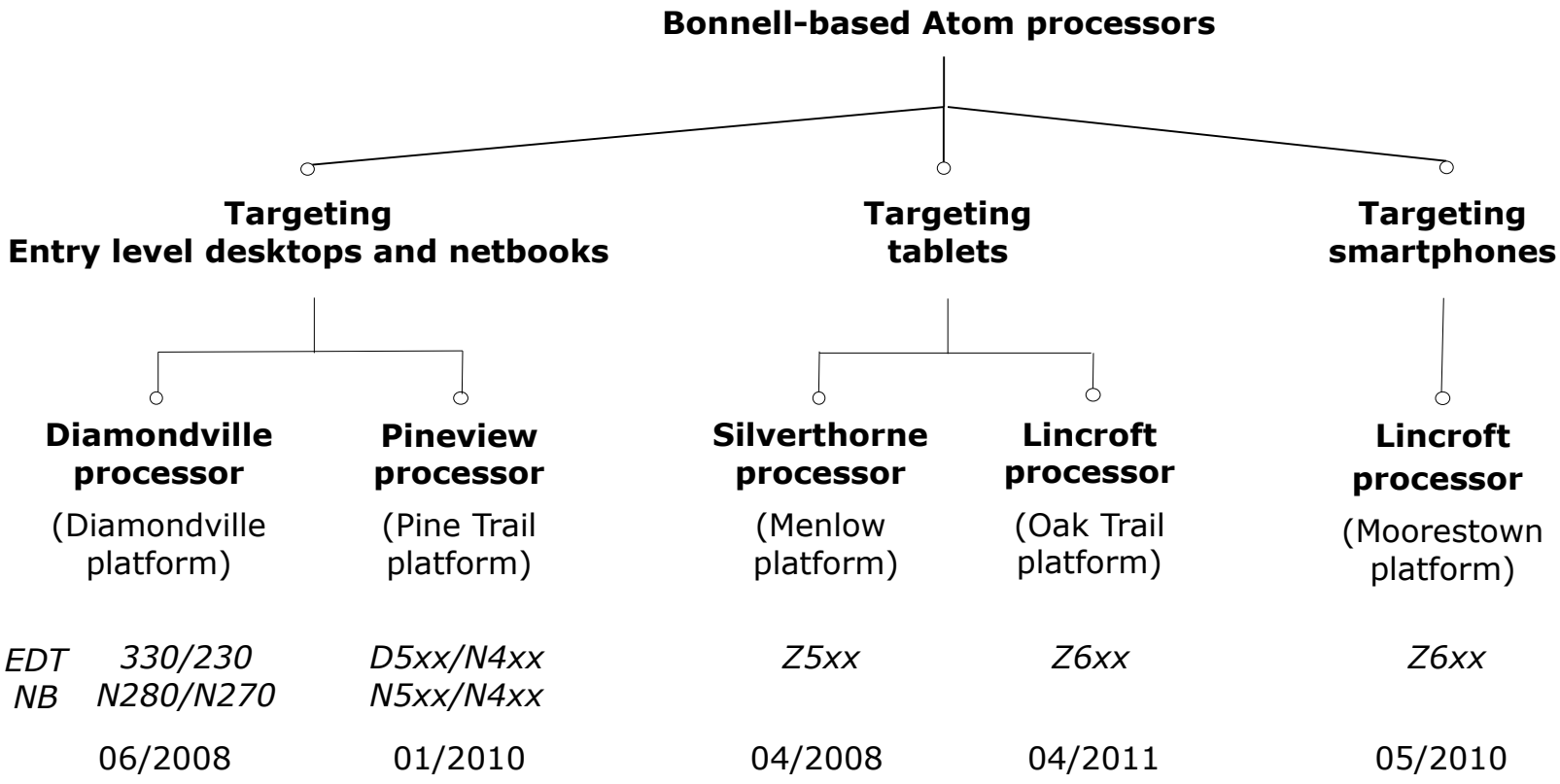
SCHEMATIC TRANSISTORS:	
Core:	13,828,574
Uncore:	2,738,951
L2 & L2 tag:	30,644,682
TOTAL:	47,212,207

	Area %
Core	28%
Uncore	72%
BIU	9%
L2	22%
IO FSB	35%
PLL+FUSE	7%
Total	100%

FEC: front-end cluster (plus L1 instruction cache)
FPC: floating point cluster
IEC: instruction execution cluster
MEC = memory execution cluster (with L1 data cache)
BIU = bus interface unit

2.2 The microarchitecture of the 45 nm Bonnell CPU (21)

Overview of Bonnell-based Atom processors



EDT: Entry-level Desktop
NB: Netbook

2.3 The 32 nm Saltwell CPU

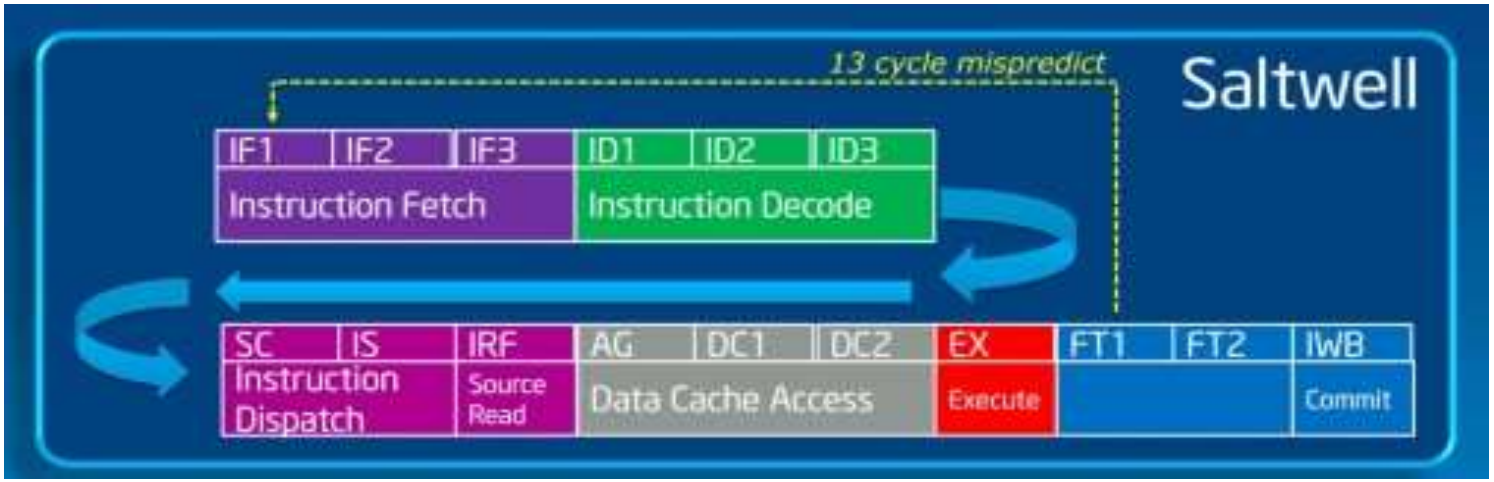
2.3 The 32 nm Saltwell CPU

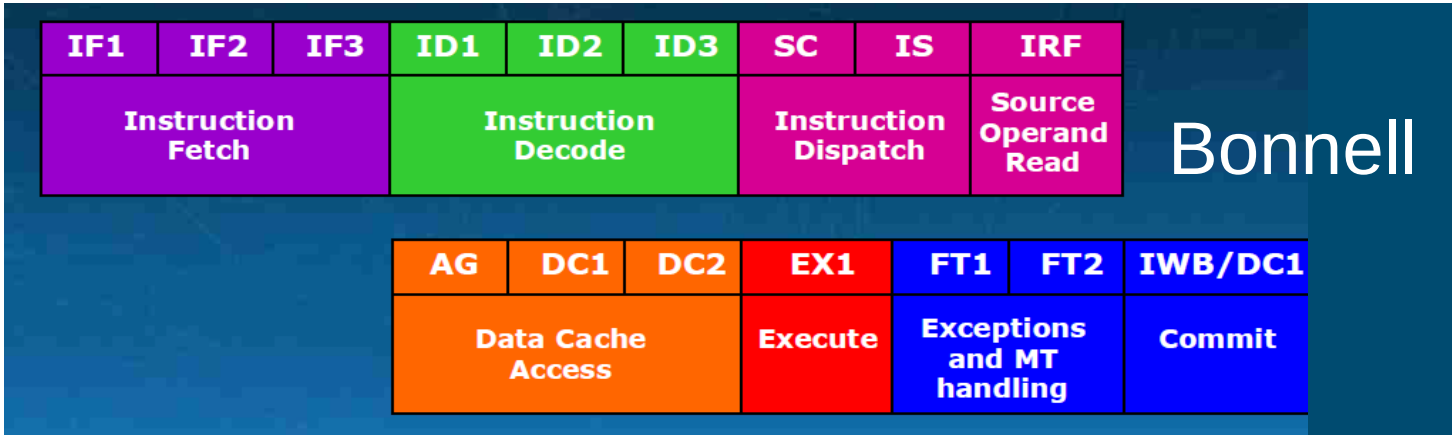
- Introduced
  - in 11/2012 as part of the Cedarview-M processor that belongs to the Cedar Trail-M entry level desktop/netbook platform and
  - in 01/2012 as part of the Penwell processor that belongs to the Menlow smartphone platform.
- It is the 32 nm shrink of the 45 nm Bonnell CPU with a few enhancements relating to the microarchitecture, like doubling the size of the Gshare branch predictor and further improvements, as detailed in [55].

  Additional enhancements relate to the power management, like
  - reducing the active power of the CPU PLL,
  - separating voltage rails for the CPU and the L2 cache and
  - enabling full power-gating of the CPU in the C6 standby mode [56].
- The Saltwell CPU has the same pipeline stages as the Bonnell CPU, as indicated below.

2.3 The microarchitecture of the 32 nm Saltwell CPU (2)

Pipeline stages of the Bonnell [52] **and Saltwell** [57] **CPUs**





2.3 The microarchitecture of the 32 nm Saltwell CPU (3)

Dynamic frequency/power range of the Saltwell CPU [56]

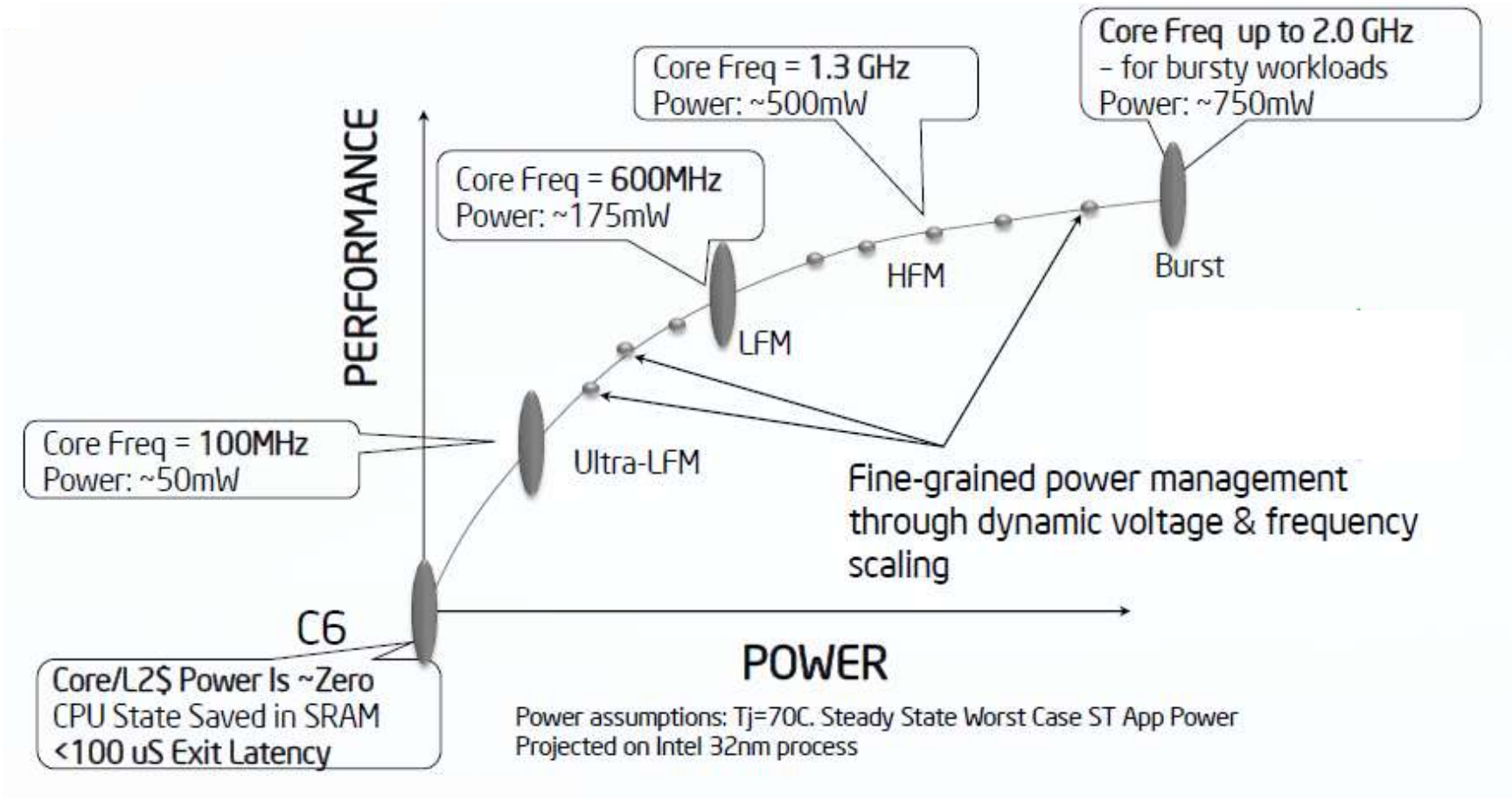
- Active CPU power management is accomplished by dynamic frequency voltage scaling by means of P-states controlled under Enhanced Intel SpeedStep Technology.
- The dynamic clock range spans from 600 MHz (termed as LFM, i.e. Low frequency Mode) at 175 mW to 1.3 GHz (termed as HFM i.e. High Frequency Mode) at 500 mW.
- Further on there is a burst mode for light workloads the CPU can run up to 2.0 GHz consuming 1200 mW for short periods of time.

The burst mode is sustained until thermal monitors placed on the platform, the processor or the CPU indicate that the thermal limits has been reached.

When this occurs, a combination of firmware and software throttle the CPU back into al lower P-state.

2.3 The microarchitecture of the 32 nm Saltwell CPU (4)

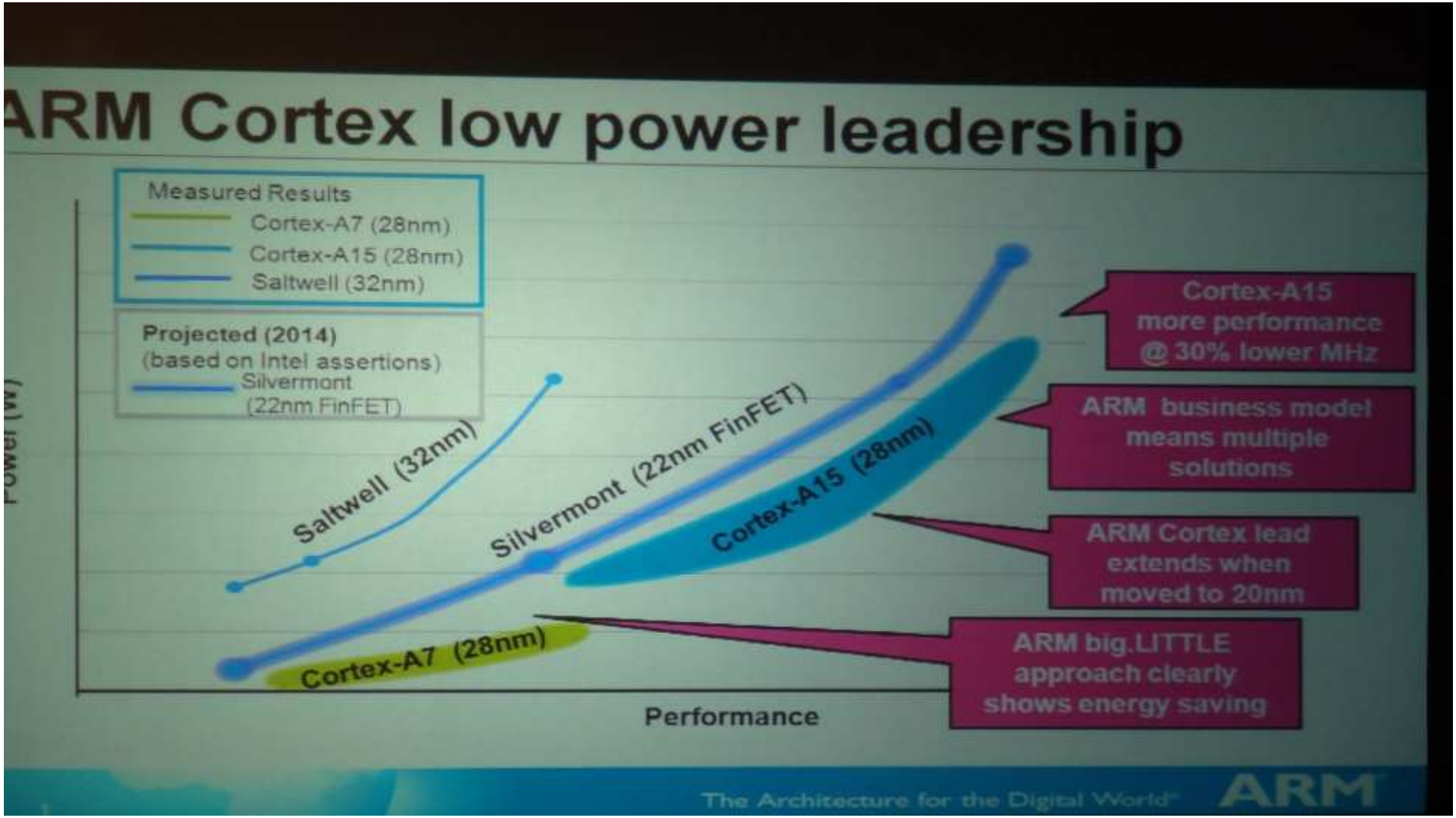
Dynamic frequency/power range of the Saltwell CPU based Z2480 (Pennwell) processor of the Medfield platform [58]



HFM: High Frequency Mode
LFM: Low Frequecy Mode
Ultra-LFM: Ultra-Low Frequency Mode

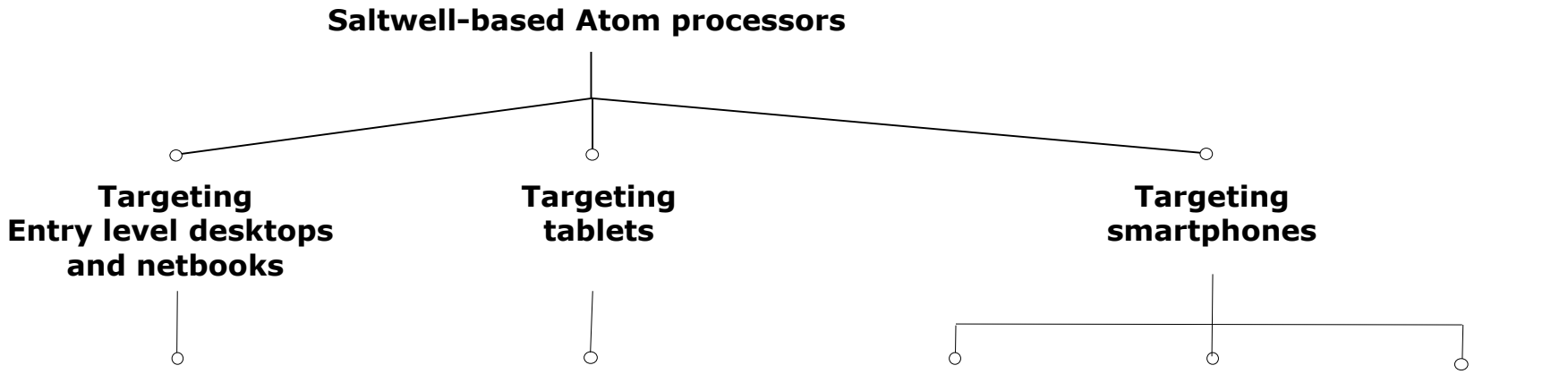
2.3 The microarchitecture of the 32 nm Saltwell CPU (5)

ARM's Figure about performance and power consumption of their and Intel's CPUs [138]



2.3 The microarchitecture of the 32 nm Saltwell CPU (6)

Overview of Saltwell-based Atom processors



EDT: Entry-level Desktop
NB: Netbook

2.4 The 22 nm Silvermont CPU

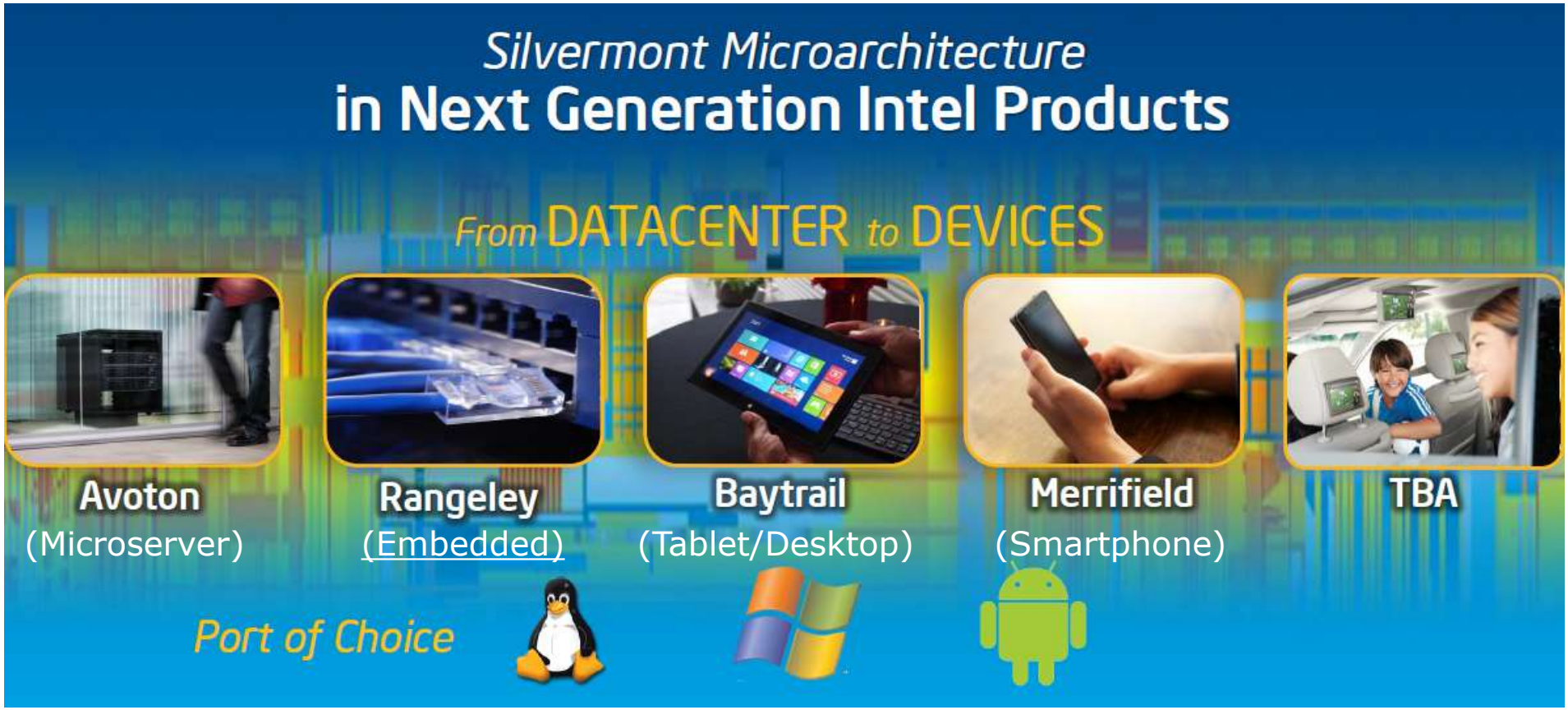
2.4 The 22 nm Silvermont CPU

Its key features

- The Silvermont CPU supports already the 32/64-bit x86 ISA.
- It underlies Intel's third generation Atom processors, such as the Valleyview D/M/T processors targeting all-in-one desktops, netbooks and tablets, respectively or the Merrifield processor targeting smartphones.
- Revealed in 5/2013, in products appeared in Q3/2013 to Q1/2014.
- It is manufactured using a 22 nm process.

2.4 The microarchitecture of the 22 nm Silvermont CPU (2)

Target markets of Silvermont-based products [61]



Spectrum of Intel's processors after the introduction of Silvermont-based devices [61]

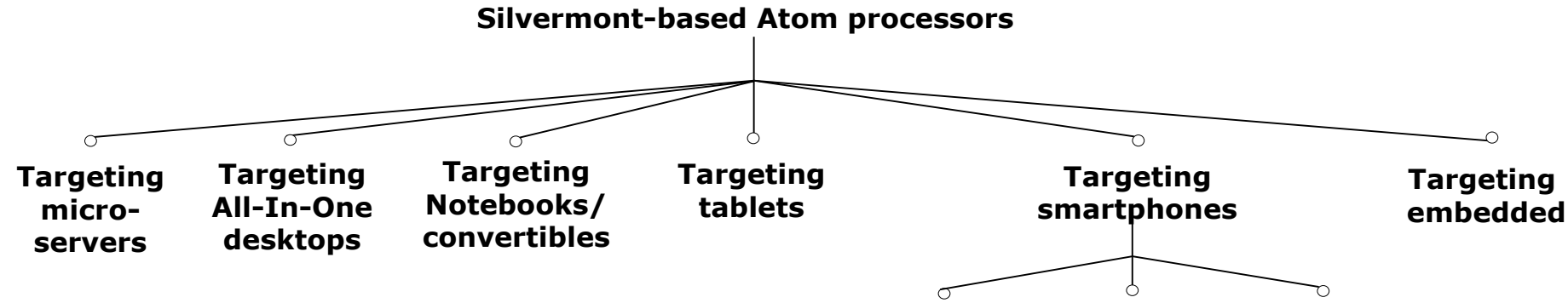
2.4 The microarchitecture of the 22 nm Silvermont CPU (4)

Main features of Silvermont-based products

- First Silvermont-based Atom products are typically dual or quad-core SOCs, whereas microservers include up to 8 cores [59].
- Silvermont-based SOCs are optimized first for Microsoft Windows 8 and Windows Phone, but Intel subsequently optimized their tablet and laptop processors also for Google's Android and other Linux-based Oss as well [59].

2.4 The microarchitecture of the 22 nm Silvermont CPU (5)

Overview of Silvermont-based processors and platforms



Avoton processors	Valleyview-D processors	Valleyview-M processors	Valleyview-T processors	Merrifield processors	Moorefield processors	SoFIA processors	
(Edisonvile platform)	(Bay Trail-D platform)	(Bay Trail-M platform)	(Bay Trail-T platform)	(Merrifield platform)	(Moorefield platform)	(SoFIA (x3) platform)	
C2350 (2C) C25xx (4C) C27xx (8C)	J1xxx 2C/4C J2xxx 4C	N28xx 2C N29xx 4C N35xx 4C	Z3600 2C (Android) Z37xx 4C (Windows/ Android)	Z3460 2C Z3480 2C	E3800 1C/2C/4C	C23xx 2C C25xx 4C	C23xx 2C C25xx 4C

D: Desktop
M: Mobile
T: Tablet

Remark: The networking/communication aimed **Rangley processors** (C23xx (2C)/C25xx (4C)) are not shown

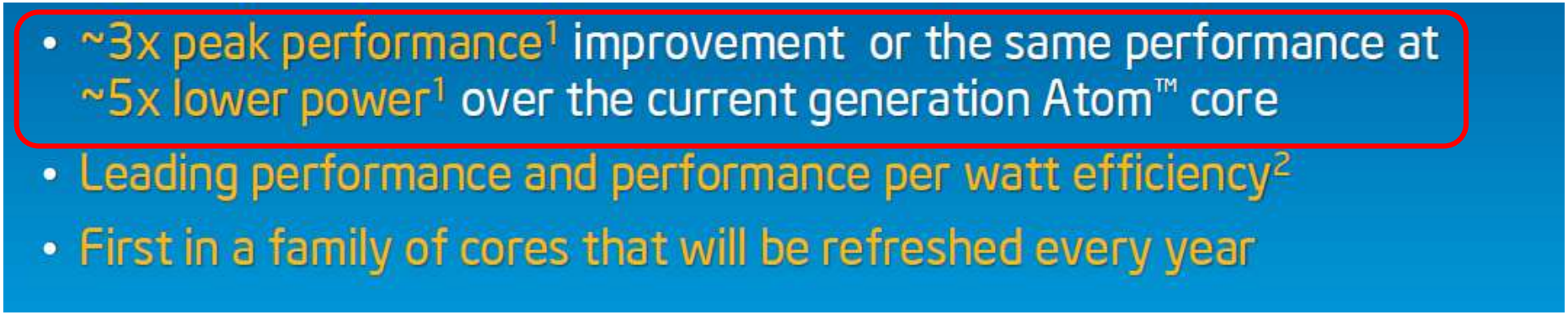
2.4 The microarchitecture of the 22 nm Silvermont CPU (6)

Categories of Bay Trail processors [106]

Bay Trail-T *For tablets*	Z3600 series: dual-core, targets Android Z3700 series: quad-core, targets Windows/Android
Bay Trail-M *For notebooks*	N2000 series: dual-core (N28xx), quad-core (N29xx) N3000 series: quad-core (N35xx)
Bay Trail-D *For desktops*	J1000 series: dual-core (J1750, J1800), quad-core (J1850, J1900) J2000 series: quad-core (J2900, J2850)

2.4 The microarchitecture of the 22 nm Silvermont CPU (7)

Key benefit of the Silvermont microarchitecture [60]



The Conroe core of the Core 2 line of Intel with its performance advantage over AMD's Athlon 64/Opteron processors was the basis for Intel's performance lead gained after 2006 and sustained until now in desktops and servers.

In view of some analysts (e.g. [60]) the Silvermont CPU core could become Intel's Conroe for the mobile market. But unlike Conroe Silvermont won't change the world overnight but would allow Intel to go forward and get more and more market share in tablets and smartphones.

In addition, after acquisitions, new hires and some significant internal organizational changes, Intel seems to focus finally on the mobile market.

Although the Bonnell core (Intel's first Atom core) marked Intel's entrance into the mobile segment, it's the Silvermont core (Intel's first new Atom microarchitecture since 2008) and Intel's new attitude to the mobile market that finally makes Intel really competitive with major players on the mobile field, like ARM, Apple and Qualcomm.

2.4 The microarchitecture of the 22 nm Silvermont CPU (8)

Key features of the microarchitecture of the Silvermont CPU core

- The Silvermont CPU has a two-wide, out-of-order superscalar microarchitecture.
- It does not supports hypertreading.
- Silvermont's microarchitecture is module-based with two cores per module, as detailed later.

2.4 The microarchitecture of the 22 nm Silvermont CPU (9)

The assumed reasoning behind not supporting hyperthreading (based on [60])

- Previous CPU cores of the Atom line supported hyperthreading to increase performance.
- Hyperthreading however, has an associated power penalty, but the performance gain achieved justified it.
- With 22 nm technology however, Intel came into the position to add in more cores for higher threaded performance. Obviously, twice as much cores provide significantly more performance potential than hyperthreading with resource constraints.
- On the other hand, with power gating Intel is able to switch off not used units with almost no penalty on static dissipation. So with about twice as much transistors available, quad cores without hypertreading seems to be a better design option than two cores with hypertreading or quad cores with hyperthrading.

2.4 The microarchitecture of the 22 nm Silvermont CPU (10)

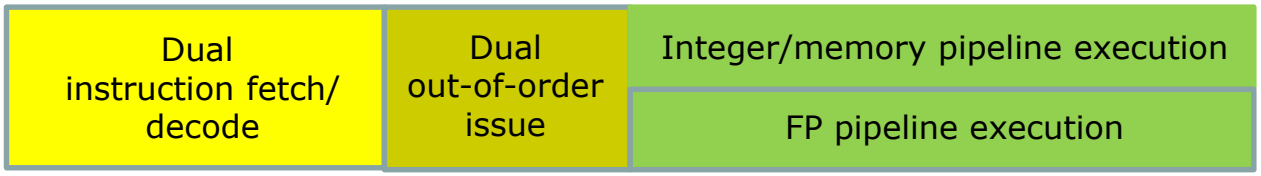
The assumed reasoning behind switching to out-of-order issue

- As stated in a number of papers, e.g. in [60], Intel's policy in accepting design options is, implement design options only if they promise at least twice as much performance gain than additional power consumption, e.g. at least 2 % performance gain for 1 % higher power consumption.
- Thus the chosen out-of-order design seems to satisfy the 2 to 1 design rule.

2.4 The microarchitecture of the 22 nm Silvermont CPU (11)

Simplified principle of operation of Silvermont's microarchitecture [51]

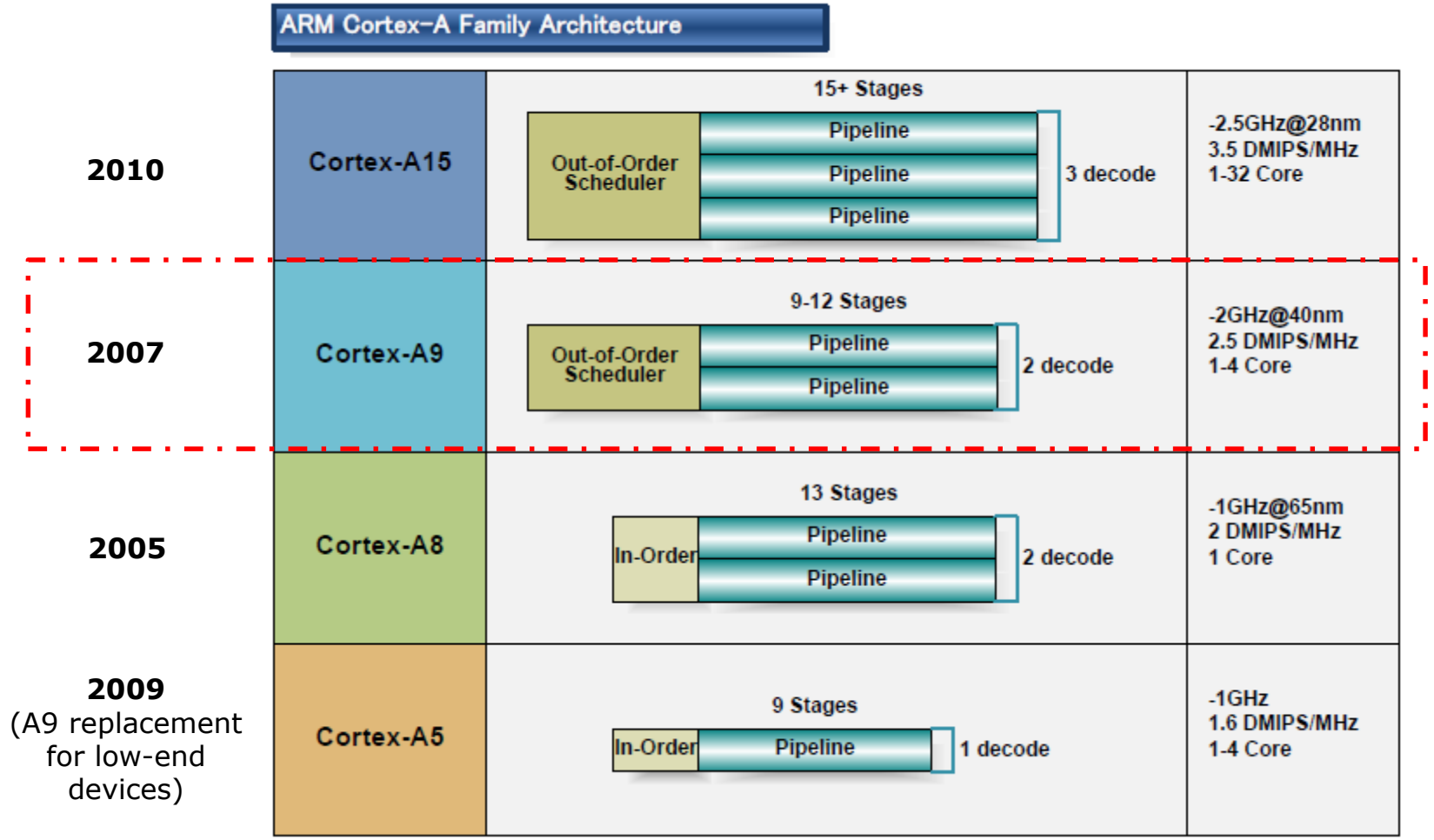
It is a two wide, out-of-order issue superscalar, as indicated below.



12-stage memory/14-stage integer pipeline

2.4 The microarchitecture of the 22 nm Silvermont CPU (12)

Comparing the principle of operation of Intel's Silvermont microarchitecture with that of ARM's Cortex line of processors [45]

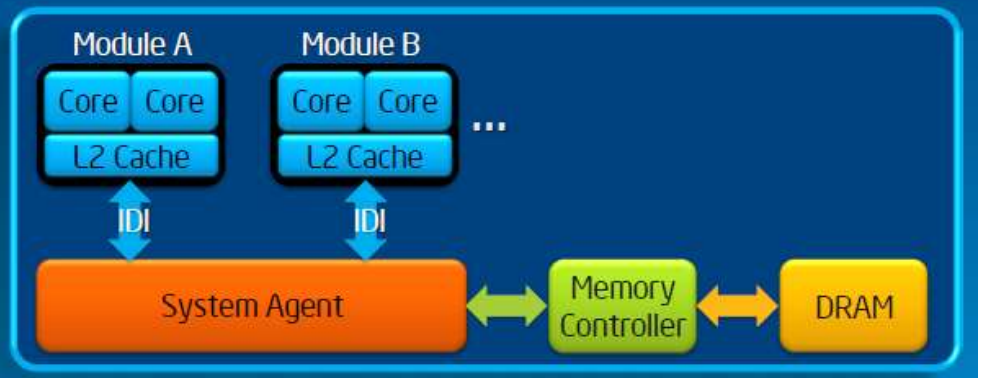


The number of pipeline stages relates to the integer/memory pipeline

2.4 The microarchitecture of the 22 nm Silvermont CPU (13)

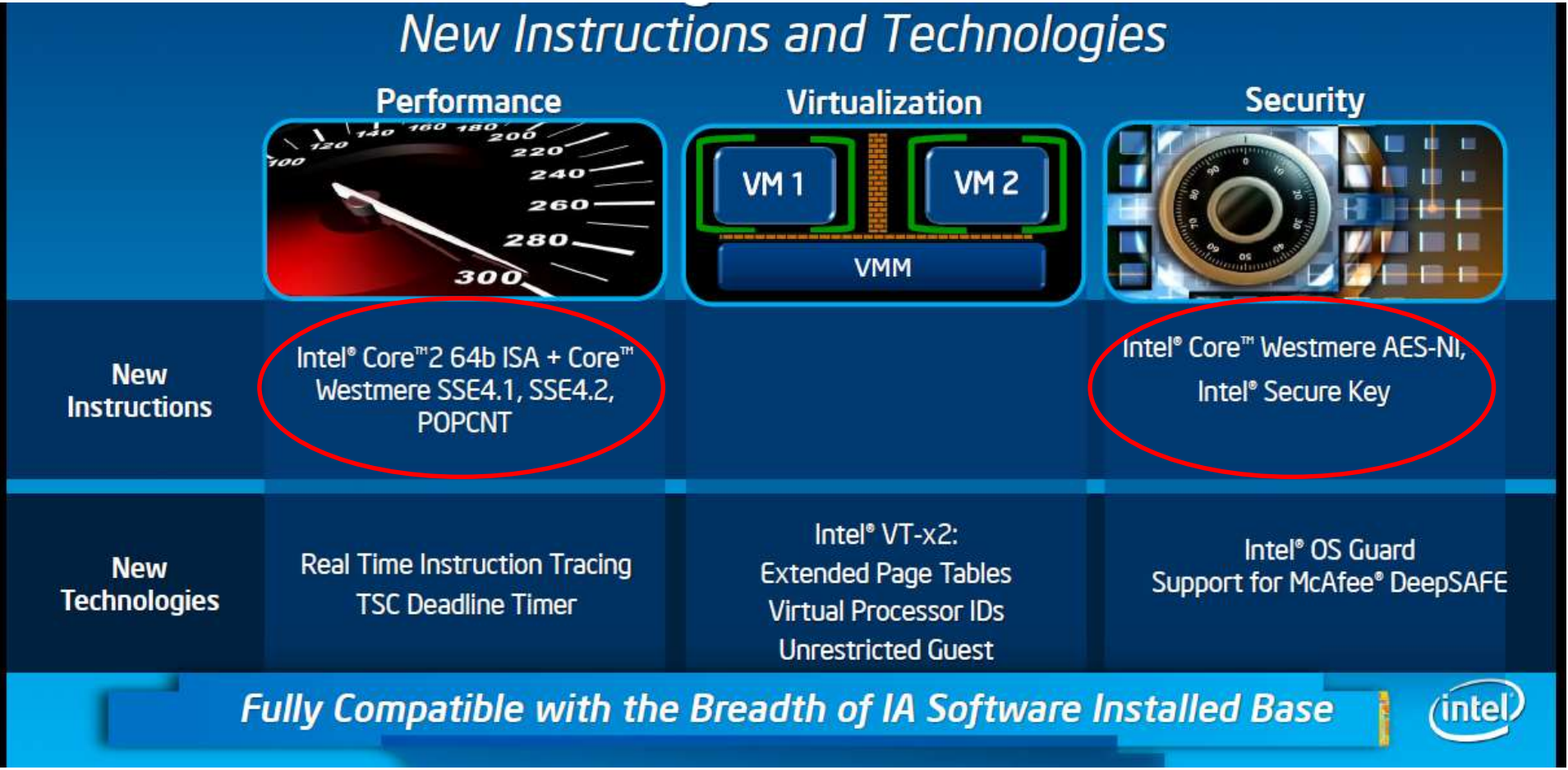
The modular structure of the Silvermont CPU [61]

- "Module" building block-based expansion from 1 to 8 cores
- "Module" contains:
  - Two cores
  - Tightly coupled second-level cache (up to 1MB): very low latency, high bandwidth
  - Dedicated point-to-point interface (IDI) to SOC Fabric
    - Independent read, write channels
    - Higher bandwidth, Lower Latency, OOO transaction support
- Per-core frequency and power management support



2.4 The microarchitecture of the 22 nm Silvermont CPU (14)

ISA extensions and new technologies introduced by Silvermont [61]



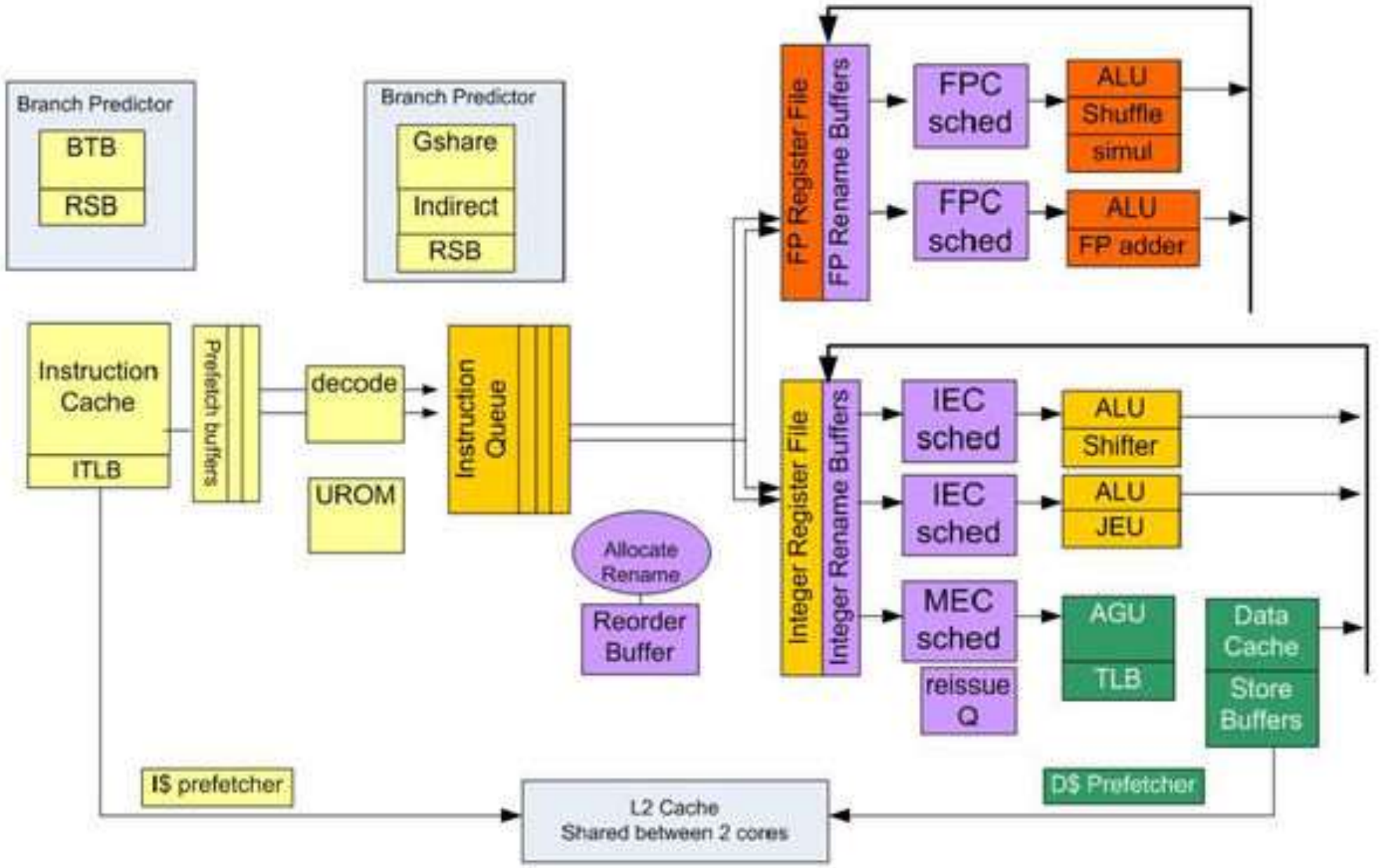
2.4 The microarchitecture of the 22 nm Silvermont CPU (15)

New instructions introduced into the Silvermont core [143]

	Feature	Description	Benefits
Security	Intel® AES New Instructions[1]	Instructions to perform AES encryption and decryption	• Supports 128, 192, 256 bit keys and all modes of operation • Mitigates all known software side channel attacks
	PCLMULQDQ instruction	New instruction to improve AES-GCM (Galois Counter Mode) performance	• High Performance Message Authentication
	Intel® Secure Key[2] (RDRAND instruction)	Provides high quality random numbers to all software	• Harden attack surface
Performance	VM Functions (VMFUNC)	Allow VMX non-root to load new EPT pointers	• Hardware assists for security technologies
	Intel® SSE4.1	47 new instructions	• Primitives for compiler auto-vectorization • Media acceleration • Streaming loads to speed up accesses to device memory
	Intel® SSE4.2, POPCNT	7 new instructions	• Accelerated String and Text Processing of Large Data Sets

2.4 The microarchitecture of the 22 nm Silvermont CPU (16)

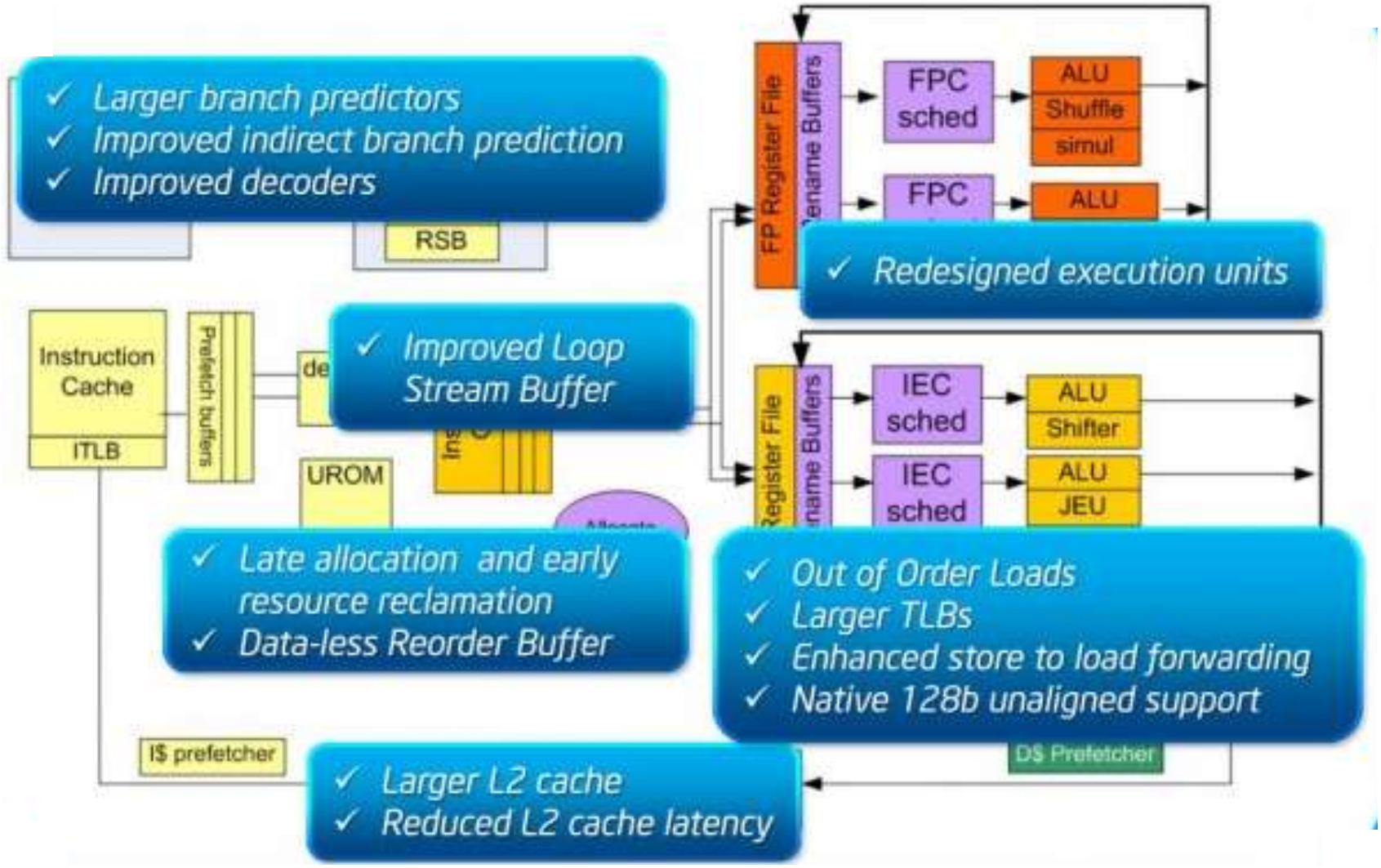
Silvermont's block diagram [143]



Only a subset of the SIMD EUs have 128-bit wide data paths in contrast to the Goldmont core [144]

2.4 The microarchitecture of the 22 nm Silvermont CPU (17)

Major enhancements of Silvermont's micro-architecture [143]

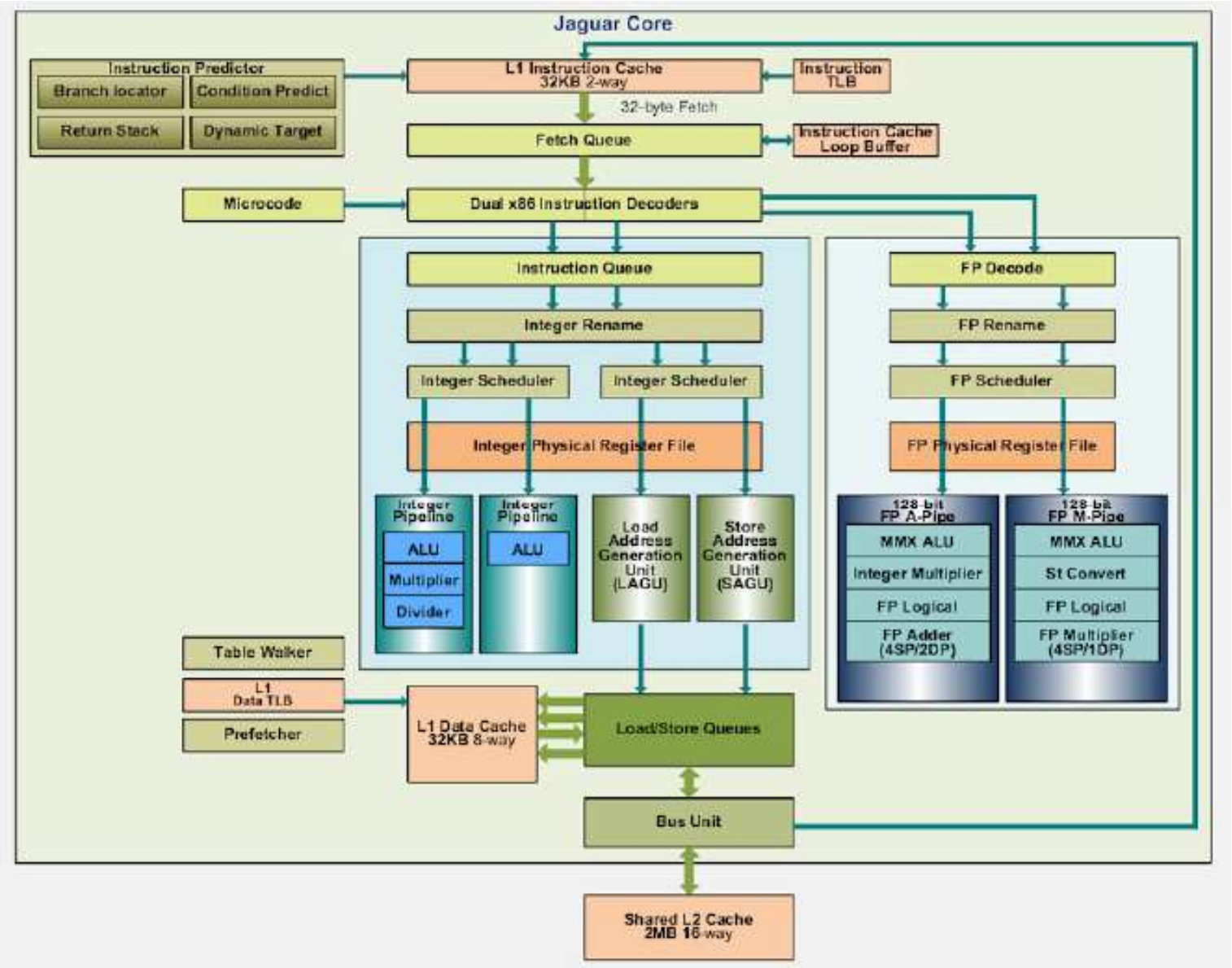


Comparing Intel's Silvermont and of AMD's Jaguar microarchitectures

A comparison of both microarchitecture shows that both are very similar to each other.

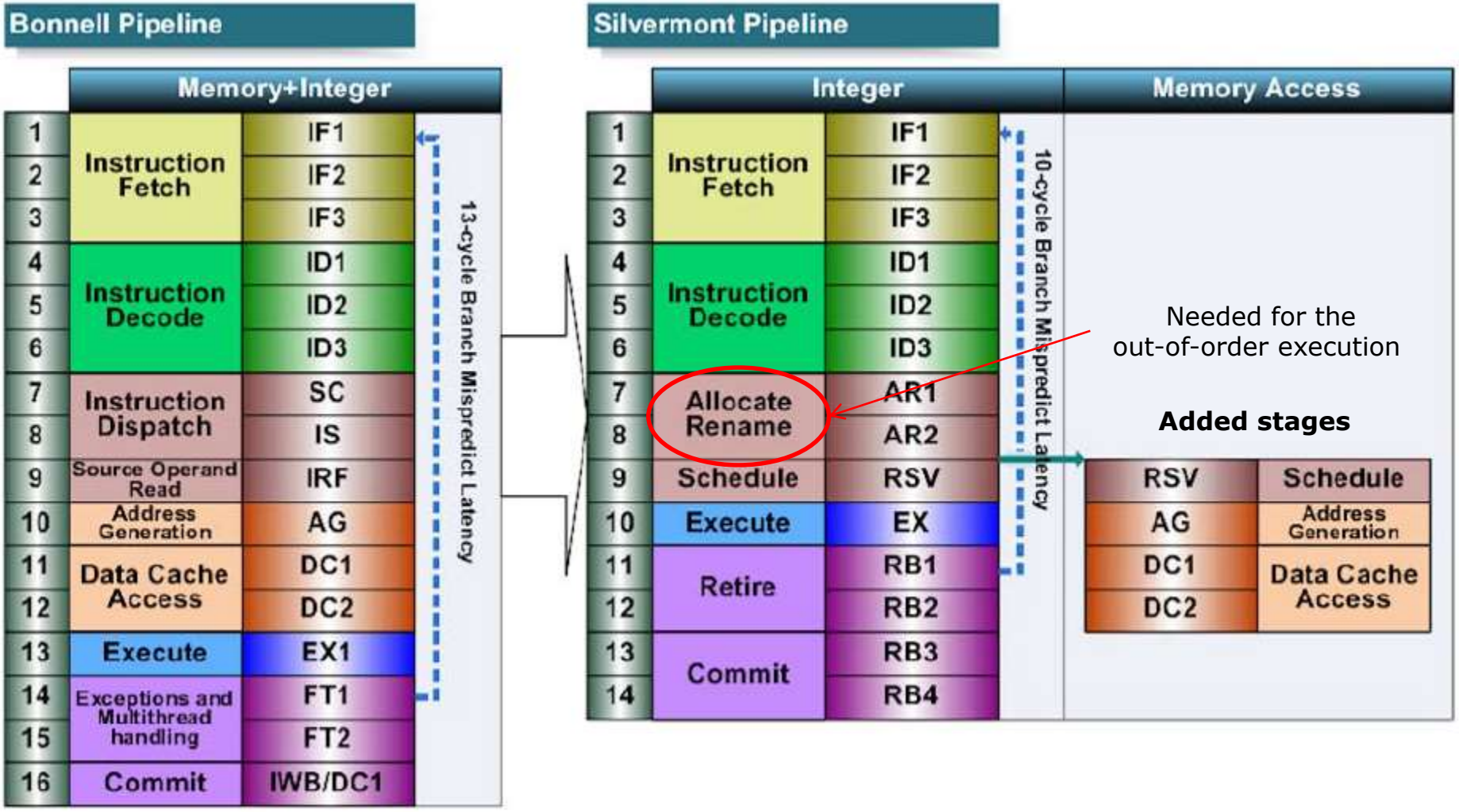
2.4 The microarchitecture of the 22 nm Silvermont CPU (19)

For comparison: AMD's Jaguar microarchitectures [51]



2.4 The microarchitecture of the 22 nm Silvermont CPU (20)

Silvermont's pipeline vs. Bonnell's pipeline [51]



2.4 The microarchitecture of the 22 nm Silvermont CPU (21)

Comparing Silvermont's pipeline with the Bonnell/Saltwell pipeline [60]

Improving the mispredict penalty

- In the previous pipeline implementations (Bonnell's or Saltwell's pipelines) all instructions, including those that didn't have cache accesses (since their operations were in registers) had to go through the data cache access stages even if nothing happened during these stages.
- Silvermont's pipeline allows to bypass these stages if the instructions don't need memory data, this shortens the mispredict penalty from 13 cycles down to 10 cycles.

Improving branch prediction

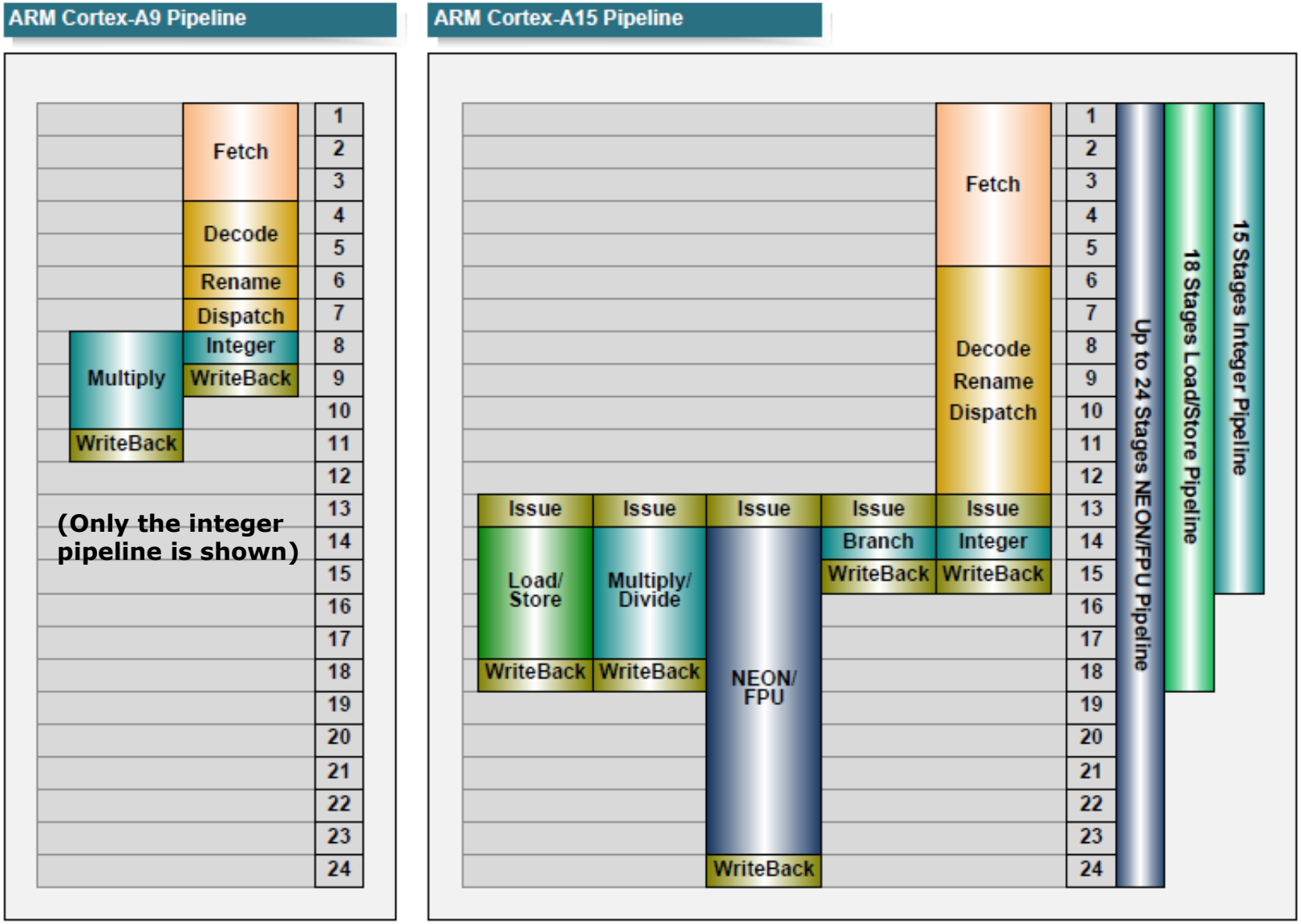
- In Silvermont's mictroarchitecture Intel significantly increased the size of the associated data structures and added an indirect branch predictor.
- Improvements of branch prediction increased IPC by about 5 -10 %.

Retire and commit stages

- Retire and commit are designations often used as synonyms.
- Related to the Silvermont pipeline Intel makes a not usual differentiation between these pipeline stages (without giving any details).

2.4 The microarchitecture of the 22 nm Silvermont CPU (22)

For comparison: ARM's Cortex-A9 and A15 pipelines [63]



Improved Burst Mode

Introduction of the Burst Mode in Intel's Atom lines [54]

- In their Atom lines Intel introduced the Burst mode technology in the Bonnell CPU-based Lincroft processor of the Moorestown smartphone platform (5/2010).
- With the Burst Mode introduced additional P-states are exposed for the OS such that if there is a power headroom available, e.g. after an idle period, performance can be increased over the TDP limited performance for a short time.
- The Burst Mode introduced is controlled by the OS such that all available P-states (f_c/V_{core} states), including the p-states belonging to the Burst mode, are enumerated by the BIOS for the OS as available P-states.
- The OS directs the P-state usage according to the utilization grade of the CPU.

  This means that if there is a power headroom, e.g. after an idle period, and there is need for high performance, the OS requests the highest P-state (Burst frequency) and lets operate the processor in the Burst Mode until the chip or the external case becomes too hot, i.e. until the chips junction temperature (Tj) or the case temperature (Tskin) becomes higher than a predefined value (assuming that there is need for the highest P-state.

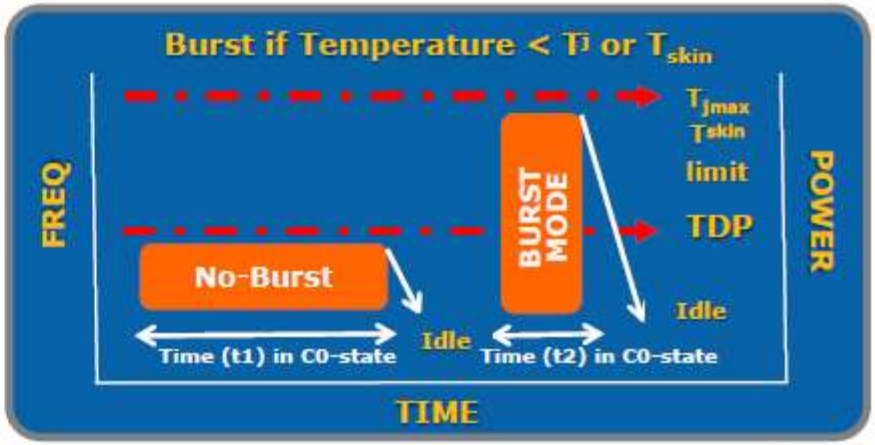
  In these cases the processor will be throttled to a lower operating point (P-state).

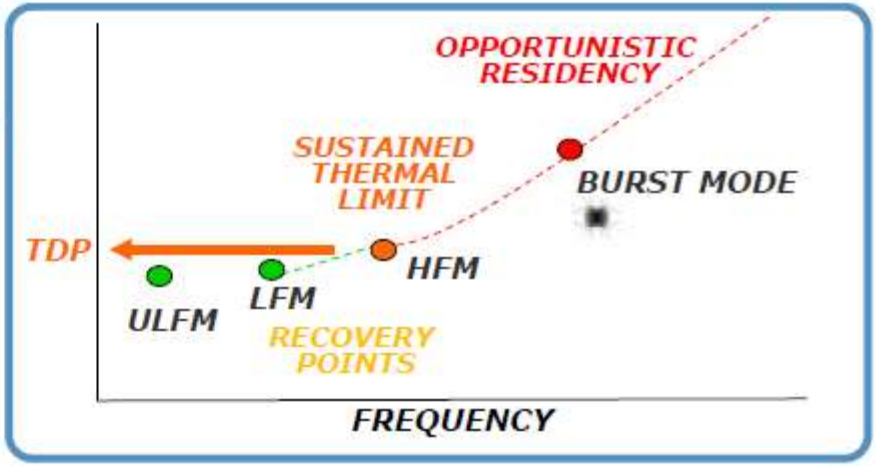
The next Figure illustrates the operation of the Burst Mode, as introduced in the Lincroft processor.

Intel's Burst mode technology as introduced into the Lincroft processor (5/2010) [18]

It is designated also as the Burst Performance Technology (BPT).

- Takes advantage of Thermal headroom on T_J and T_{Skin} for short duration
- System reduces frequency to Recovery points when T_{Skin} thresholds are exceeded





Intel® BPT provides on-demand performance and Battery Life Saving without impacting thermal design

Remark 1

Skin temperature t_{skin} is the temperature of the computer case, like the case of a laptop.

If the laptop case becomes hotter than a given temperature it can be unpleasant for the user having the laptop on his or her lap.

Remark 2

Here we note that the Burst mode as introduced into the Atom line is similar to the Turbo Boost technology introduced into the Nehalem processor in 11/2008 nevertheless it differs in implementation details.

On the other hand, subsequently also the Turbo Boost technology was further developed to the Turbo Boost technology 2.0 in Sandy Bridge processors (1/2011).

2.4 The microarchitecture of the 22 nm Silvermont CPU (27)

Silvermont's enhancements of the Burst Mode [61]

- The Burst Mode in the Silvermont processor is managed by a microcontroller rather than by the OS, and operates based on thermal, electrical and power delivery constrains.
- Power will be shared
  - between CPU cores
  - between CPU cores and dedicated cores (termed also as SOC IPs (e.g. a graphics core (GFX)), and
- the Burst Mode supports dynamic burst operation, as indicated next, and detailed later for the dynamic burst operation.

Power sharing between CPU cores [61]

Burst Mode Improvements

- Prior Atom™ cores
  - Opportunistically exposed additional P-states based on available thermal headroom
- Silvermont enhancements
  - Burst frequency managed in hardware based on Thermal, Electrical and Power Delivery constraints
  - Power sharing between CPU cores and SOC IPs (e.g. Graphics) is supported
  - Burst operating points can be dynamically adjusted

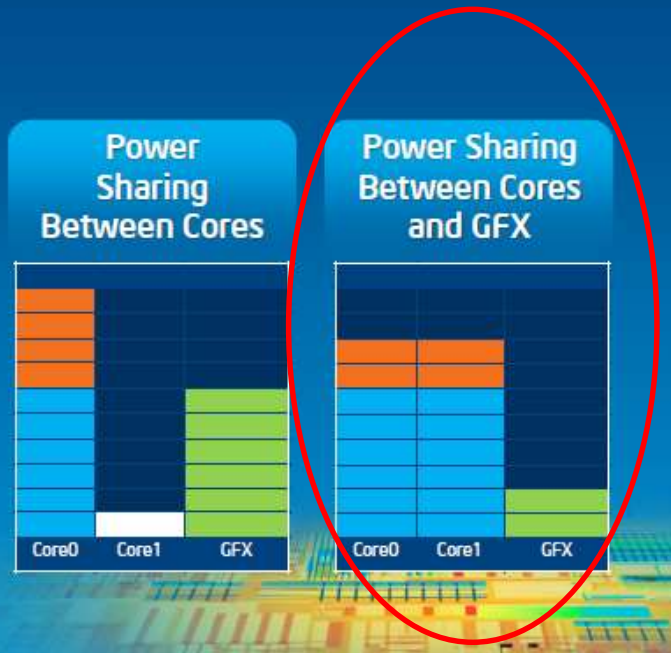
Maximize Performance within Platform Capabilities

intel

Power sharing between CPU cores and the graphics core (GFX) [61]

Burst Mode Improvements

- Prior Atom™ cores
  - Opportunistically exposed additional P-states based on available thermal headroom
- Silvermont enhancements
  - Burst frequency managed in hardware based on Thermal, Electrical and Power Delivery constraints
  - Power sharing between CPU cores and SOC IPs (e.g. Graphics) is supported
  - Burst operating points can be dynamically adjusted

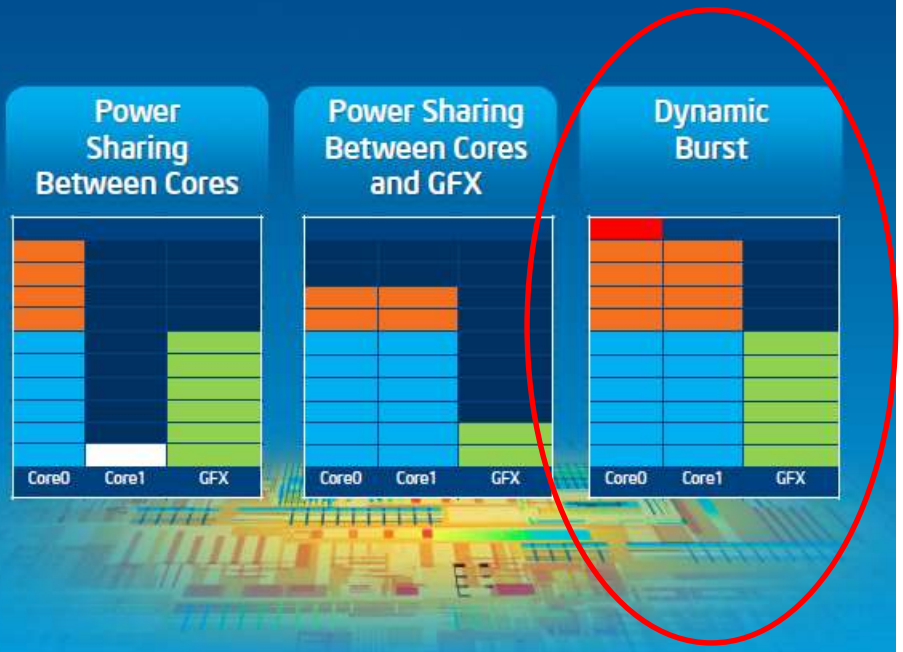


Maximize Performance within Platform Capabilities

Dynamic burst operation [61]

Burst Mode Improvements

- Prior Atom™ cores
  - Opportunistically exposed additional P-states based on available thermal headroom
- Silvermont enhancements
  - Burst frequency managed in hardware based on Thermal, Electrical and Power Delivery constraints
  - Power sharing between CPU cores and SOC IPs (e.g. Graphics) is supported
  - Burst operating points can be dynamically adjusted



Maximize Performance within Platform Capabilities

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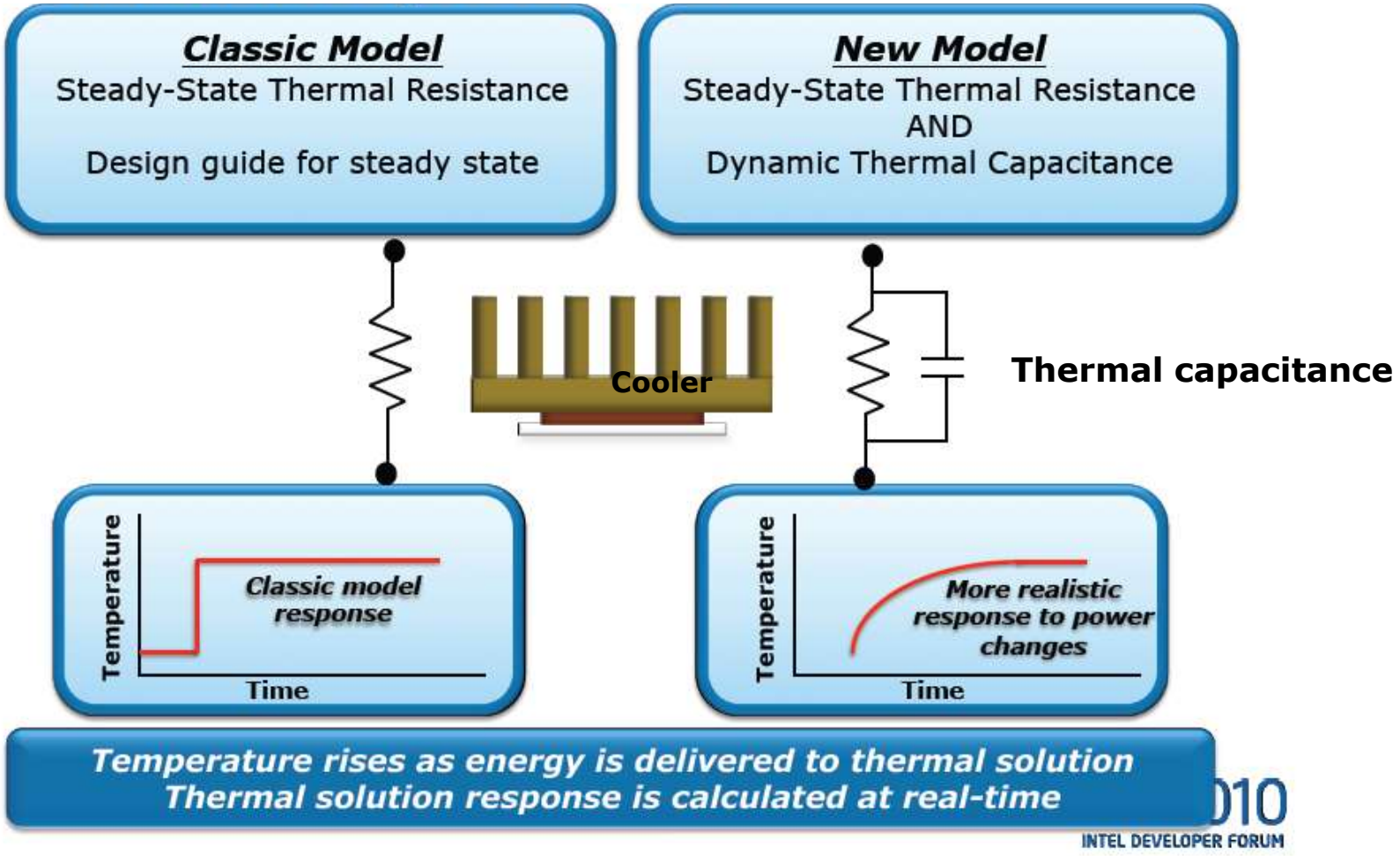
The Dynamic Burst operation

Dynamic Burst operation is similar to Intel's Turbo Boost 2.0 technology that was introduced in the Sandy Bridge line (1/2011) and will be recapped subsequently.

Intel's Turbo Boost 2.0 technology [64]

The concept of the 2.0 generation Turbo Boost technology

The concept utilizes the real temperature response of processors to power changes in order to increase the extent of overclocking [64]



The concept of dynamic Turbo mode: While taking into account the fact that the temperature of a device will rise only slowly, use "thermal "energy budget" accumulated during idle periods to push the core clock far beyond the TDP value for short periods of time (e.g. for 20 sec).

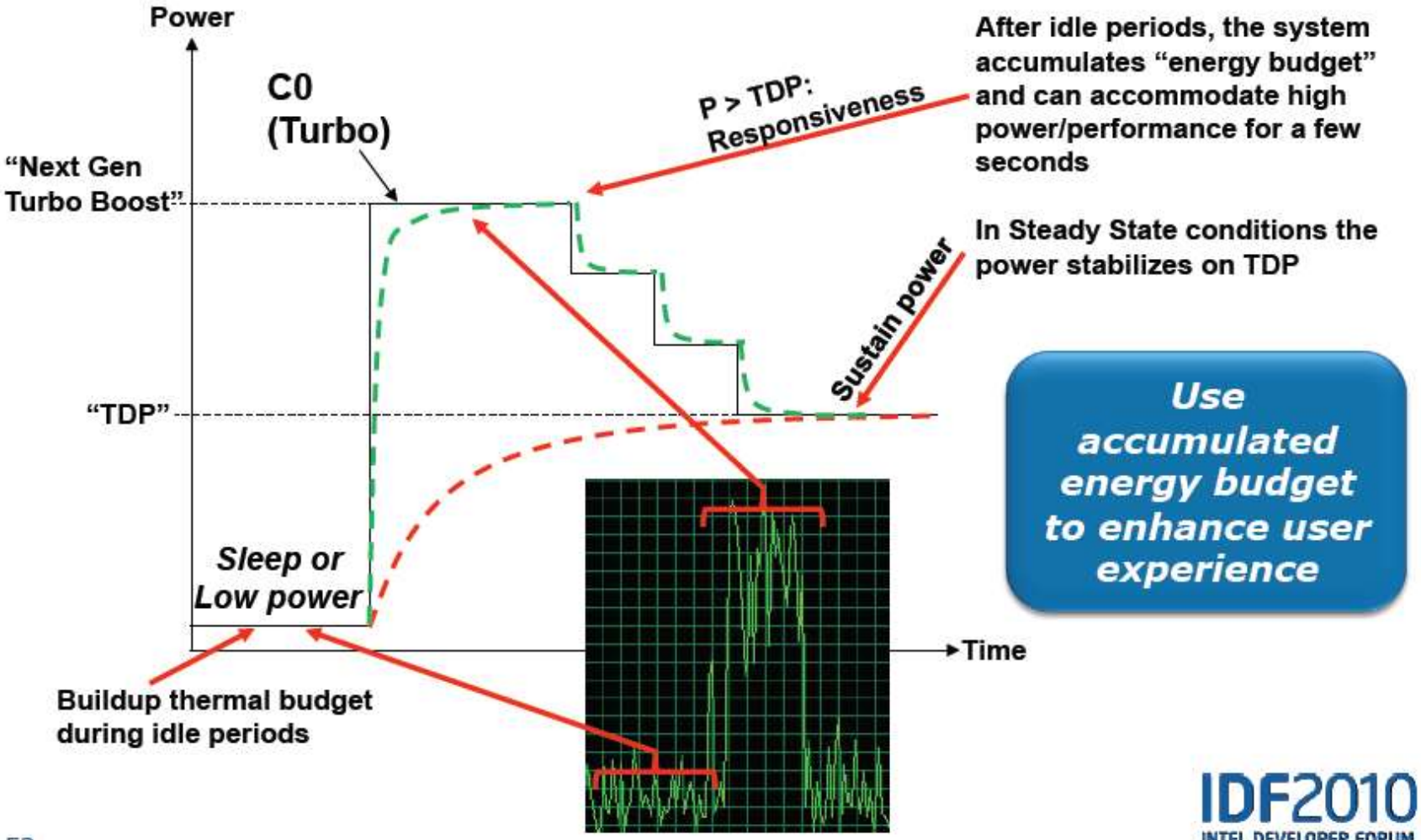
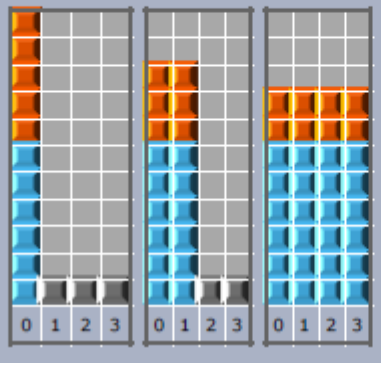


Figure: The concept of dynamic Turbo mode [64]

The evolution of Intel's Turbo Boost technology [65]

Turbo Boost 1.0 | Turbo Boost 2.0

Client	Merom/ Penryn (Mobile only)	Nehalem/Westmere: NHM/M Clarksfield, NHM/D Lynnfield/Clarkdale	WSM/M Arrandale, WSM/D	Sandy Bridge
Key New Capabilities	• 1 turbo bin when other core is asleep	• Turbo controlled within power limit • Multi-core turbo • More turbo if cores are asleep	• Graphics Dynamic Frequency • Driver controlled power sharing between IA and Graphics (Mobile)	• HW controlled power sharing between IA cores and Graphics • Dynamic Turbo provides high responsiveness • More Turbo headroom from Improved power monitoring and control
Turbo Behavior Illustrative only. Does not represent actual number of turbo bins.		Quad Core Die Single Core Turbo / Dual Core Turbo / Quad Core Turbo 	Dual Core Die Single Core Turbo / Dual Core Turbo / Graphics Turbo 	Dual Core Die / Quad Core Die 

2.4 The microarchitecture of the 22 nm Silvermont CPU (35)

Note that in both Turbo Boost implementations individual cores may run at different frequencies but all cores share the same power plane.

Note also that Intel's Turbo Mode implementations in the Bonnell and Silvermont CPUs of the Atom line correspond roughly to Intel's Turbo Boost 1.0 and 2.0 implementations used in the Core 2 based lines.

Improved C state management [53]

From the C6 low power state Intel made already use in their Bonnell CPU.

Nevertheless, the Bonnell CPU was dual threaded, thus the CPU could flush L2 and enter the Package C6 state only after both threads have already saved their state and entered the Thread C6 state.

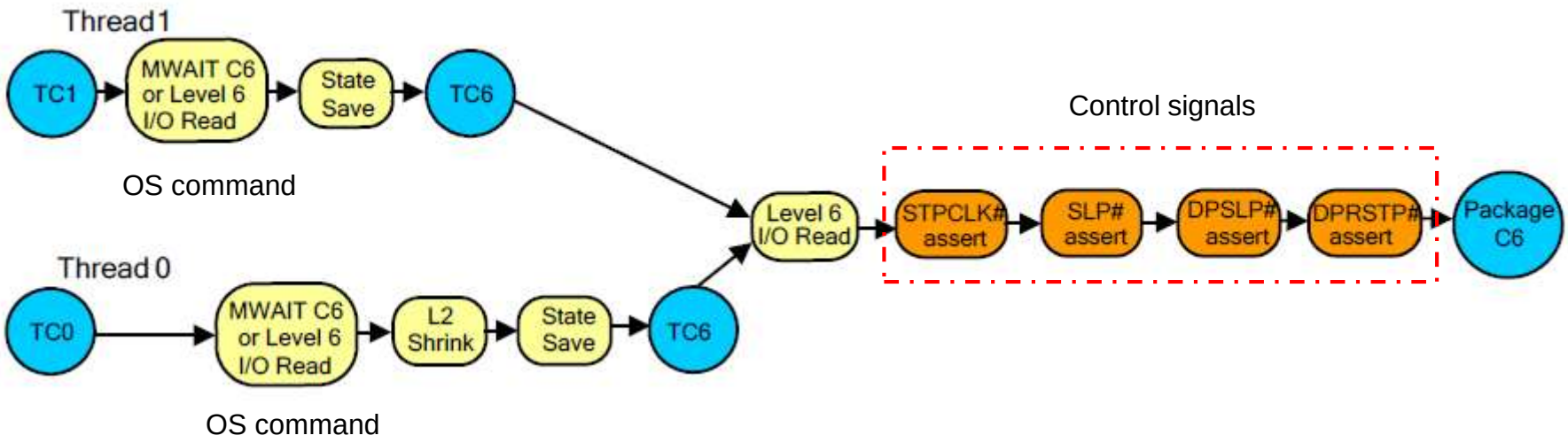


Figure: The sequence of entering the C6 Package state [53]

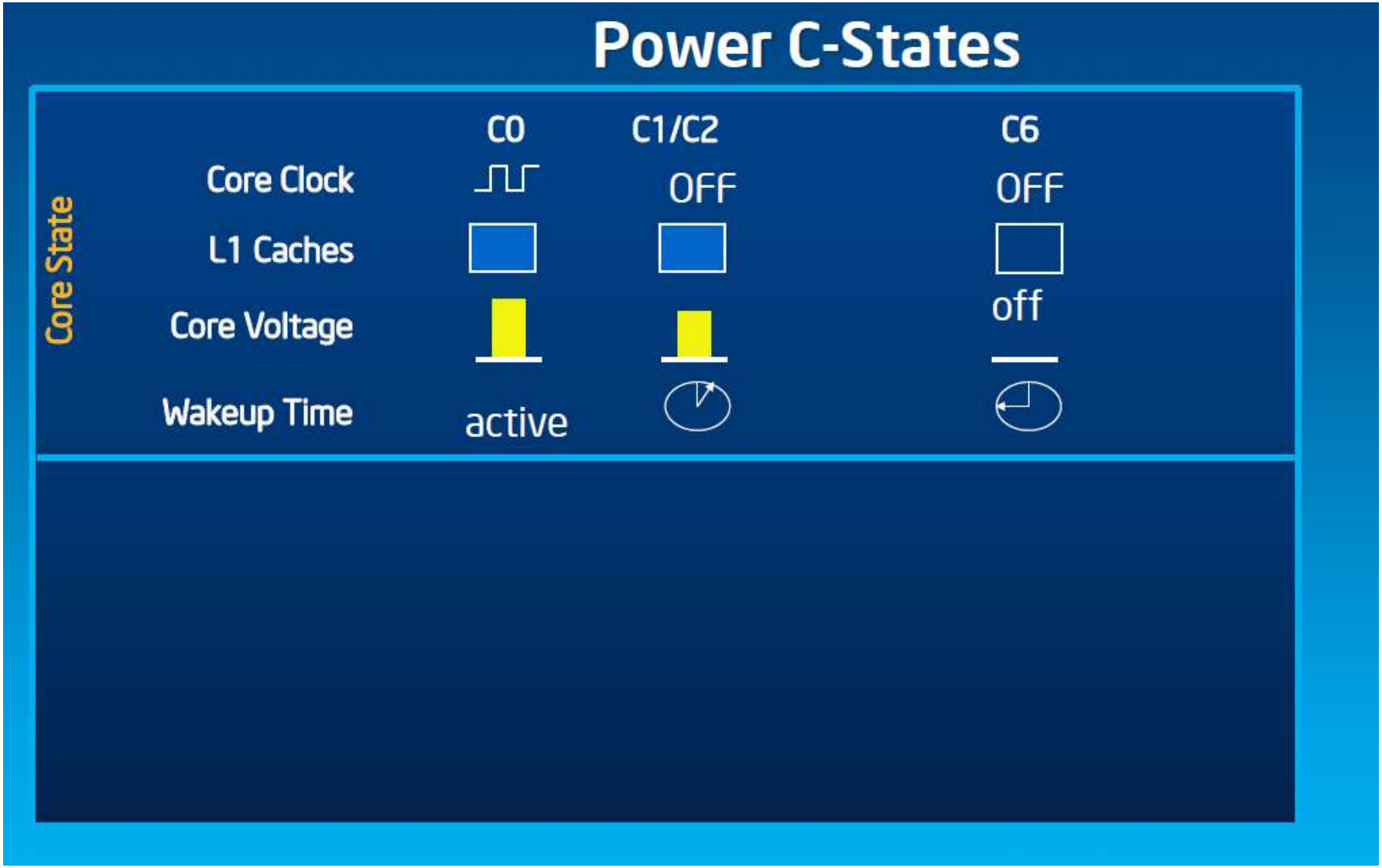
C6 state management in the Silvermont CPU

In contrast to the Bonnell and Saltwell CPUs the Silvermont CPU core does not support hyperthreading but it is module-based with two cores per module.

Now each core can enter into the Core C6 state independently.

In the Core C6 state L1 cashes associated with the core are flushed and the core becomes power gated, as indicated in the next slide.

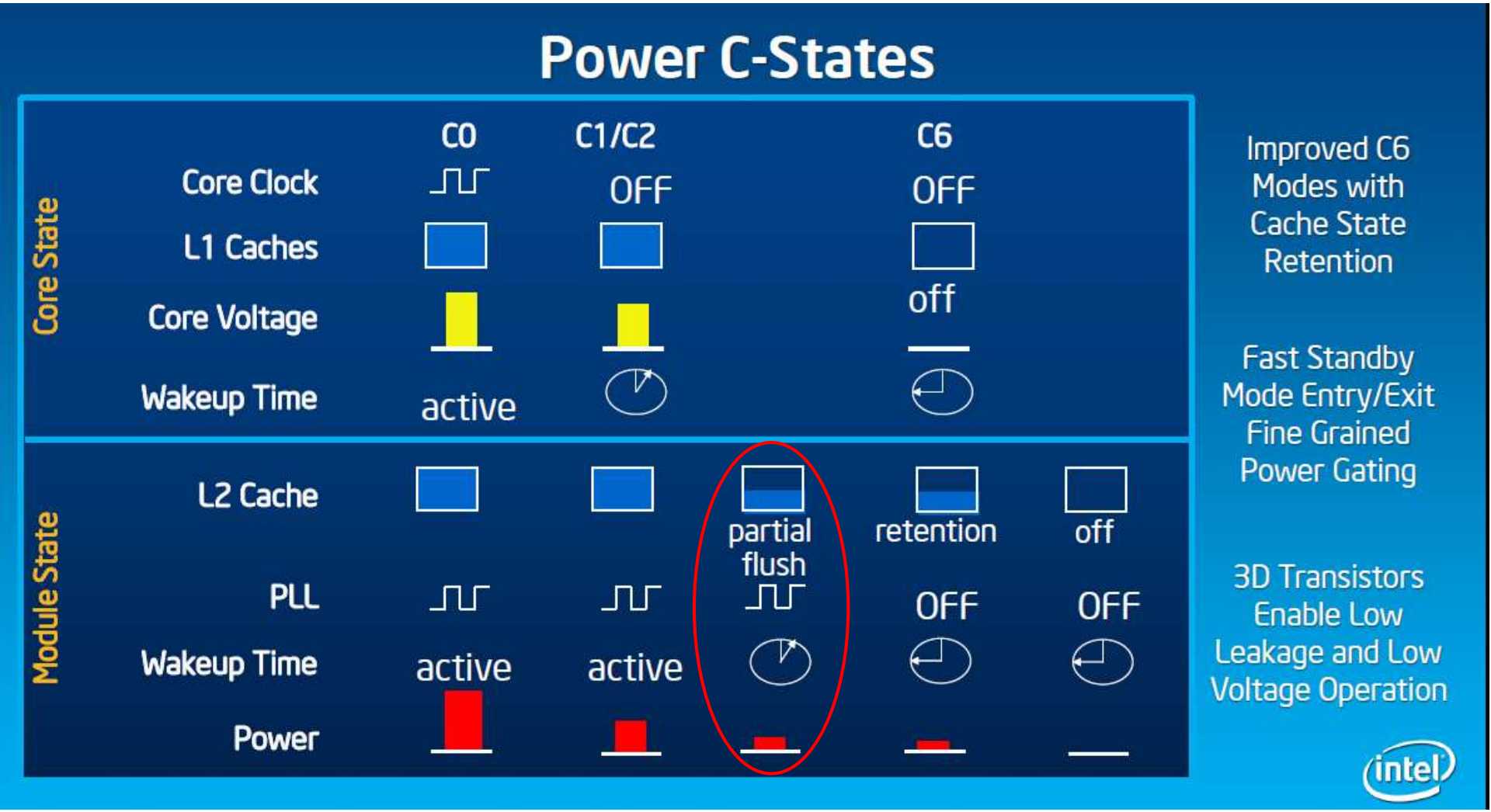
The Core C6 state of the Silvermont CPU [61]



Introducing a sub-state with partially flushing L2 and power gating flushed L2 sections [61]

To reduce power consumption, Intel introduced a sub-state allowing software-based control of the L2 cache size and power gate parts of L2, as indicated next.

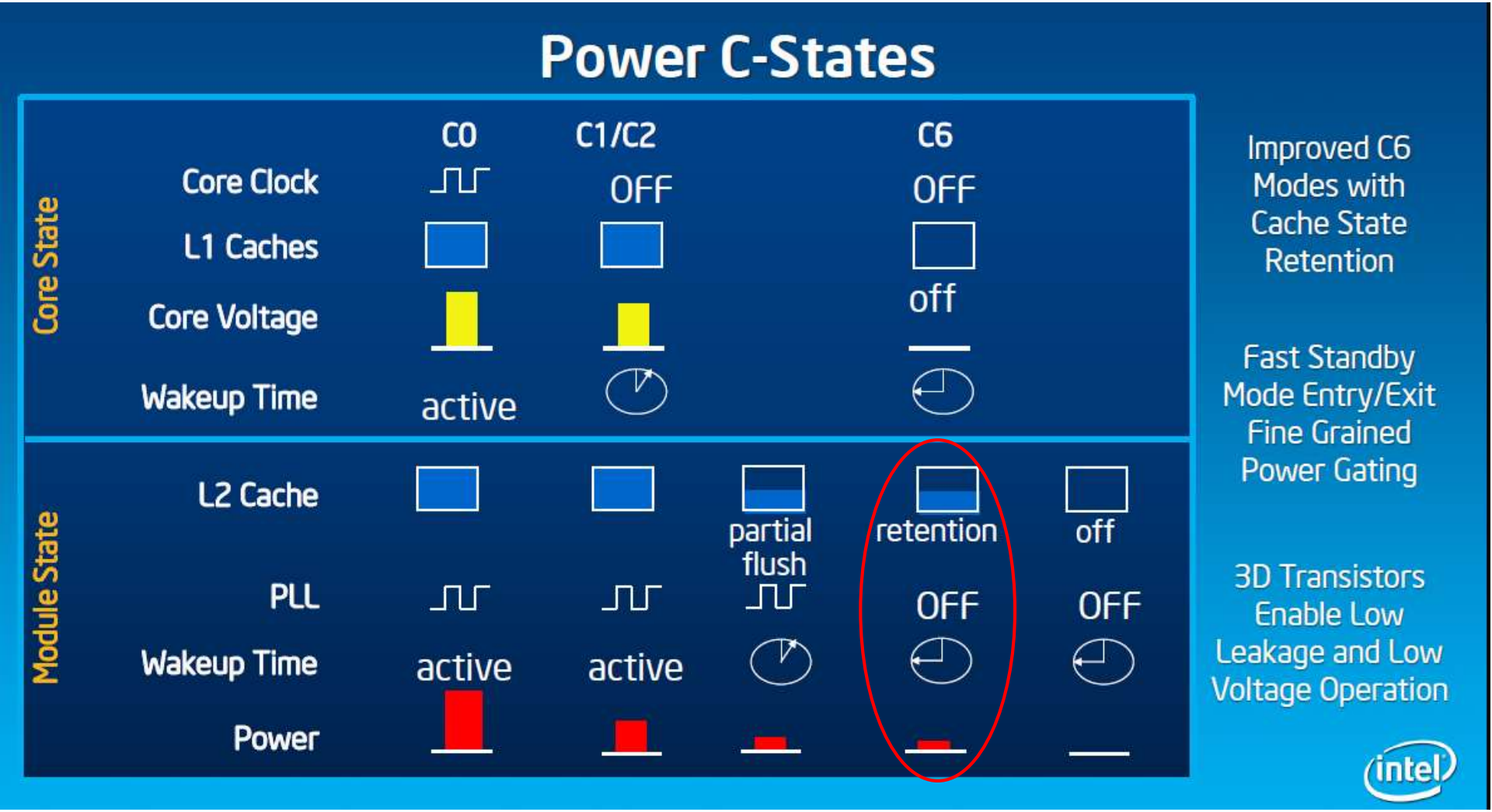
The sub-state with partially flushing L2 and power gating flushed L2 sections [61]



Introducing a Fast Standby mode sub-state with L2 retention and switching off the PLL [62]

To reduce power consumption, Intel introduced a further sub-state, the Fast Standby mode sub-state, allowing the partial retention of the L2 cache content in order to achieve a faster entry/exit, as compared to the C6 Module state with the state saved in an SRAM, as the next slide shows.

The sub-state with partially flushing L2 and power gating flushed L2 sections [61]

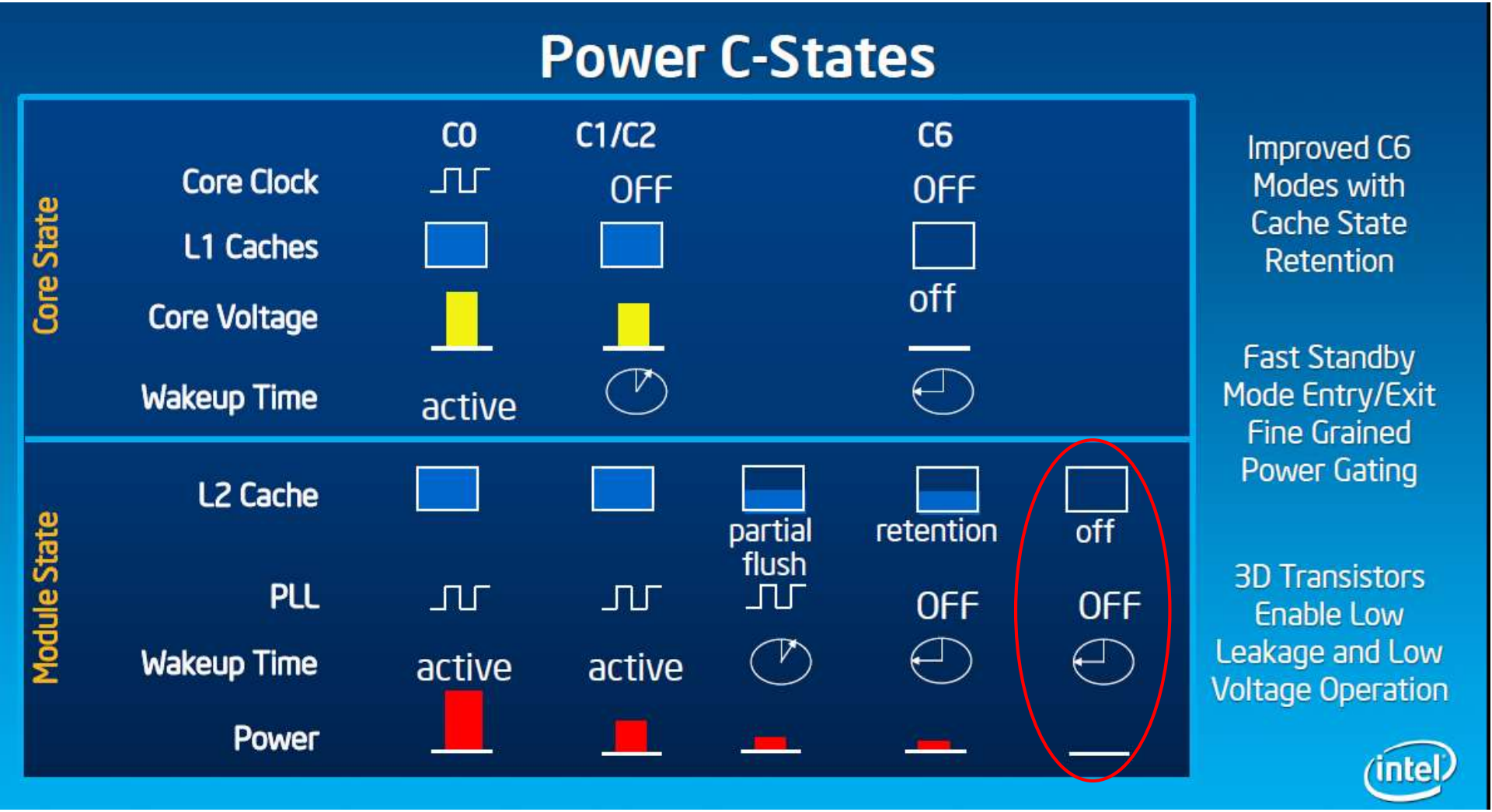


The Module C6 state

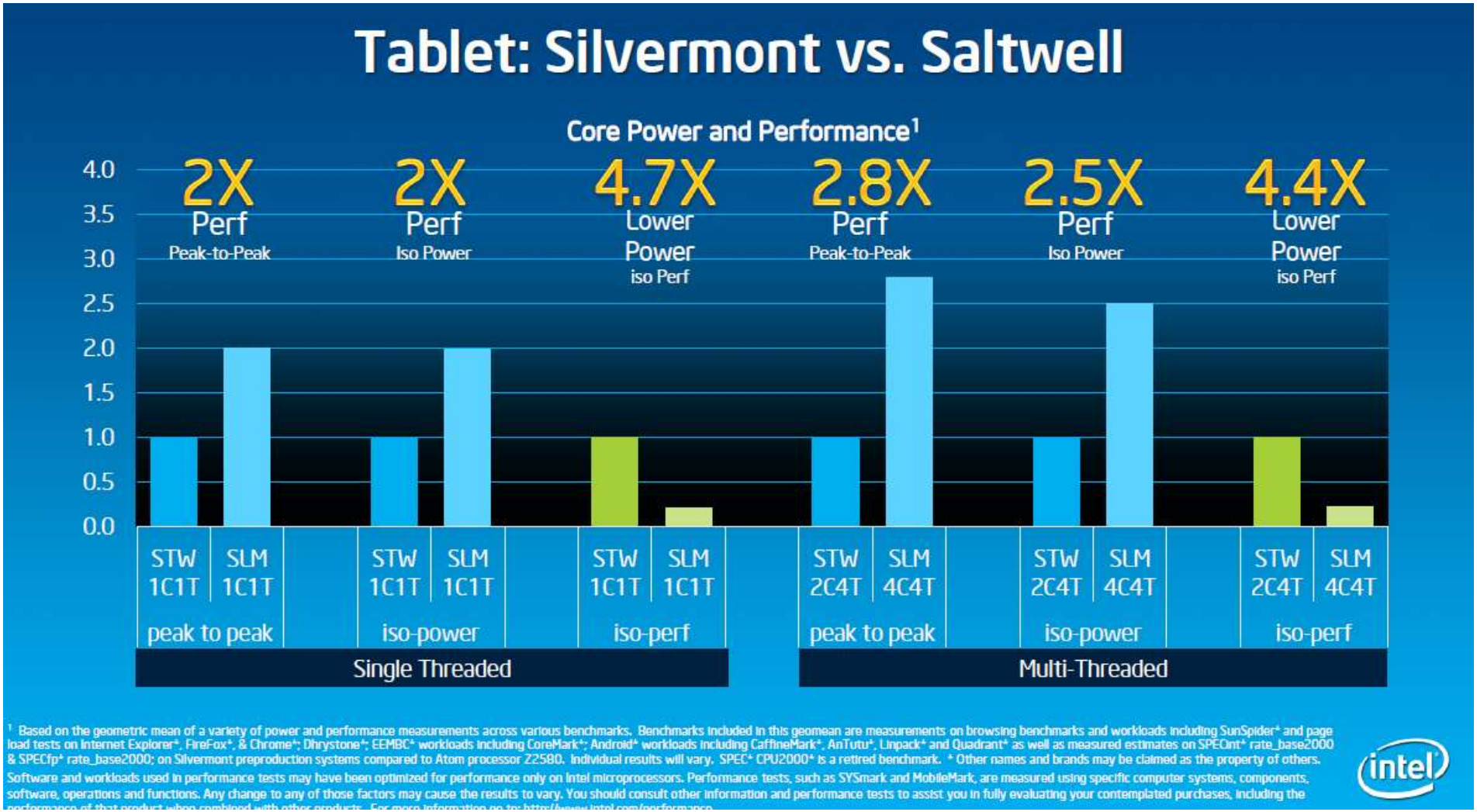
After both cores already entered the Core C6 state and the cores remain idle further on, the microcontroller can decide to let enter the module into the Module C6 state.

In the Module C6 state the L2 cache is flushed and the whole module becomes power gated.

The Module C6 state with the L2 cache flushed [61]

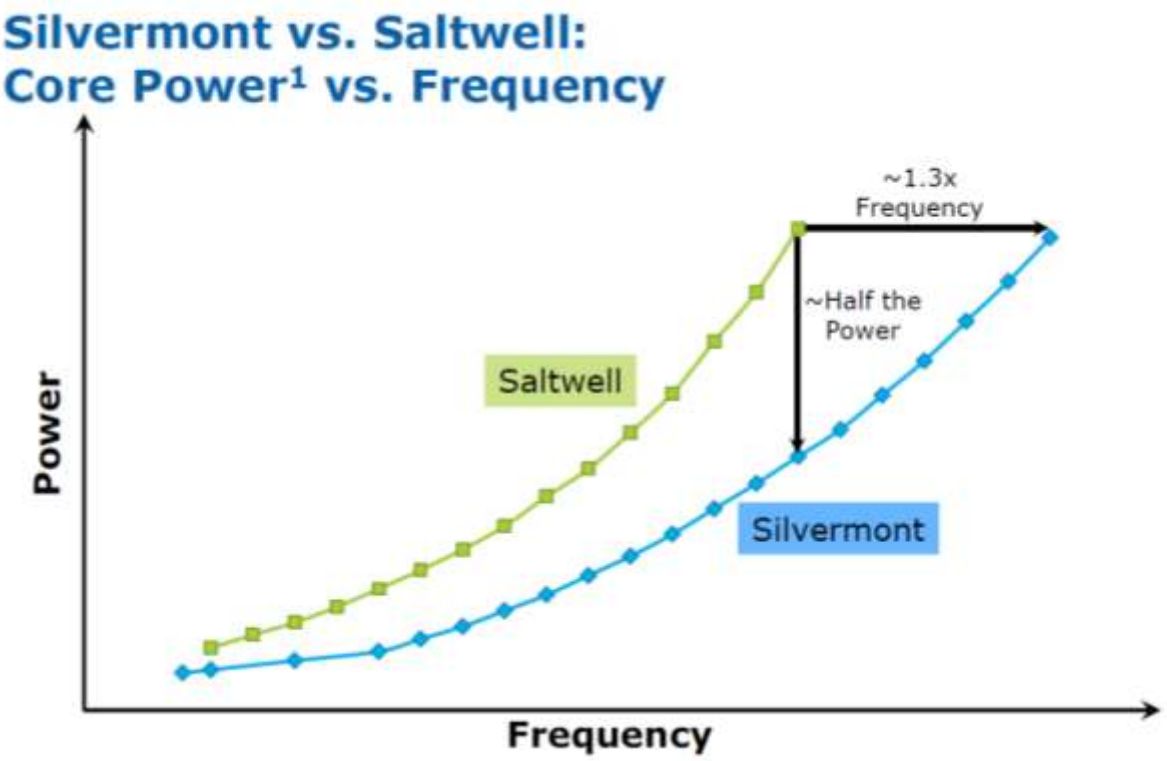


Silvermont's performance and power consumption vs. that of the Saltwell CPU [61]

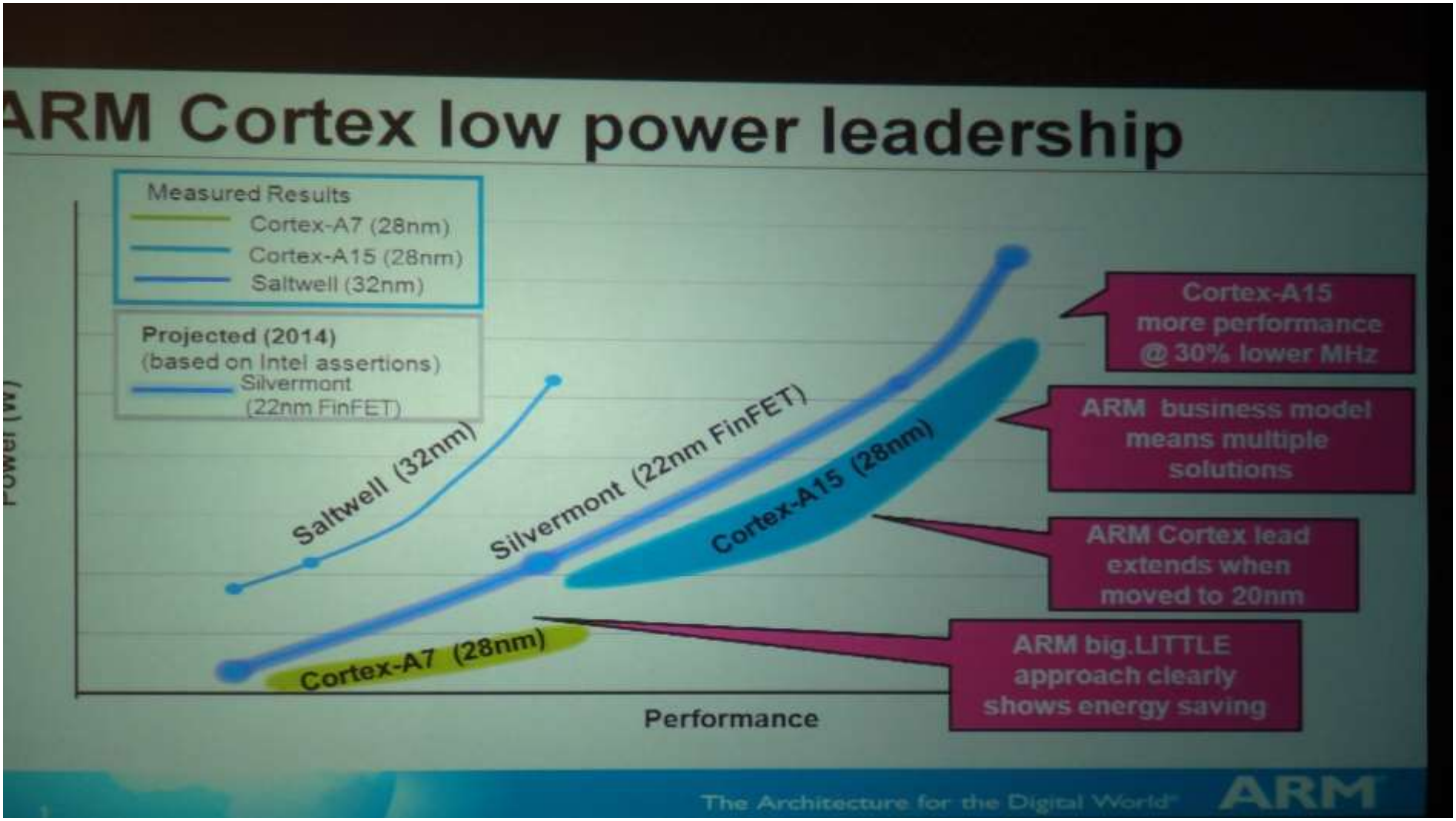


[1] Based on the geometric mean of a variety of power and performance measurements across various benchmarks. Benchmarks included in this geomean are measurements on browsing benchmarks and workloads including SunSpider* and page load tests on Internet Explorer*, FireFox*, & Chrome*; Dhrystone*; EEMBC* workloads including CoreMark*; Android* workloads including CaffineMark*, AnTutu*, Linpack* and Quadrant* as well as measured estimates on SPECint* rate_base2000 & SPECfp* rate_base2000; on Silvermont preproduction systems compared to Atom processor Z2580. Individual results will vary. SPEC* CPU2000* is a retired benchmark. * Other names and brands may be claimed as the property of others.
Software and workloads used in performance tests may have been optimized for performance only on Intel microprocessors. Performance tests, such as SYSmark and MobileMark, are measured using specific computer systems, components, software, operations and functions. Any change to any of those factors may cause the results to vary. You should consult other information and performance tests to assist you in fully evaluating your contemplated purchases, including the

Power-to-frequency curves of the Silvermont and Saltwell CPUs [143]



ARM's Figure about performance and power consumption of their and Intel's CPUs [138]



2.5 The 14 nm Airmont CPU core

2.5 The 14 nm Airmont CPU core

- Airmont is the 14 nm die shrink of Silvermont.

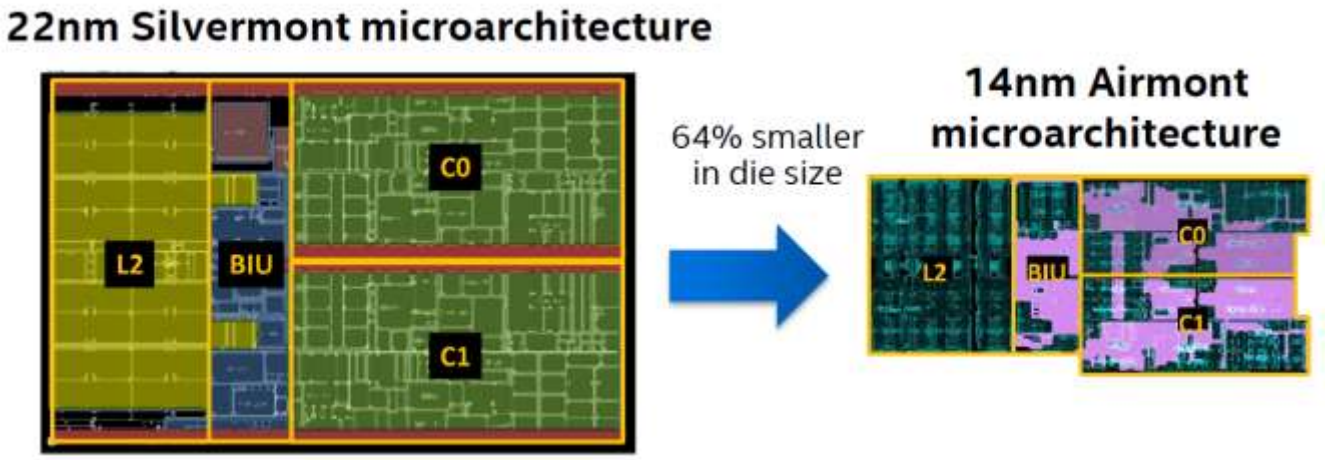


Figure: The 14 nm Airmont die as a shrink of the 22 nm Silvermont die [148]

- Launched in 03/2015.

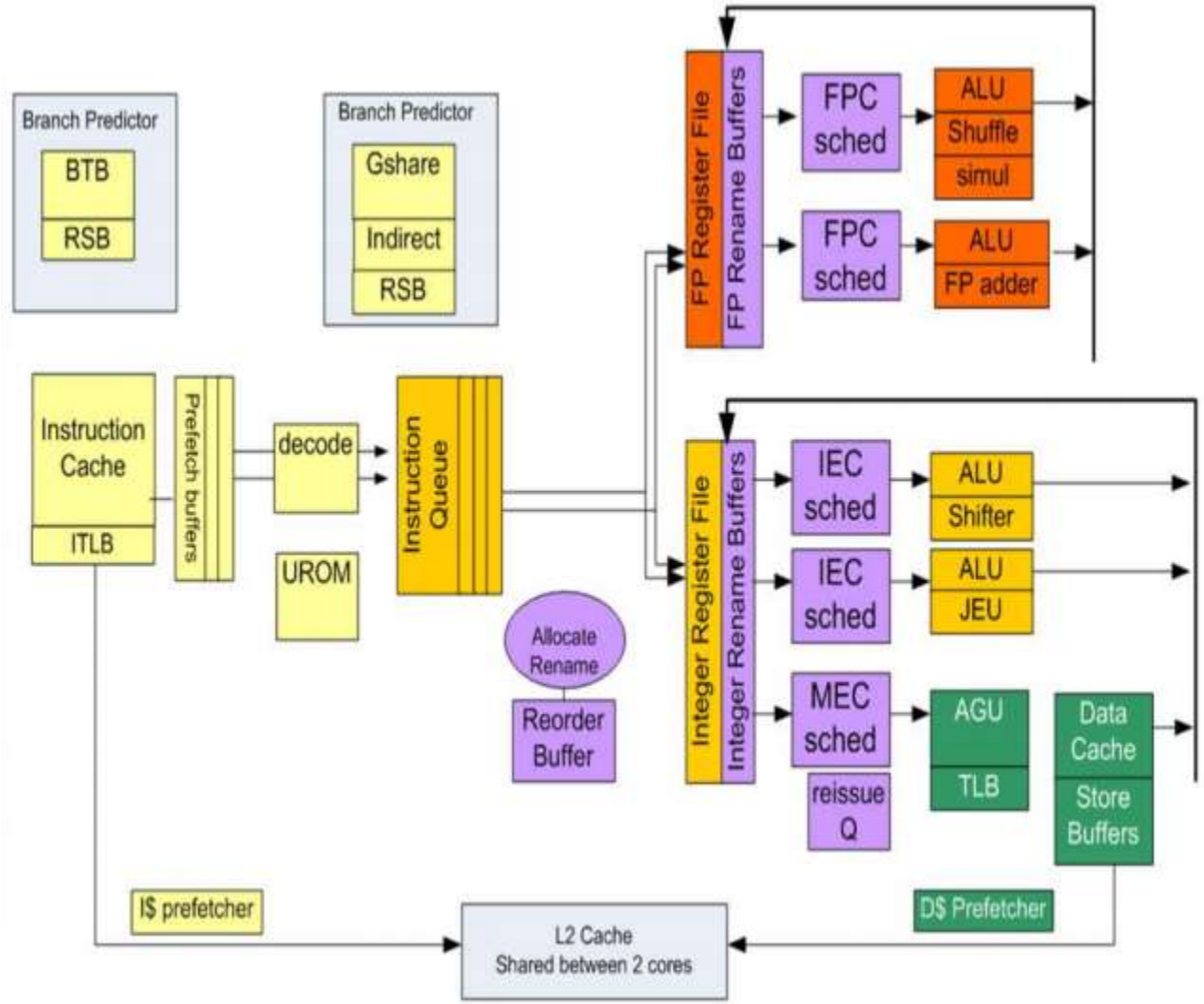
2.5 The 14 nm Airmont CPU core (2)

Key features of the microarchitecture of the Airmont CPU [149]

- The Airmont CPU has basically the same microarchitecture as the Silvermont CPU i.e. it is a two-way dual-core out-of-order superscalar with a shared L2 cache of 1 MB and it does not support HT.
- Nevertheless, it has a few enhancements vs. the Silvermont core in order to improve IPC, like
  - doubled branch predictor array size
  - larger ROB (Reorder Buffer) window
  - deeper reservation windows
  - deeper store buffer
  - more load misses in flight
- The Airmont CPU is used in the Cherry Trail SoC family aimed at tablets, as well as in the Braswell SoC line that is aimed at PCs (not discussed here).

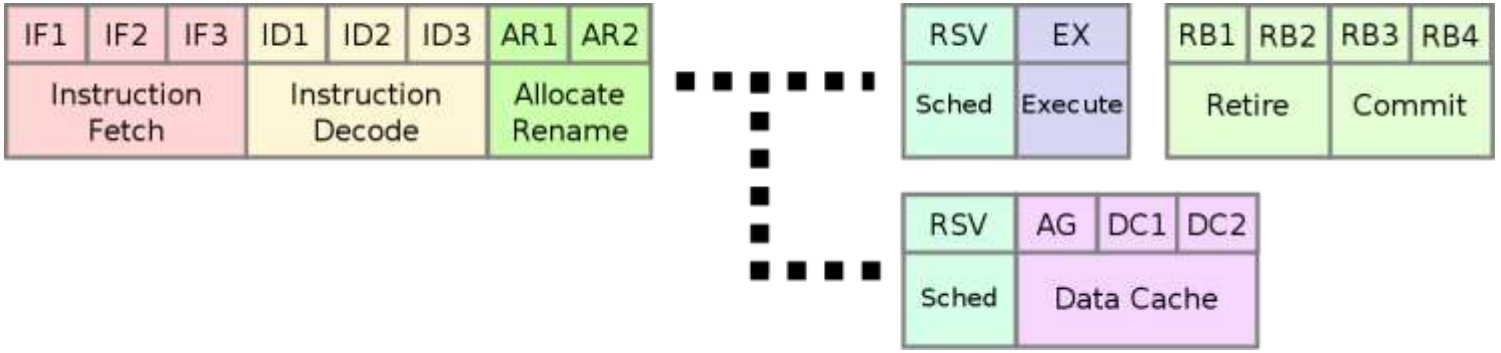
2.5 The 14 nm Airmont CPU core (3)

Microarchitecture of the Airmont CPU [150]



2.5 The 14 nm Airmont CPU core (4)

Pipeline stages of the Airmont CPU [150]



2.5 The 14 nm Airmont CPU core (5)

Airmont-based platforms [150]

Platform	Processor	Target
Braswell	Braswell	Entry-level PCs, Notebooks, Tablets
Cherry Trail	Cherry Trail	Lightweight tablets / High-end Smartphones
Riverton	Riverton	Smartphones (HSPA+, LTE Category 3, and TD-SCDMA)
Binghamton	Binghamton	Smartphones (3G only)

The Riverton and Binghampton platforms were internally planned by Intel, nevertheless subsequently cancelled.

2.6 The 14 nm Goldmont CPU

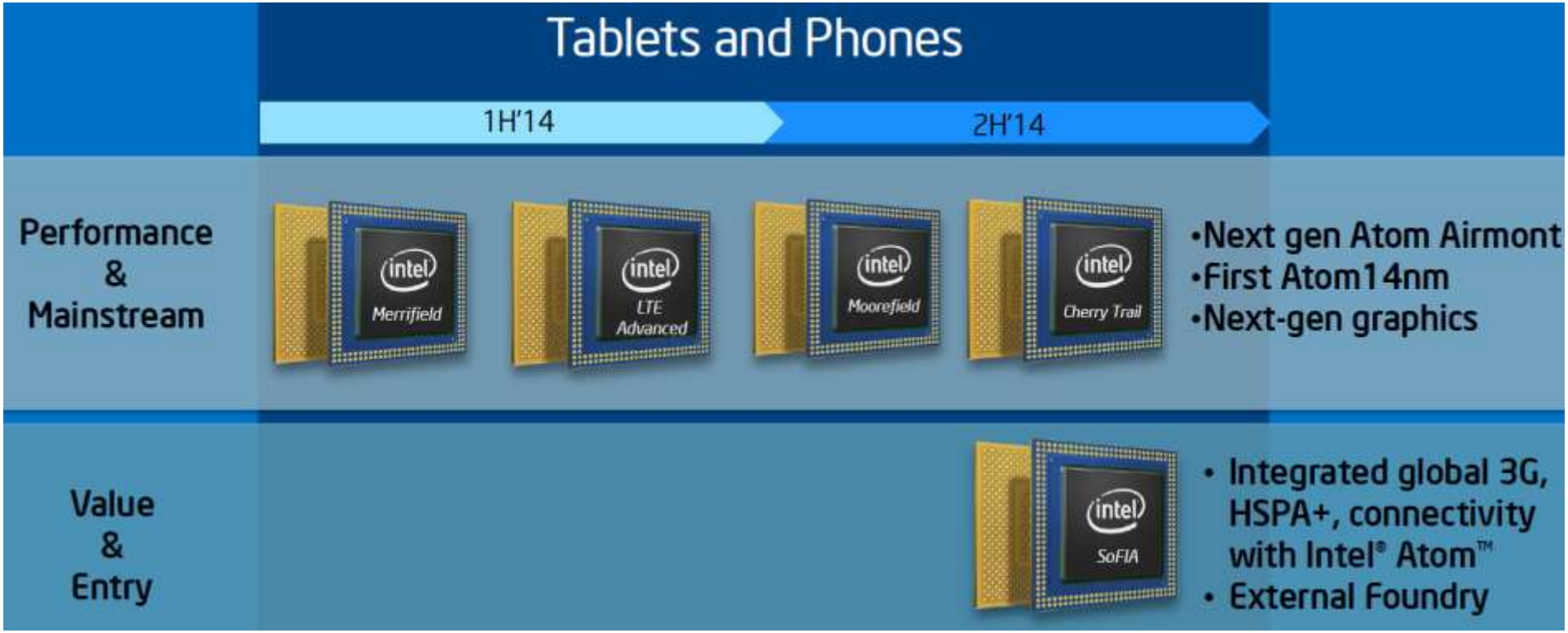
2.6 The 14 nm Goldmont CPU

Updating the Atom roadmap and announcing the Goldmont microarchitecture

At their Annual Investor Day in 11/2013 Intel updated their Atom roadmap by a large number of announcements including the Merrifield, Moorefield, Cherry Trail, Broxton and SoFIA processors, and the Goldmont microarchitecture, as seen in the next Figures, presumable to underline their strong commitment in the mobile market despite unsatisfactory market success.

2.6 The 14 nm Goldmont CPU (2)

Intel's Atom roadmap from 11/2013 of devices to be shipped in 2014 [151]



2.6 The 14 nm Goldmont CPU (3)

Intel's Atom roadmap from 11/2013 of devices to be shipped in 2015 [151]

As the roadmap shows Intel announced the Goldmont microarchitecture already in 11/2013. without giving any details.

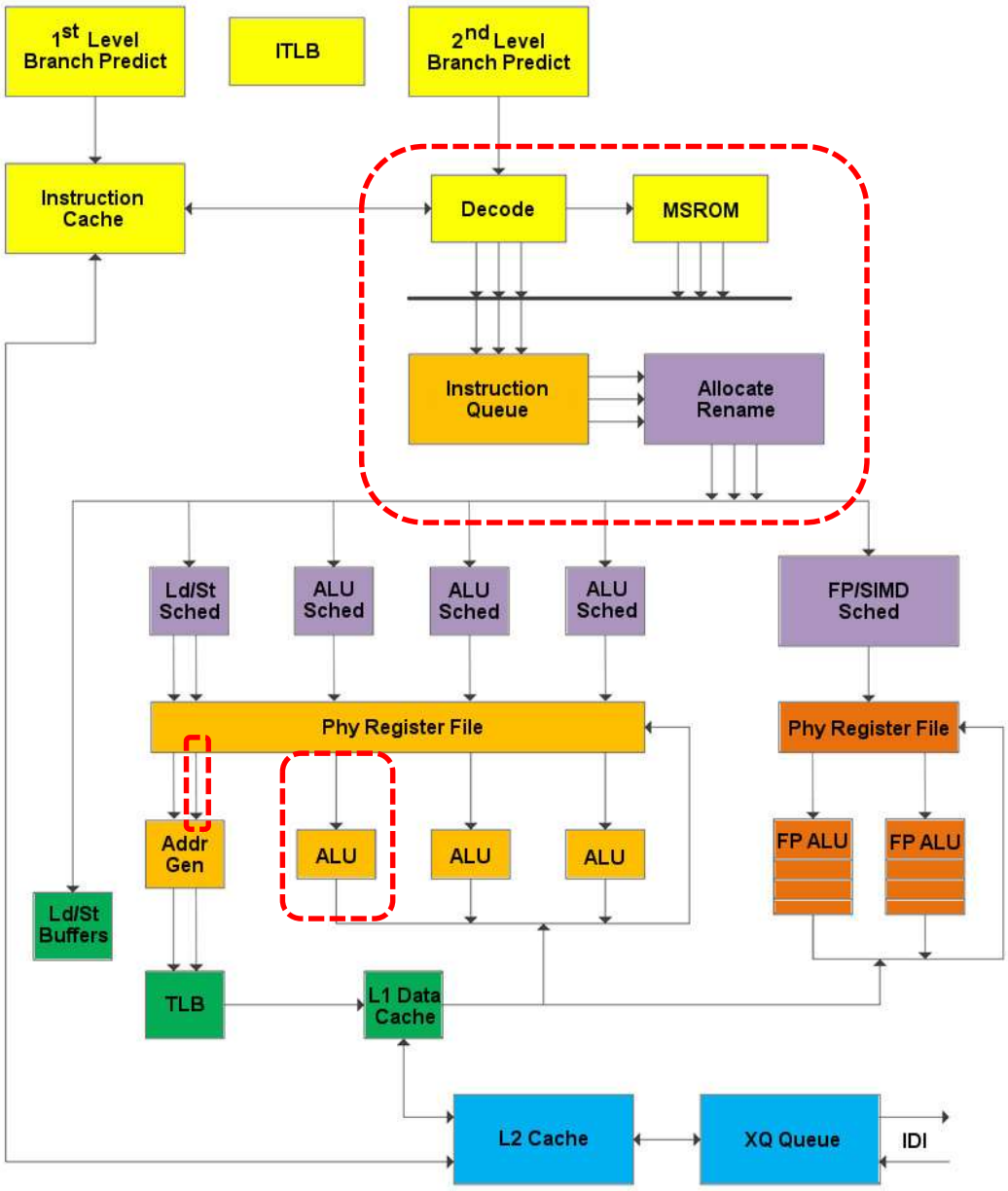
2.6 The 14 nm Goldmont CPU (4)

Key features of the Goldmont CPU microarchitecture

- Goldmont is a 3-wide out-of-order superscalar unlike the Airmont CPU that has a 2-wide out-of-order microarchitecture.
- It is fabricated on 14 nm technology.
- Launched: Q3/2016 (Apollo Lake processors)/08/2017 (Denverton processors)

2.6 The 14 nm Goldmont CPU (5)

Block diagram of the Goldmont CPU [144]



2.6 The 14 nm Goldmont CPU (6)

Main enhancements of the Goldmont microarchitecture vs. the Silvermont microarchitecture [144]

The Goldmont microarchitecture has an out-of-order execution engine with a 3-wide superscalar pipeline.

Specifically:

- The decoder can decode 3 instructions per cycle.
- The microcode sequencer can send 3 uops per cycle for allocation into the reservation stations.
- Retirement supports a peak rate of 3 per cycle.
- Enhancement in branch prediction which de-couples the fetch pipeline from the instruction decoder.
- Larger out-of-order execution window and buffers that enable deeper out-of-order execution across integer, FP/SIMD, and memory instruction types.
- Fully out-of-order memory execution and disambiguation.

  The Goldmont microarchitecture can execute one load and one store per cycle (compared to one load or one store per cycle in the Silvermont microarchitecture).
- Integer execution cluster in the Goldmont microarchitecture provides three pipelines and can execute up to three simple integer ALU operations per cycle.
- SIMD integer and floating-point instructions execute in a 128-bit wide engine.
- Throughput and latency of many instructions have improved, e.g. many SIMD instructions were doubled throughput;
- The Goldmont microarchitecture provides new instructions (see Table).

2.6 The 14 nm Goldmont CPU (7)

Main microarchitecture enhancements of the front-end of Goldmont CPU vs. the Silvermont CPU [144]

Feature	Goldmont Microarchitecture	Silvermont Microarchitecture
Number of Decoders	3	2
Max Throughput of Decoders	20 Bytes per cycle	16 Bytes per cycle
Fetch and Icache Pipeline	Decoupled	Coupled
ITLB	48 entries, large page support	48 entries
Branch Mispredict Penalty	12 cycles	10 cycles
L2 Predecode Cache	16K	NA

2.6 The 14 nm Goldmont CPU (8)

New instructions introduced along with the Goldmont microarchitecture [152]

SGX1 - Software Guard Extensions, Version 1
RDSEED - Generates 16, 32 or 64 bit random numbers seeds (NIST SP 800-90B & NIST SP 800-90C)
SMAP - Supervisor Mode Access Prevention
MPX - Memory Protection Extensions
XSAVEC - Save processor extended states with compaction to memory
XSAVES - Save processor supervisor-mode extended states to memory.
CLFLUSHOPT - Flush & Invalidates memory operand and its associated cache line (All L1/L2/L3 etc..)
SHA - Hardware acceleration for SHA hashing operations

2.6 The 14 nm Goldmont CPU (9)

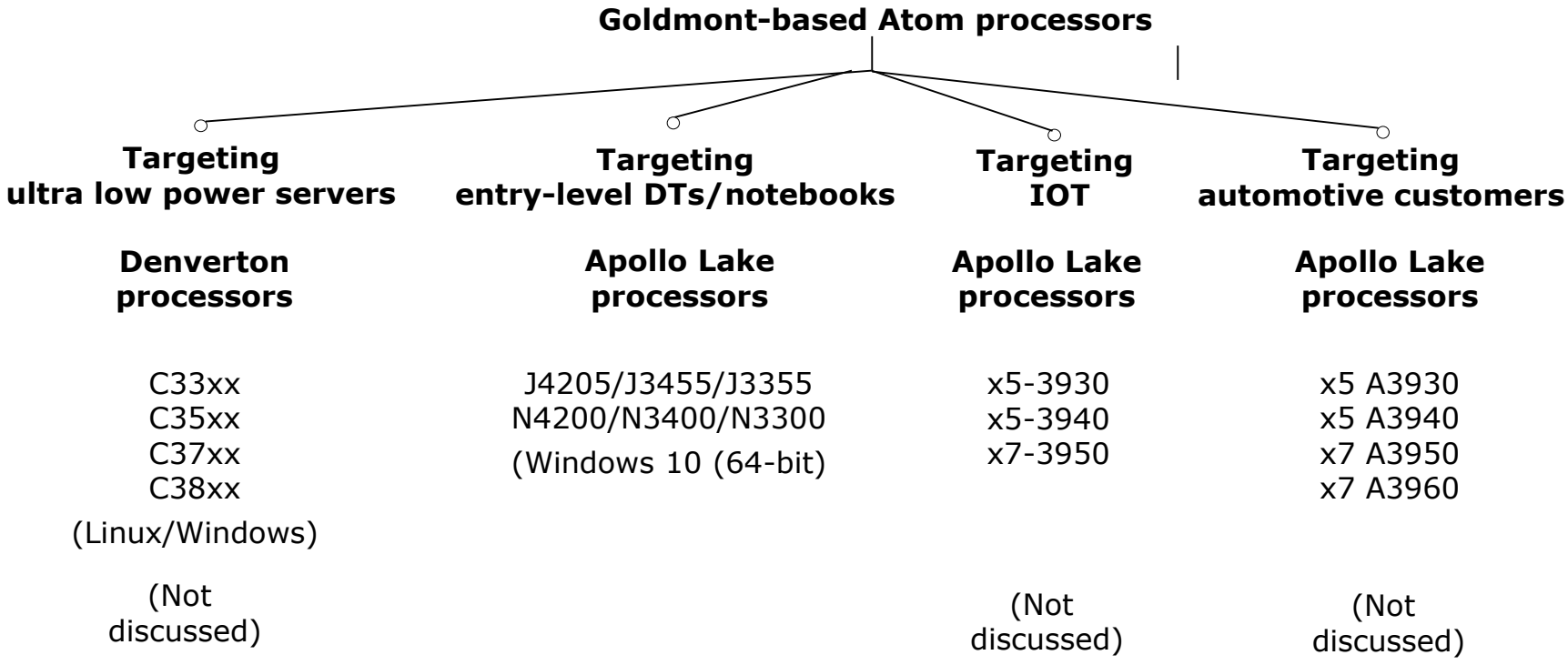
Goldmont-based platforms [152]

Platform	Processor	Target
	Apollo Lake	Entry-level PCs, tablets
	Denverton	Ultra-low power servers, networking, storage, and IoT
Willow Trail	Willow Trail	~~Lightweight Tablets & high-end smartphones~~
Morganfield	Broxton	~~Smartphones~~

The Morganfield platform with their Broxton SOC and the Willow Trail platform were internally planned by Intel, nevertheless subsequently cancelled when Intel has withdrawn from the smartphone and the tablet segment in 2016.

2.6 The 14 nm Goldmont CPU (10)

Goldmont-based Atom processors [152]



2.7 The 14 nm Goldmont Plus CPU

2.7 The 14 nm Goldmont Plus CPU

Its key features

- Goldmont Plus is a 3-wide out-of-order superscalar with a 4-wide retire unlike the Goldmont CPU that has a 3-wide retire.
- It is manufactured on 14 nm technology.
- Launched: 12/2017

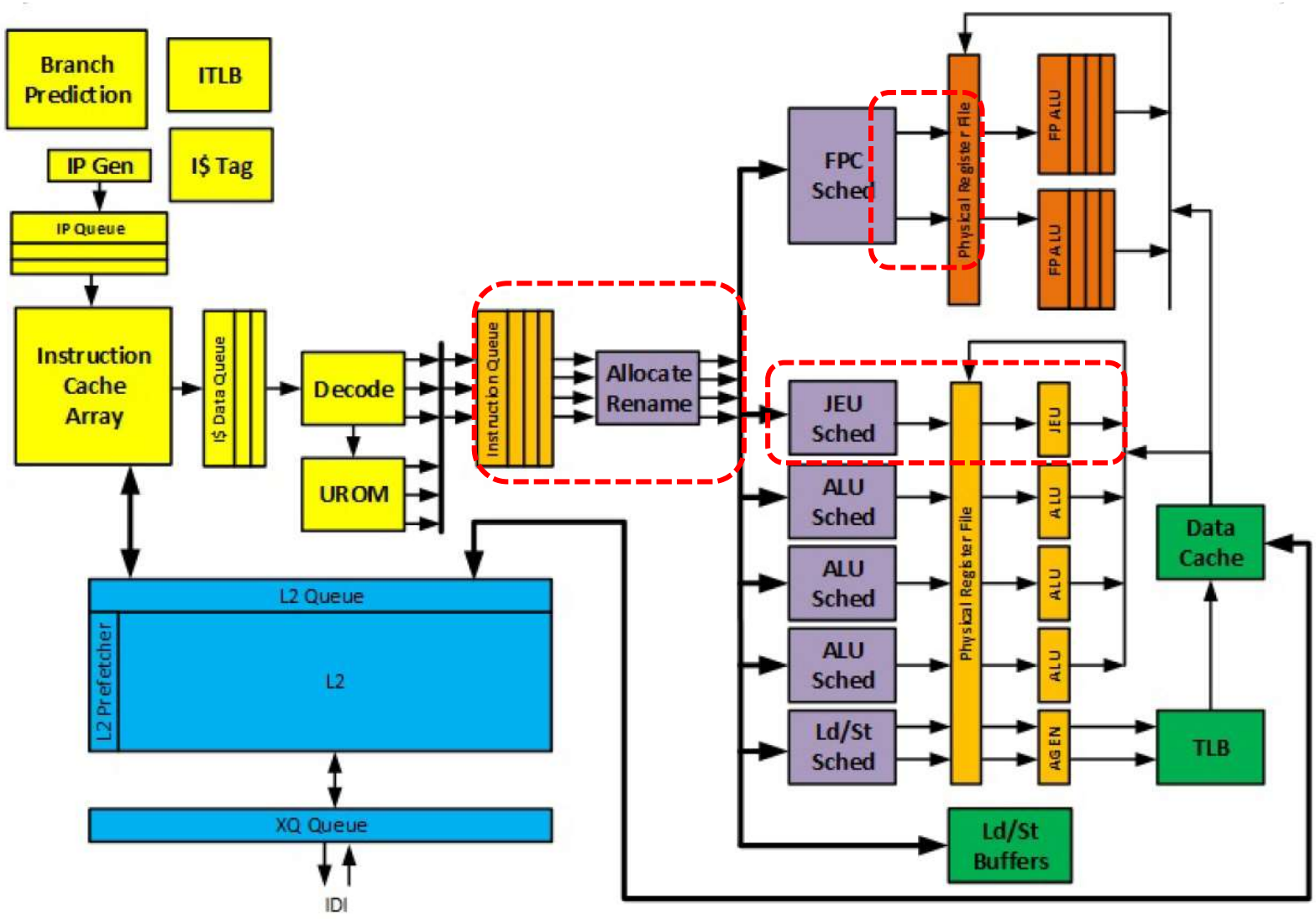
2.7 The 14 nm Goldmont Plus CPU (2)

Main enhancements of the Goldmont Plus microarchitecture vs. the Goldmont microarchitecture [144]

- Widens previous generation Goldmont processor back-end pipeline to 4-wide allocation to 4-wide retire, while maintaining 3-wide fetch and decode pipeline.
- Enhanced branch prediction unit.
- 64KB shared second level pre-decode cache (16KB in Goldmont microarchitecture).
- Larger reservation station and ROB entries to support large out-of-order window.
- Wider integer execution unit.
- New dedicated JEU port with support for faster branch redirection.
- Radix-1024 floating point divider for fast scalar/packed single, double and extended precision floating point divides.
- Improved AES-NI instruction latency and throughput.
- Larger load and store buffers. Improved store-to-load forwarding latency store data from register.
- Modular system design with four cores sharing up to 4MB L2 cache.
- Support for Read Processor ID (RDP) new instruction.

2.7 The 14 nm Goldmont Plus CPU (3)

Block diagram of the Goldmont Plus CPU [144]



2.7 The 14 nm Goldmont Plus CPU (4)

New instructions introduced along with the Goldmont Plus microarchitecture [153]

SGX1 - Software Guard Extensions, Version 1
UMIP - User-mode instruction prevention
PTWRITE - Trace logger write user data
RDPID - Read Processor ID

2.7 The 14 nm Goldmont Plus CPU (5)

Microarchitecture enhancements of the front-end of Goldmont Plus CPU vs. the Goldmont CPU [153]

Feature	Goldmont Plus Microarchitecture	Goldmont Microarchitecture
Number of Decoders	3	3
Max. Throughput Decoders	20 Bytes per cycle	20 Bytes per cycle
Fetch and Icache Pipeline	Decoupled	Decoupled
ITLB	48 entries, large page support	48 entries, large page support
2nd Level ITLB	Shared with DTLB	
Branch Mispredict Penalty	13 cycles (12 cycles for certain Jcc)	12 cycles
L2 Predecode Cache	64K	16K

2.7 The 14 nm Goldmont Plus CPU (6)

Goldmont Plus-based Atom processors [153]

Goldmont Plus-based Atom processors

Targeting
entry-level DTs/notebooks

Gemini Lake
processors

Pentium Silver J5005/N5000
Celeron J4105/J4005
N4100/N4000
(Windows 10)

3. Atom-based platforms targeting entry level desktops and notebooks

- 3.1 Introduction and overview
- 3.2 The Diamondville platform
- 3.3 The Pine Trail platform
- 3.4 The Cedar Trail-D/M platform
- 3.5 The Bay Trail D/M platforms
- 3.6 The Braswell platform
- 3.7 The Apollo Lake platform
- 3.8 The Gemini Lake platform

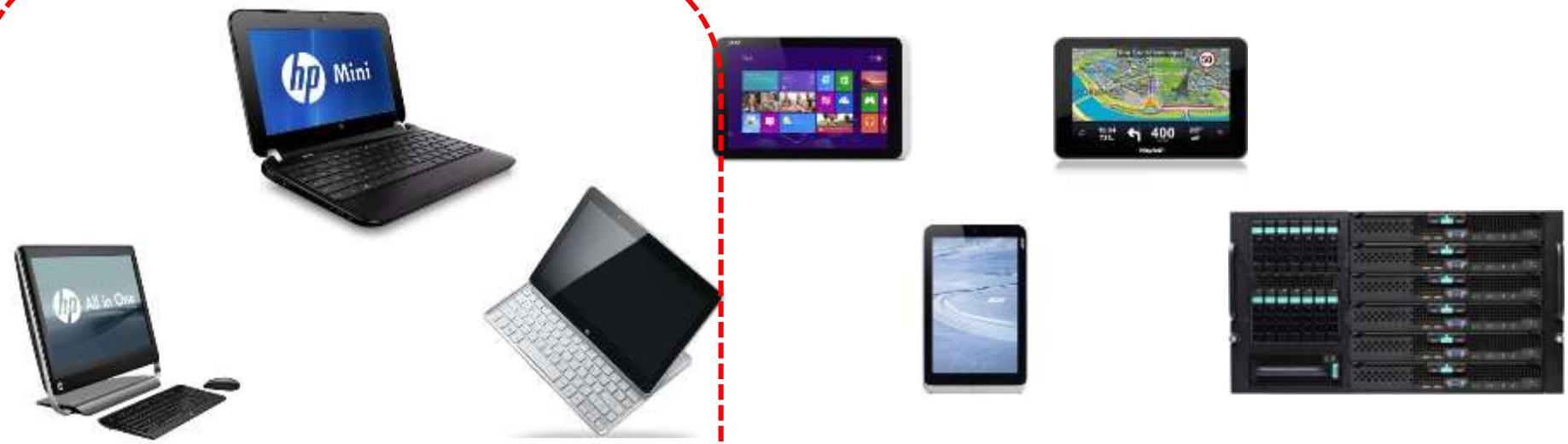
3.1 Introduction and overview

3.1 Introduction to Atom-based platforms targeting entry level desktops and netbooks (1)

3.1 Introduction and overview

Presentation of Intel's Atom-based product series in these slides

A t o m b a s e d p r o d u c t s e r i e s



Entry-level desktops	Notebooks (Subnotebooks)	Convertibles	Tablets	Smartphones	Embedded	Microservers
D/J-Series *(First D, then J)*	***N-Series***		***Z-Series*** *Zx6xx/x7xx*	***Z-Series*** *Zx4xx/x5xx*	***E/CE-Series***	***S-Series***
Section 3			*Section 4*	*Section 5*	*Not discussed*	*Not discussed*

3.1 Introduction to Atom-based platforms targeting entry level desktops and netbooks (2)

Intel's slide introducing entry-level DTs (called nettops) and netbooks at the IDF 2008 [9]

Key features of entry-level desktops (called nettops) and netbooks

- Internet connectivity is a key usage
- Platform is optimized for low BOM cost (Bill Of Material cost)
- Running under Windows and Linux

3.1 Introduction to Atom-based platforms targeting entry level desktops and netbooks (3)

Overview of Atom-based platforms targeting entry-level desktops and notebooks

Atom-based platforms targeting entry-level desktops and notebooks

	Diamondville	**Pine Trail**	**Cedar Trail-D/M**	**Bay Trail-D/M**	**Braswell**	**Apollo Lake**	**Gemini Lake**
Intro.	06/2008	01/2010	Q3/2011	10/2013	04/2015	2017	12/2017
Processor	Diamondville	Pineview	Cedarview-D/M	Valleyview-D/M	Braswell	Apollo Lake	Gemini Lake
Technology CPU	45 nm Bonnell	45 nm Bonnell	32 nm Saltwell	22 nm Silvermont	14 nm Airmont	14 nm Goldmont	14 nm Goldmont Plus
No. of cores	1C/2C	1C/2C	1C/2C	2C/4C	2C/4C	2C/4C	2C/4C
Chipset	945GC + ICH7 9N40 + ICH9M 945GSE + ICH7M	NM10	NM10	SOC	SOC	SOC	SOC
	(Section 3.2)	*(Section 3.3)*	*(Section 3.4)*	*(Section 3.5)*	*(Section 3.6)*	*(Section 3.7)*	*(Section 3.8)*

Main features of Intel's Atom-based platforms targeting entry level desktops and notebooks-1

	Diamondville				Pine Trail			
Launched	06/2008				01/2010			
Focus	Entry-level desktops (Nettops)		Notebooks/Sub notebooks (Netbooks)		Entry-level desktops (Nettops)		Notebooks/Sub notebooks (Netbooks)	
Processor	Diamondville				Pineview			
Models	330	230	N280	N270	D525/0510	D425/0410	N570/N550	N475-N435
Technology	45nm				45nm			
Die size	2x26mm^2	26 mm^2			87 mm^2	66 mm^2	87 mm^2	66 mm^2
No. of trans.	2x47 mtrs	47 mtrs			176 mtrs	123 mtrs	176 mtrs	123 mtrs
Micro-arch.	Bonnell				Bonnell			
32/64-bit	64-bit		32-bit		64-bit			
1C/2C	2C	1C	1C		2C	1C	2C	1C
HT	HT				HT			
fc [GHz]	1.6 GHz	1.6 GHz	1.67 GHz	1.6 GHz	1.80/1.67	1.8/1.66	1.66/1.50	1.83-1.33
L2	2x512 kB	512 kB			2x512 kB	512 kB	2x512 kB	512 kB
No. of mem.ch.	Single channel (64-bit)		Single channel (32-bit)		Single channel (64-bit)			
Memory	DDR2-533		DDR2-667	DDR2-533	DDR3-800 (only D525/D425) else DDR2-800/667		DDR3-667 (except N450/N470) DDR2-667	
GPU	GMA 950 in the north bridge		X4500 MHD in the north bridge	GMA 950	GMA 3150 on the processor die			
DX	DX 9.0c		DX 10	DX 9.0c	DX 9.0c			
Dixplay output	TVOut, CRT, LVDS, SDVO				VGA, LVDS			
GPU clock	400-133 MHz		533/400 MHz	166 MHz	400 MHz		200 MHz	
Proc. TDP	8 W	4 W	2.5 W		13 W	10 W	8.5 W	6.5-5 W
FSB	533/400 MT/s		667 MT/s	533 MT/s	DMI (2 lanes, each 500 MB/s in each direction)			
Socket	BGA 437				BGA 559			
Chipset	945GC[1] (Lakeport) + ICH7U		GN40 + ICH9M	945GSE[2] + ICH7M	NM10 (Tiger Point)			
OS	Windows XP Home Linux				Windows XP Home/Windows Vista/Windows 7 Moblin (Intel's Linux version)			

MID: Mobile Internet Devices, typically tablets
UMPC: Ultra Mobile PC: typically tablets

[1]: TDP: 22,2 W
[2]: TDP: 11,8 W

Main features of Intel's Atom-based platforms targeting entry level desktops and notebooks -2

	Cedar Trail-D/M		Bay Trail - D	Bay Trail - M
Launched	Q3/2011		Q3 2013	Q3 2013
Focus	Entry Level DTs	Notebooks	Entry level DTs All-in-One DTs (AIO)	Notebooks/"2 in 1's
Processor	Cedarview – D/ M		Valleyview - D	Valleyview - M
Models	D2701-D2500	N2800-N2100	J2900/J2850/J1900/ J18xx/J1700	N35xx/N29xx/N28xx
Technology	32nm		22nm	
Die size				
No. of trans.				
Micro-arch.	Saltwell		Silvermont (Out-Of-Order)	
32/64-bit	64-bit		64-bit	
No. of cores	2C	1C/2C	2C/4C	
HT	HT (except D2500)		no	
fc [GHz]	2.13-1.86	1.86/1.6	Up to 2.41 GHz	Up to 2.16 GHz
L2	2x512 kB		2x1 MB for 4 cores/1 MB for one core	
No. of mem.ch.	Single channel (64-bit)		Dual channels (64-bit)	
Memory up to	DDR3-1066/800		DDR3L-1333	DDR3L-1066/1333
GPU	GMA 3650/GMA 3600 (Power VR SGX 545)		Gen. 7	
DX	DX 9.0C		DX 11	
GPU clock (base)		640/400 MHz	688 MHz	313 MHz
ISP	--		ISP	
Display output	VGA, eDP, DP1.1, HDMI 1.3a, LVDS		VGA, DP 1.2, HDMI 1.4a, MIPI-DSI	
Proc. TDP	10 W	6.5/3.5 W	≤ 10 W	≤7.5 W
FSB	DMI x4 (Actually 4/2 PCIe lanes in both dir.)	DMI x2	—	
Socket	BGA 559		FCBGA1170	
Chipset	NM 10		no, SoC	
OS	Windows XP Windows 7 MeeGo 1.2 Windows Embedded CE		Windows 7 Windows 8 non CS Linux	Windows 7 Windows 8 non CS Windows 8 (32-bit)

Main features of Intel's Atom-based platforms targeting entry level desktops and notebooks -3

	Braswell		Apollo Lake	
Launched	Q1/2015		Q3/2016	
Focus	Entry-level DTs	Notebooks/Convertibles	Entry level DTs	Notebooks/Convertibles
Processor	Braswell		Apollo Lake	
Models	J3710/J3160/J3060	N3710/N3700/ N3160/N3150/N30xx	J4205/J3455/J3355	N4200/N3400/N3300
Technology	14 nm		14 nm	
Die size				
No. of trans.				
Micro-arch.	Airmont		Goldmont	
32/64-bit	64-bit		64-bit	
No. of cores	2C/4C		2C/4C	
HT	no		no	
fc [GHz]	Up to 1.6 GHz		Up to 2.0 GHz	1.1 GHz
L2	1 MB/2C		1 MB/2C	
No. of mem.ch.	Dual channels (64-bit)		Dual channel (64-bit)	
Memory up to	DDR3L-1600		LPDDR4-2400	
GPU	Gen. 8 LP		Gen. 9 LP HD 505	
DX	DX 11.1		DX 12.0	
GPU clock (base)	Up to 400 MHz		250 MHz	200 MHz
ISP	ISP		ISP	
Display output	eDP, DP, HDMI		eDP, DP, HDMI, MIPI-DSI	
Proc. TDP	≤ 6.5 W	≤ 6 W	10 W	6 W
FSB	--		--	
Socket	FCBGA1170		FCBGA1296	
Chipset	no, SoC		No, SOC	
OS	Windows 7 (32/64-bit) Windows 8.1 (64-bit) Windows 10 (64-bit)		Windows 10 (64-bit)	

Main features of Intel's Atom-based platforms targeting entry level desktops and notebooks -4

	Apollo Lake		Gemini Lake	
Launched	Q3/2016		12/2016	
Focus	Entry level DTs	Notebooks/Convertibles	Entry level DTs	Notebooks/Convertibles
Processor	Apollo Lake		Gemini Lake	
Models	J4205/J3455/J3355	N4200/N3400/N3300	J5005/J4105/J4005	N5000/N4100/N4000
Technology	14 nm		14 nm	
Die size				
No. of trans.				
Micro-arch.	Goldmont		Goldmont Plus	
32/64-bit	64-bit		64-bit	
No. of cores	2C/4C		2C/4C	
HT	no		no	
fc [GHz]	Up to 2.0 GHz	1.1 GHz	Up to 2.0 GHz	1.1 GHz
L2	1 MB/2 cores		1 MB/2 cores	
No. of mem.ch.	Dual channels		Dual channels	
Memory up to	LPDDR4-2400		LPDDR4-2400	
GPU	Gen. 9 LP HD 505		Gen. 9 LP UHD 605/600	
DX	DX 12.0		DX 12.0	
GPU clock (base)	250 MHz	200 MHz	250 MHz	200 MHz
ISP	ISP		ISP	
Display output	eDP, DP, HDMI, MIPI-DSI		eDP, DP, HDMI, MIPI-DSI	
Proc. TDP	10 W	6 W	10 W	6 W
FSB	--		--	
Socket	FCBGA1296		FCBGA1090	
Chipset	No, SOC		No, SOC	
OS	Windows 10 (64-bit)		Windows 10 (64-bit)	

3.2 The Diamondville platform

3.2 The Diamondville platform

Introducing the first Atom processor-based platform and launching first products

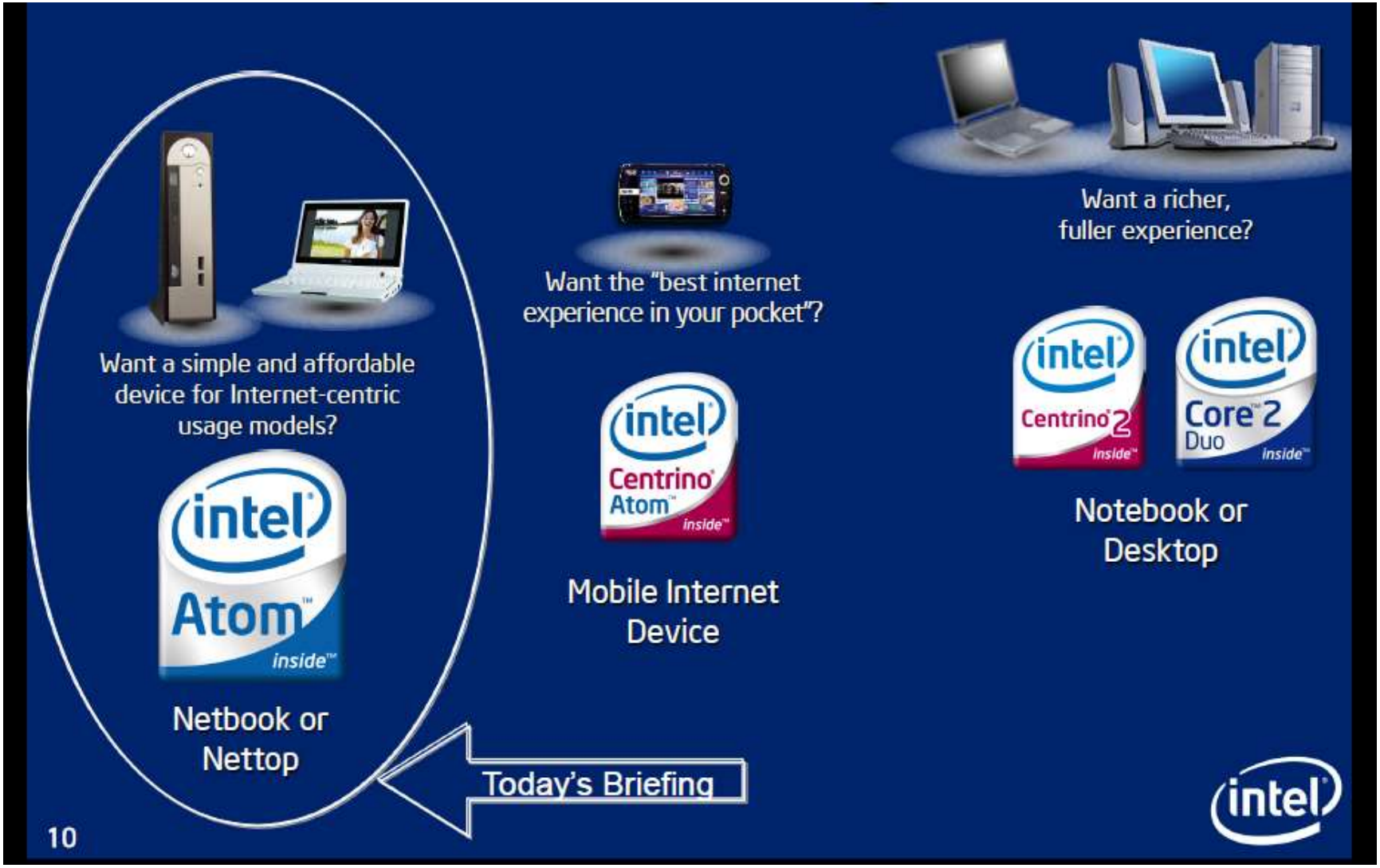
The first Atom processor based platform was the Diamondville platform, it targeted two product segments;

- entry-level desktops (termed as nettops) and
- netbooks.

It is based on the Bonnell microarchitecture.

The Diamondville platform was announced at the IDF Spring 2008 (4/2008), as shown below, first products arrived in 6/2008.

Introduction and positioning the Diamondville platform at the IDF 2008 (in 4/2008) [19]



Nettop: Entry-level desktop

Mobile Internet Device: typically a tablet

3.2 The Diamondville platform (3)

Note

On the slide Intel has also the brand mark "Centrino Atom" targeting "Mobile Internet Devices" that is tablets, in Intel's parlor.

Nevertheless, the "Centrino Atom" processor aimed at tablets is based on the same Bonnell microarchitecture as the Atom processor aimed at entry-level desktops and netbooks, and subsequently Intel branded both processors as Atom processors.

Here we mention also that the Centrino 2 platform that aimed at notebooks or desktops, covers 45 nm dual-core or quad-core Core 2 processors with a low power consumption (10- 25 W for dual core processors).

3.2 The Diamondville platform (4)

Simplified block diagram of the Diamondville platform

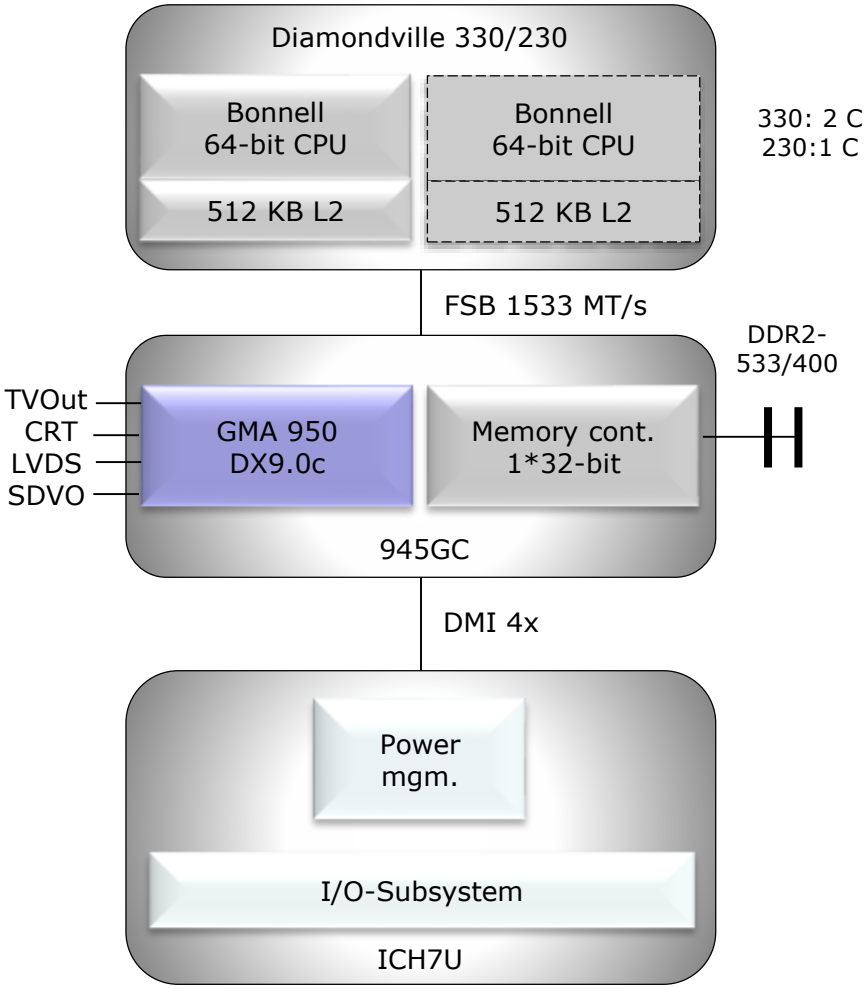
The Diamondville platform consists of three chips;

- the processor
- the north bridge and
- the south bridge,

as shown below for three different alternatives of the Diamond platform.

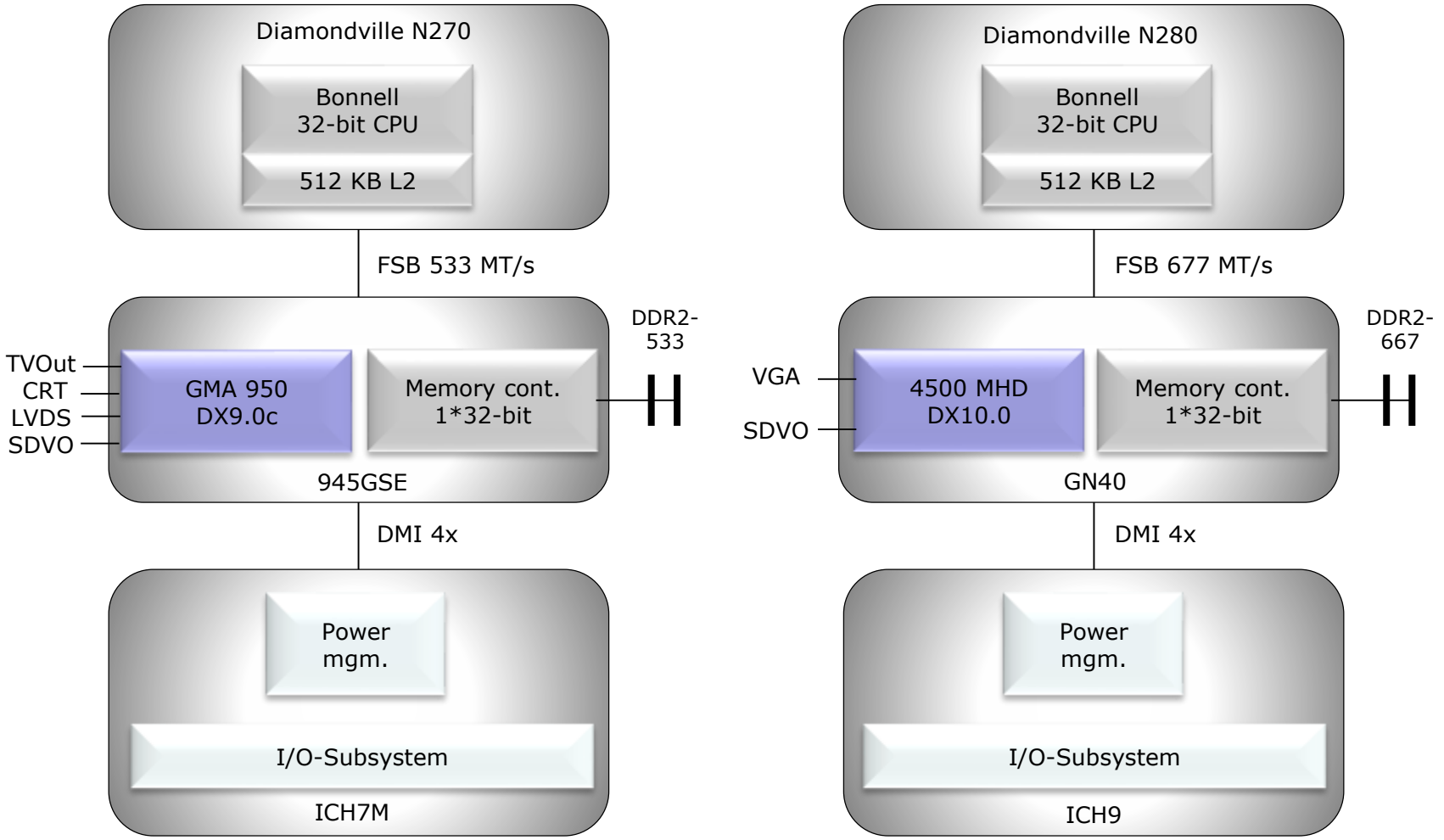
3.2 The Diamondville platform (5)

Simplified block diagram of the Diamond platform for entry-level desktops



3.2 The Diamondville platform (6)

Simplified block diagram of the Diamondville platform for nettops



3.2 The Diamondville platform (7)

Note that

- entry-level desktops are based on the 64-bit Bonnell microarchitecture whereas
- netbooks are built on the 32-bit Bonnell microarchitecture

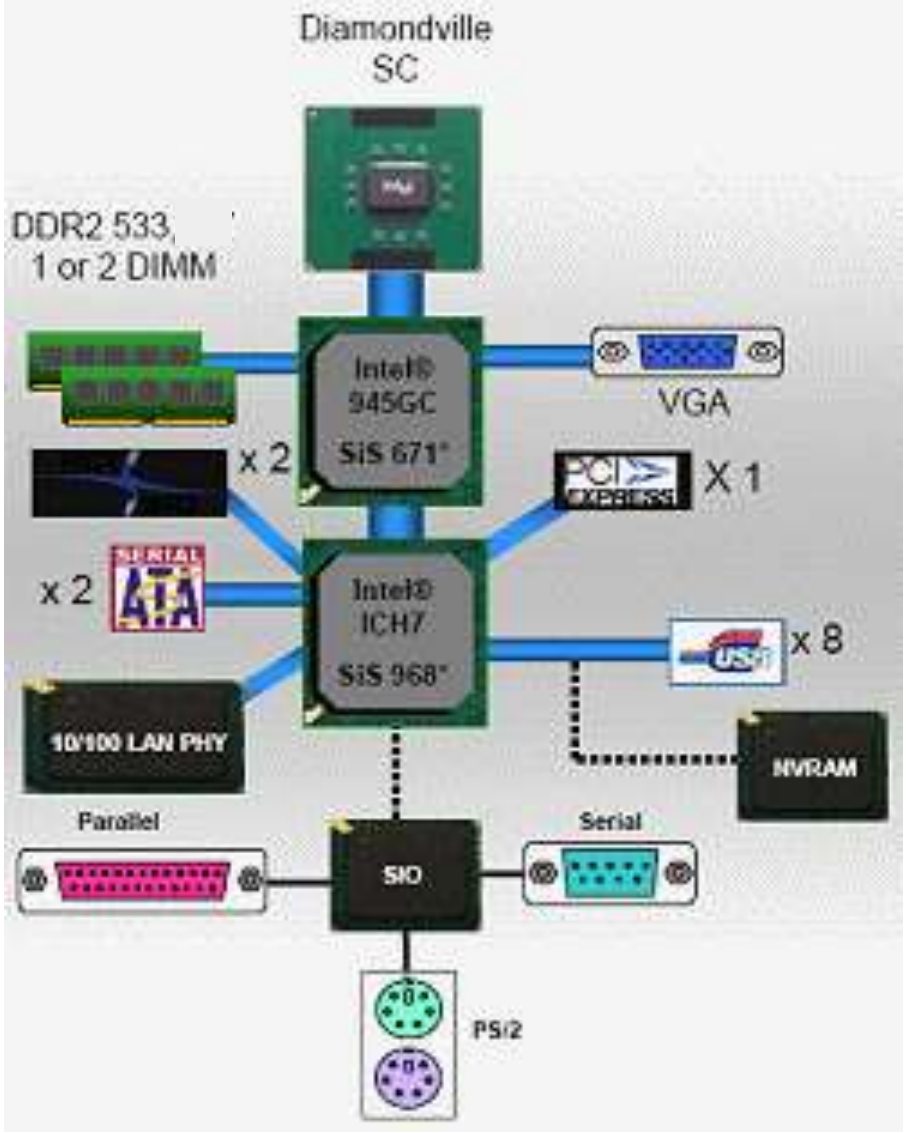
Concerning this point we mention that all subsequent Atom CPU based entry-level desktops and notebooks have 64 bit cores.

We point out further on the following features

- the entry-level 330 Diamondville processor has dual cores whereas all other processors have a single core,
- all platforms have a single channel DDR2 memory controller in the north bridge and
- all platforms have a graphics core (graphics media accelerator) also in the north bridge.

3.2 The Diamondville platform (8)

Block diagram of the single core Diamondville platform for entry-level desktops [66]



3.2 The Diamondville platform (9)

Main features of the Diamondville platform

	Diamondville				Pine Trail			
Launched	06/2008				01/2010			
Focus	Entry-level desktops (Nettops)		Notebooks/Sub notebooks (Netbooks)		Entry-level desktops (Nettops)		Notebooks/Sub notebooks (Netbooks)	
Processor	Diamondville				Pineview			
Models	330	230	N280	N270	D525/0510	D425/0410	N570/N550	N475-N435
Technology	45nm				45nm			
Die size	2x26mm^2	26 mm^2			87 mm^2	66 mm^2	87 mm^2	66 mm^2
No. of trans.	2x47 mtrs	47 mtrs			176 mtrs	123 mtrs	176 mtrs	123 mtrs
Micro-arch.	Bonnell				Bonnell			
32/64-bit	64-bit		32-bit		64-bit			
1C/2C	2C	1C	1C		2C	1C	2C	1C
HT	HT				HT			
fc [GHz]	1.6 GHz	1.6 GHz	1.67 GHz	1.6 GHz	1.80/1.67	1.8/1.66	1.66/1.50	1.83-1.33
L2	2x512 kB	512 kB			2x512 kB	512 kB	2x512 kB	512 kB
No. of mem.ch.	Single channel (64-bit)		Single channel (32-bit)		Single channel (64-bit)			
Memory	DDR2-533		DDR2-667	DDR2-533	DDR3-800 (only D525/D425) else DDR2-800/667		DDR3-667 (except N450/N470) DDR2-667	
GPU	GMA 950 in the north bridge		X4500 MHD in the north bridge	GMA 950	GMA 3150 on the processor die			
DX	DX 9.0c		DX 10	DX 9.0c	DX 9.0c			
Dixplay output	TVOut, CRT, LVDS, SDVO				VGA, LVDS			
GPU clock	400-133 MHz		533/400 MHz	166 MHz	400 MHz		200 MHz	
Proc. TDP	8 W	4 W	2.5 W		13 W	10 W	8.5 W	6.5-5 W
FSB	533/400 MT/s		667 MT/s	533 MT/s	DMI (2 lanes, each 500 MB/s in each direction)			
Socket	BGA 437				BGA 559			
Chipset	945GC[1] (Lakeport)[1] + ICH7U		GN40 + ICH9M	945GSE[2] + ICH7M	NM10 (Tiger Point)			
OS	Windows XP Home Linux				Windows XP Home/Windows Vista/Windows 7 Moblin (Intel's Linux version)			

MID: Mobile Internet Devices, typically tablets
UMPC: Ultra Mobile PC, typically tablets

[1]: TDP: 22,2 W
[2]: TDP: 11,8 W

Table: Intel's Atom-based platforms targeting entry level desktops (nettops) and netbooks-1

3.2 The Diamondville platform (10)

Note that the low processor TDP of 2.5 – 8 W is misleading, since the platform includes also the chipset that includes two chips with a considerable higher power consumption, e.g. the 945GC has a max. TDP of 22.2 W [67] whereas the ICH7 an additional 3.3 W [68].

3.3 The Pine Trail platform

3.3 The Pine Trail platform

- It was disclosed in 5/2009 along with the OS Moblin but launched only in 12/2009.
- The Pinetrail platform is based also on the Bonnell microarchitecture.
- It aims at entry-level desktops and nettops, as indicated in Intel's slide revealed at launching the platform in 12/2009).

Figure: Target market segments of the Pine Trail platform [69]

3.3 The Pine Trail platform (2)

Key innovation of the Pine Trail platform

Rather than being a tree-chip platform as the previous Diamondville platform, the Pine Trail platform includes only two chips

- the processor (termed as the Pineview processor) and a
- the peripheral control unit (the NM10 Tigerpoint), as indicated below.

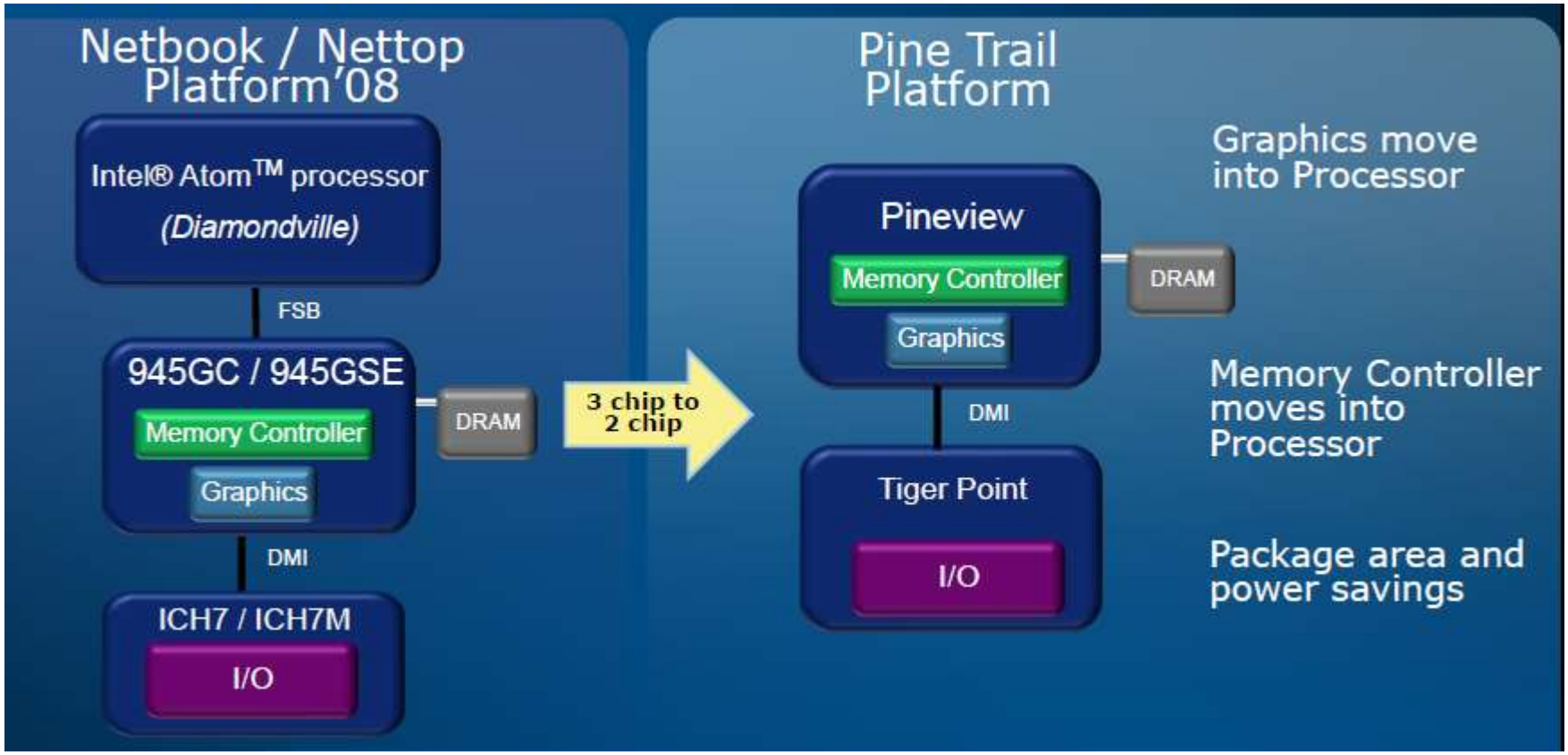


Figure: Simplified block diagram of the Pine Trail platform [70]

3.3 The Pine Trail platform (3)

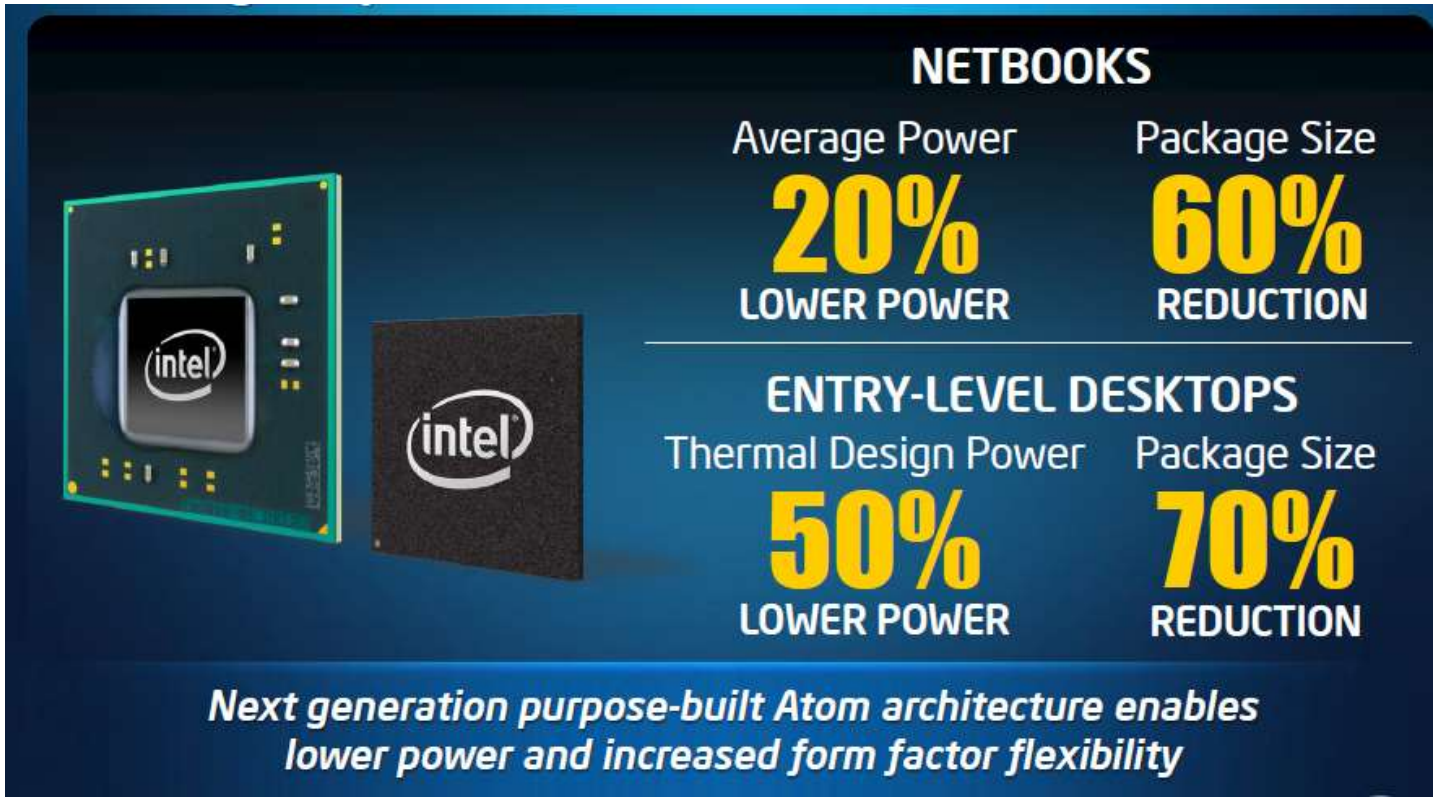
Benefits of the platform integration

- BOM savings (Bill Of Material savings)
- power reduction
- performance increase
- package size reduction,

as indicated next.

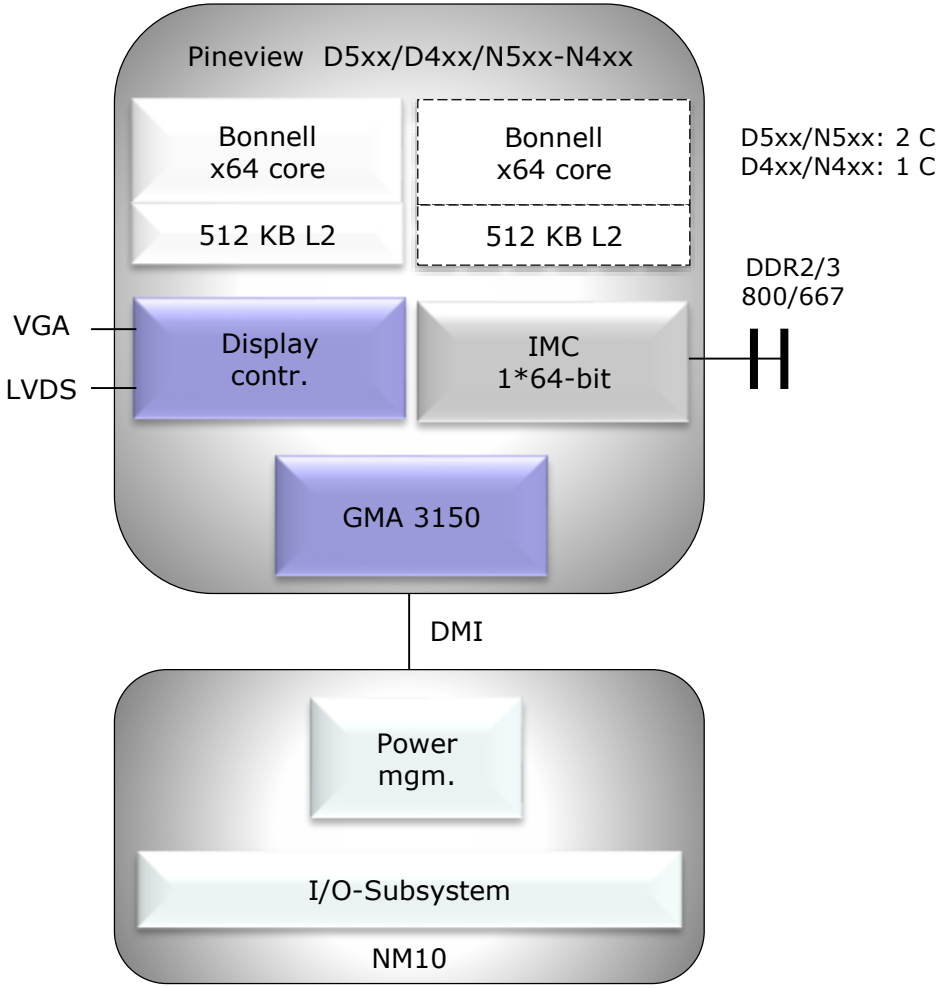
3.3 The Pine Trail platform (4)

Power and package size improvements of the Pine Trail platform vs. the previous Diamondville platform [69]



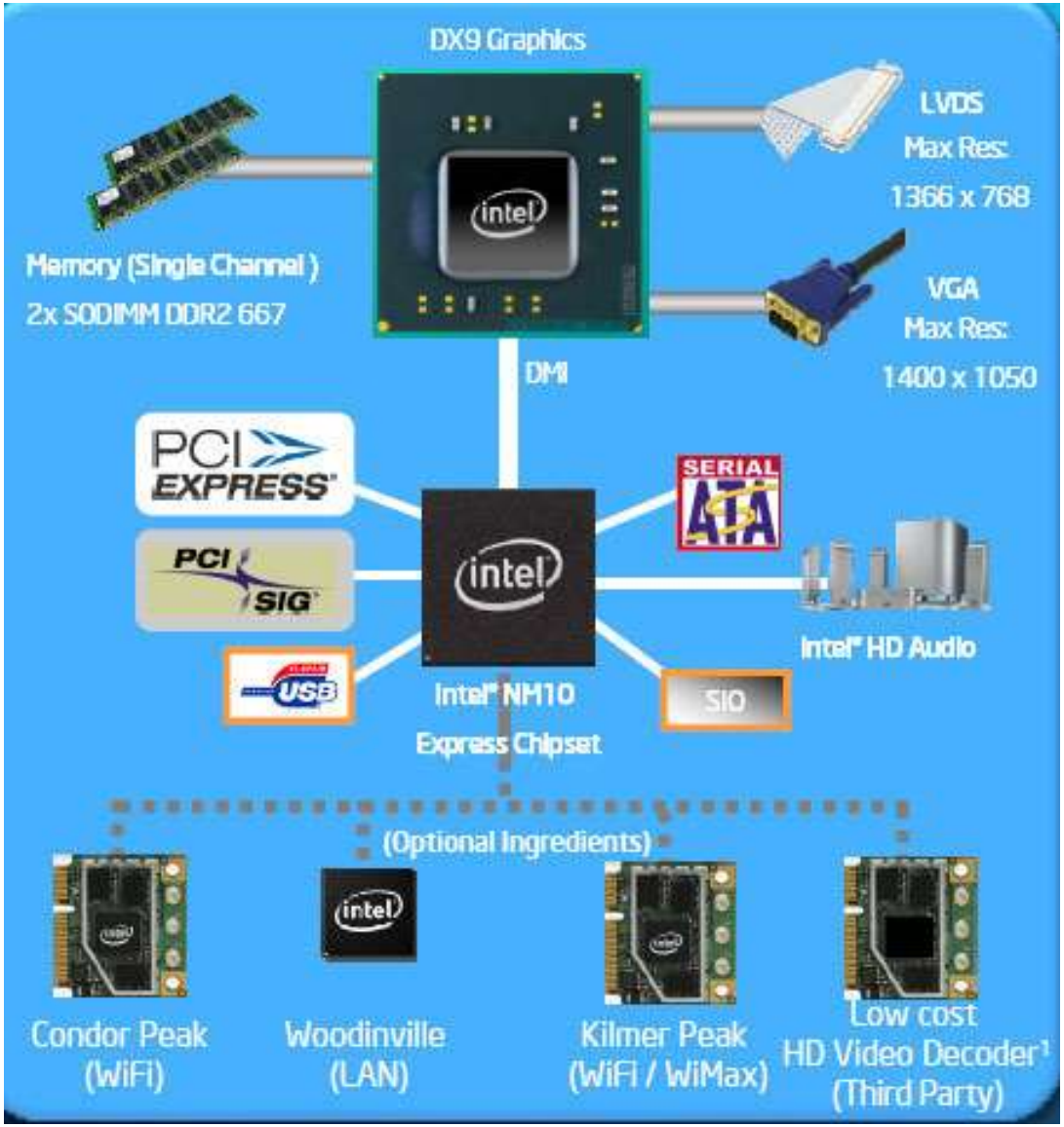
3.3 The Pine Trail platform (5)

Simplified block diagram of the Pine Trail platform for entry-level desktops and netbooks



3.3 The Pine Trail platform (6)

Example: Block diagram of the Atom N450-based configuration [71]



3.3 The Pine Trail platform (7)

Main features of the Pinetrail platform

	McCaslin	Diamondville				Pine Trail			
Launched	04/2007	06/2008				01/2010			
Focus	UMPC/MID	Entry-level desktops (Nettops)		Notebooks/Sub notebooks (Netbooks)		Entry-level desktops (Nettops)		Notebooks/Sub notebooks (Netbooks)	
Processor	Stealy	Diamondville				Pineview			
Models	A110/A100	330	230	N280	N270	D525/0510	D425/0410	N570/N550	N475-N435
Technology	90nm	45nm				45nm			
Die size		2x26mm^2	26 mm^2			87 mm^2	66 mm^2	87 mm^2	66 mm^2
No. of trans.		2x47 mtrs	47 mtrs			176 mtrs	123 mtrs	176 mtrs	123 mtrs
Micro-arch.	Pentium M Dothan derivative	Bonnell				Bonnell			
32/64-bit	32-bit	64-bit		32-bit		64-bit			
1C/2C	1C	2C	1C	1C		2C	1C	2C	1C
HT	no HT	HT				HT			
fc [GHz]	0.8/0.6 GHz	1.6 GHz	1.6 GHz	1.67 GHz	1.6 GHz	1.80/1.67	1.8/1.66	1.66/1.50	1.83-1.33
L2	512 kB	2x512 kB	512 kB			2x512 kB	512 kB	2x512 kB	512 kB
No. of mem.ch.	Single channel (32-bit)	Single channel (64-bit)		Single channel (32-bit)		Single channel (64-bit)			
Memory	DDR2-400	DDR2-533		DDR2-667	DDR2-533	DDR3-800 (only D525/D425) else DDR2-800/667		DDR3-667 (except N450/N470) DDR2-667	
GPU	GMA 950 in the north bridge	GMA 950 in the north bridge		X4500 MHD in the north bridge	GMA 950	GMA 3150 on the processor die			
DX	DX 9.0c	DX 9.0c		DX 10	DX 9.0c	DX 9.0c			
Dixplay output	VGA, SDVO	TVOut, CRT, LVDS, SDVO				VGA, LVDS			
GPU clock	133 MHz	400-133 MHz		533/400 MHz	166 MHz	400 MHz		200 MHz	
Proc. TDP	3 W	8 W	4 W	2.5 W		13 W	10 W	8.5 W	6.5-5 W
FSB	400 MT/s	533/400 MT/s		667 MT/s	533 MT/s	DMI (2 lanes, each 500 MB/s in each direction)			
Socket	BGA 663	BGA 437				BGA 559			
Chipset	945GU + ICH7U	945GC[1] (Lakeport) + ICH7U		GN40 + ICH9M	945GSE[2] + ICH7M	NM10 (Tiger Point)			
OS	Windows XP Linux	Windows XP Home Linux				Windows XP Home/Windows Vista/Windows 7 Moblin (Intel's Linux version)			

MID: Mobile Internet Devices, typically tablets
UMPC: Ultra Mobile PC, typically tablets

[1]: TDP: 22,2 W
[2]: TDP: 11,8 W

Table: Intel's Atom-based platforms targeting entry level desktops (nettops) and netbooks-1

3.3 The Pine Trail platform (8)

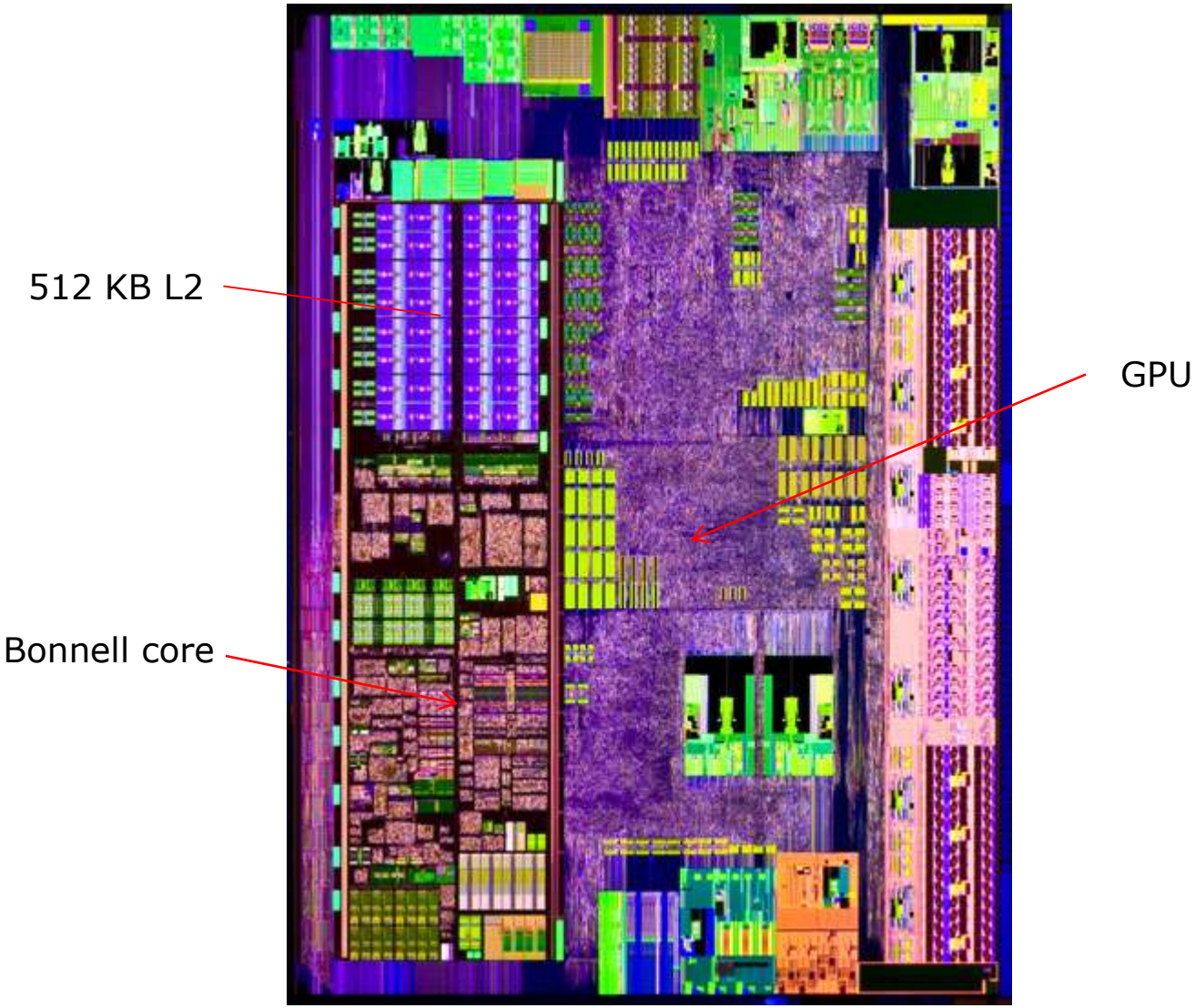
Remark

We point out the following features of the Pineview processor line:

- Processor models introduced
  - D5xx-D4xx for entry-level desktops
  - N5xx_N4xx for notebooks/subnotebooks
- Core count
  - 4xx models: single core
  - 5xx models: dual core
- Microarchitecture
  - 64 bit Bonnell microarchitecture
- Die size and transistor count
  - Single core models: 66 mm2/123 mtrs
  - Dual core models: 87 mm2/176 mtrs

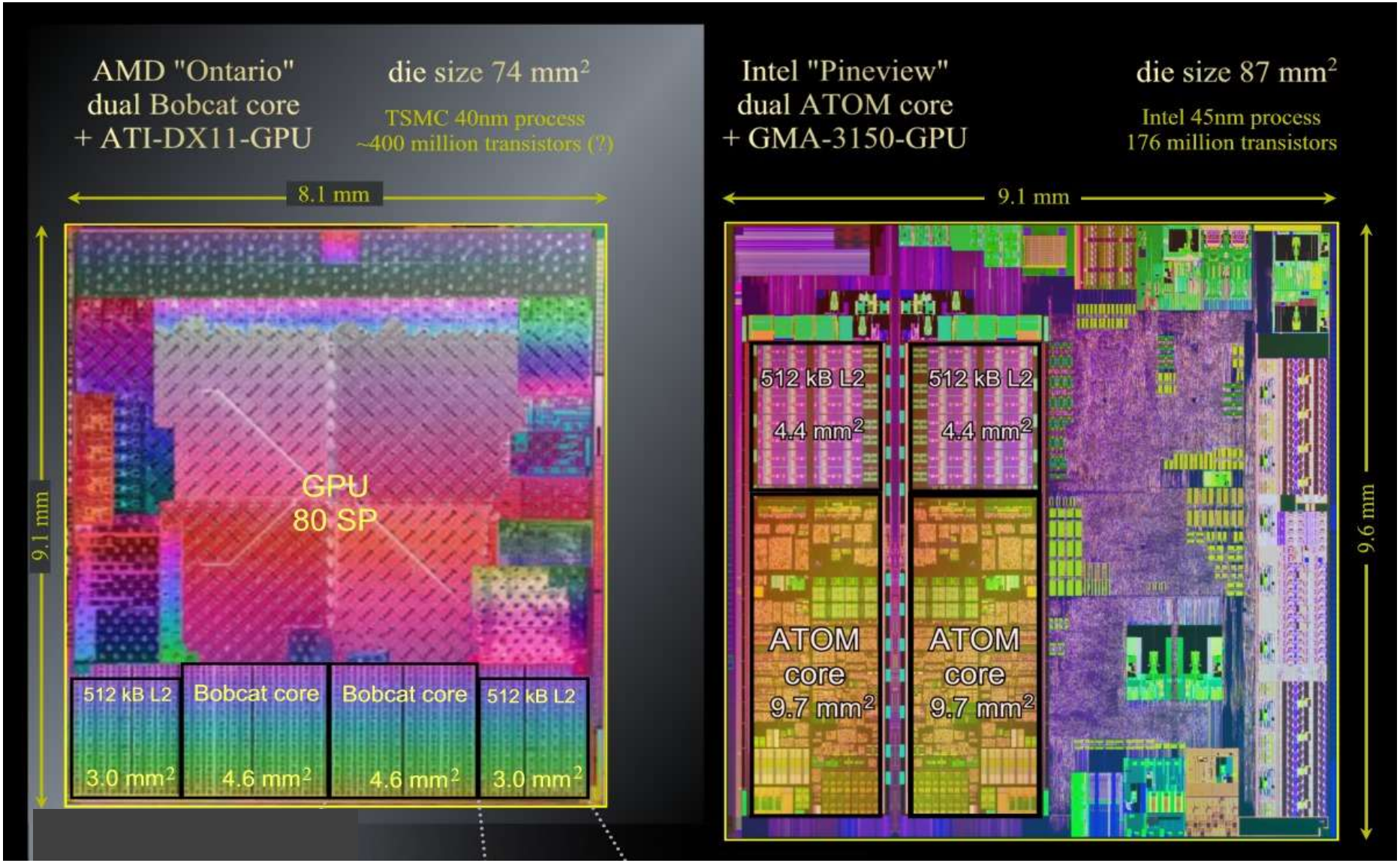
3.3 The Pine Trail platform (9)

Die shot of the single core N450 Pineview processor [72]



3.3 The Pine Trail platform (10)

Die shot of the dual core Pineview processor vs. AMD's dual Bobcat core [73]



3.3 The Pine Trail platform (11)

Note that AMD's Bobcat-based processors devote a much larger area for graphics than Intel's Pineview processors.

AMD's Bobcat processors have accordingly a better graphics performance than Intel Atom-based processors.

OS support of the Pine Trail platform [69]

3.4 The Cedar Trail-D/M platform

3.4 The Cedar Trail-D/M platform

- Announced

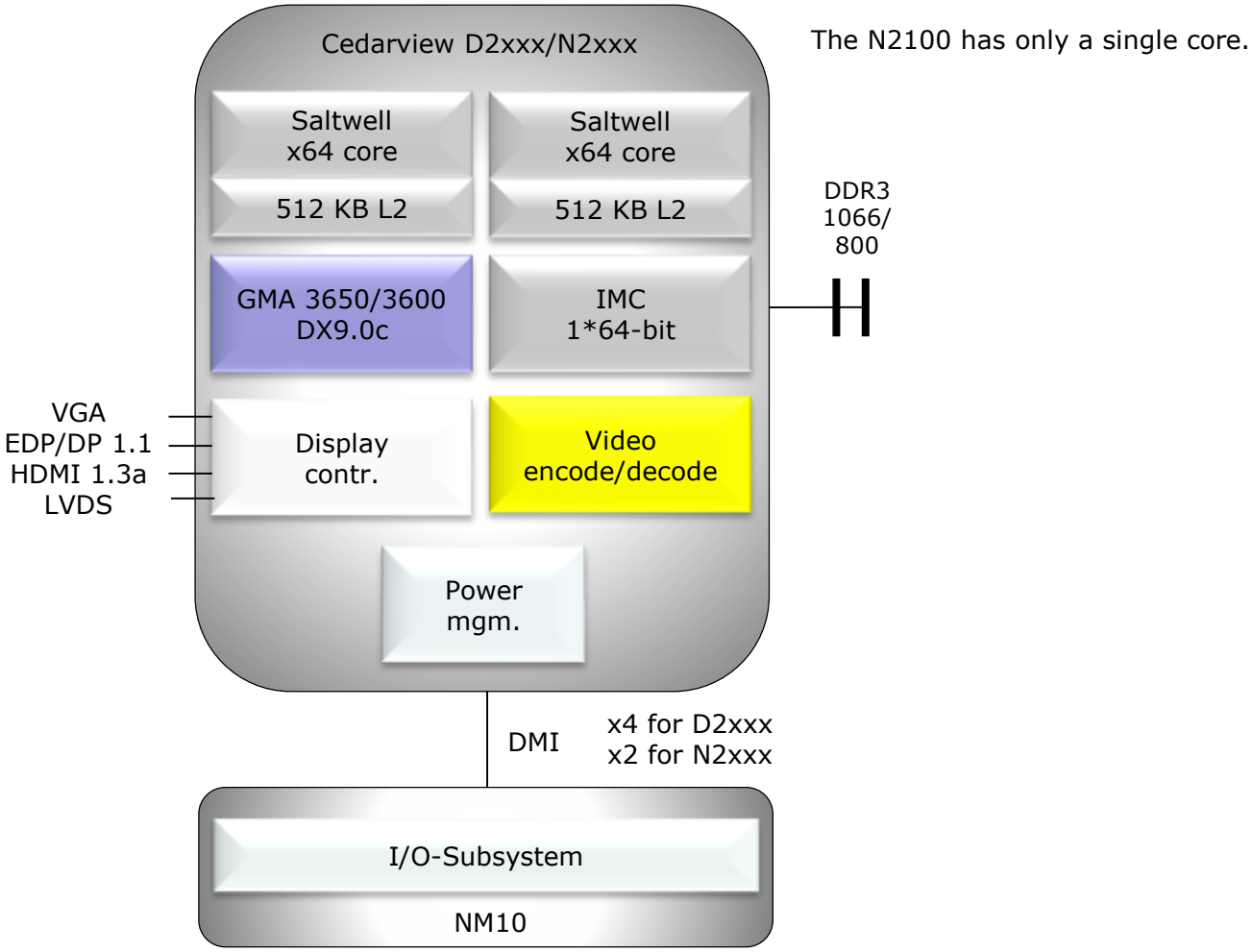
  in 1/2011 at the CES (Consumer Electronic Show) with imminent release promised then subsequently many times postponed throughout 2011 [74].

- First Cedar Trail-D/M based products: Q3/2011.

- Based on the 32 nm Saltwell CPU core.

3.4 The Cedar Trail-D/M platform (2)

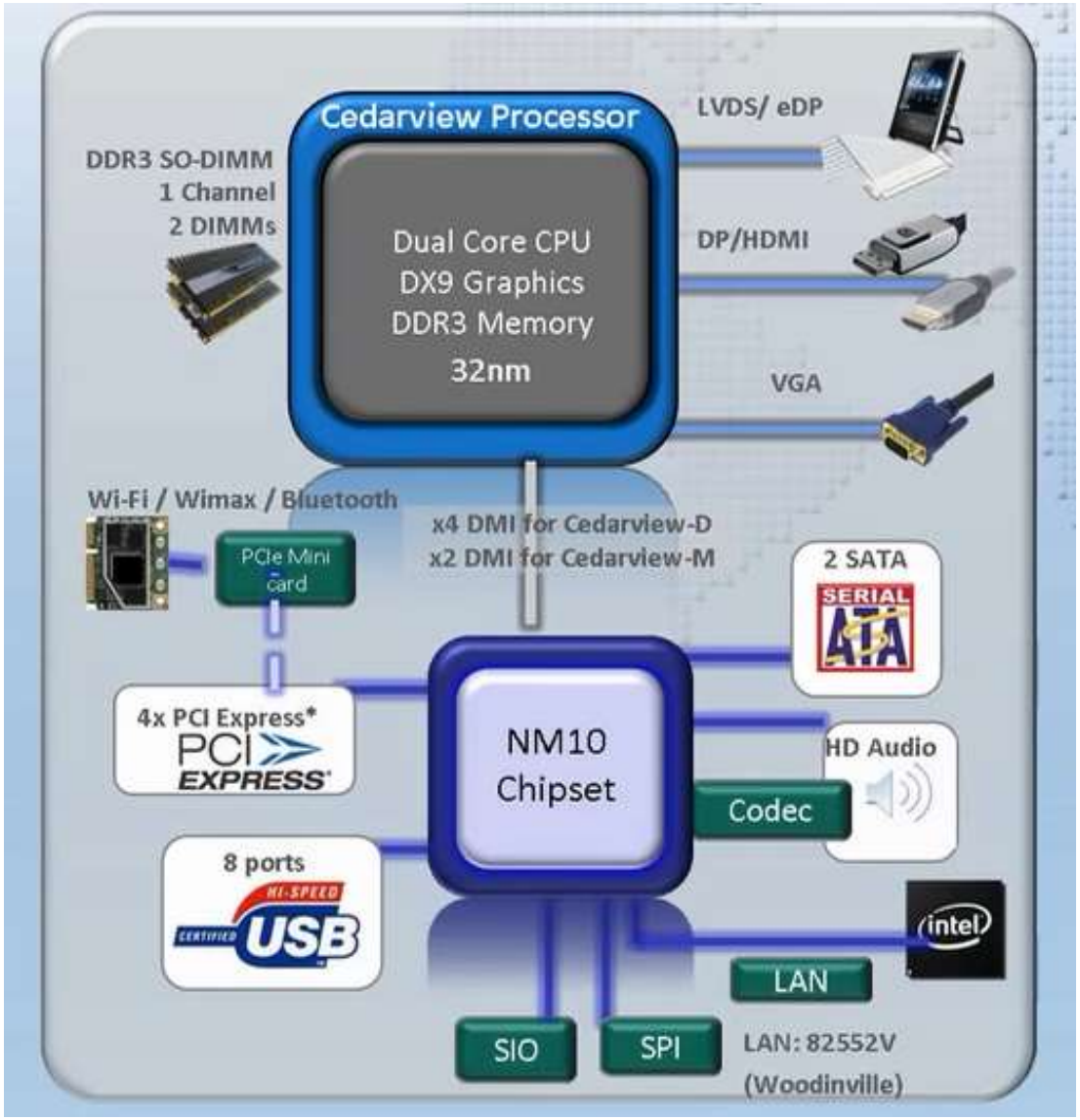
Simplified block diagram of the Cedar Trail-D/M platforms



The N2100 has only a single core.

3.4 The Cedar Trail-D/M platform (3)

Block diagram of the Cedar Trail-D/M platforms [75]



3.4 The Cedar Trail-D/M platform (4)

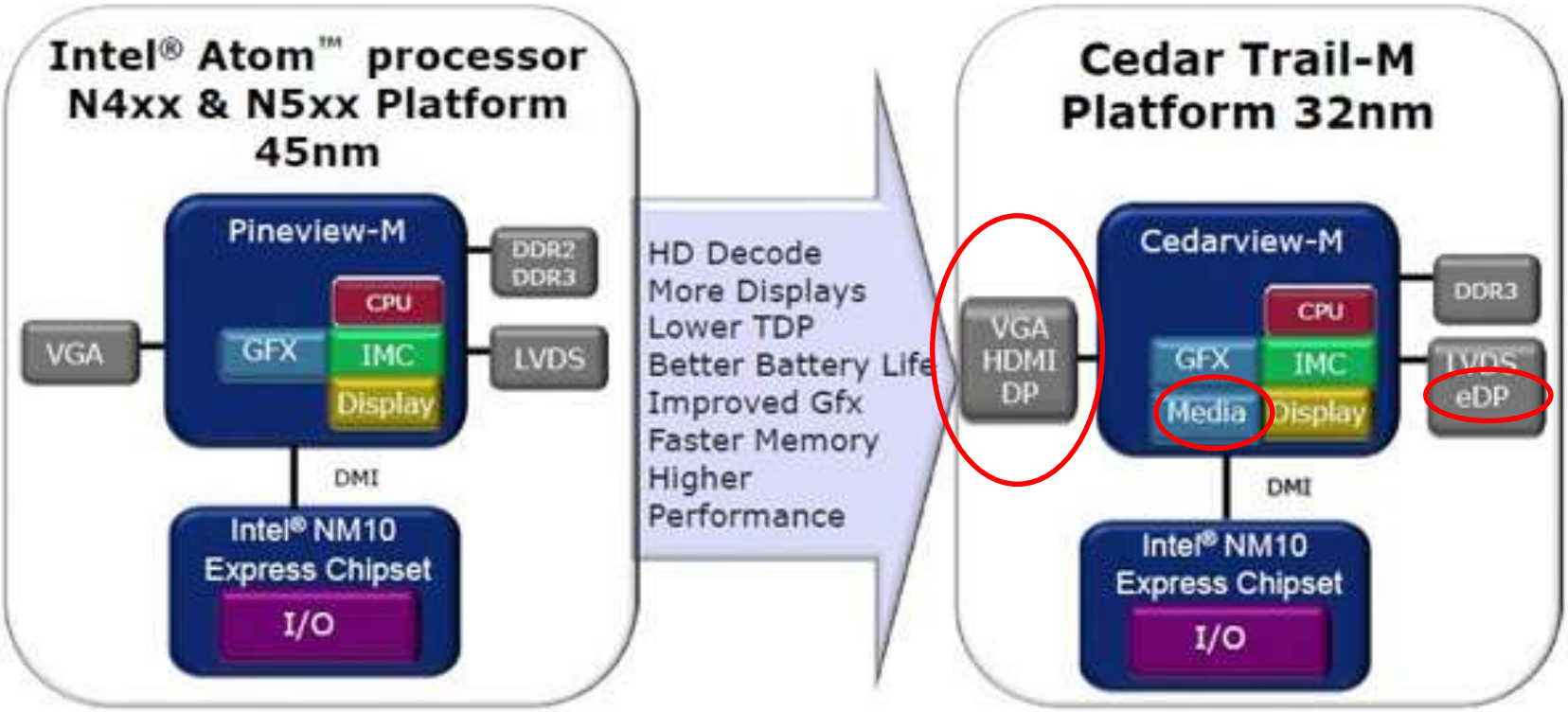
Key features of the Cedarview-D and Cedarview-N processor lines

- Processor models introduced
  - D2700/D2550/D2500 for entry-level desktops
  - N28000/N2600 for netbooks
- Core count
  - All processors introduced include dual cores
- Microarchitecture
  - 64 bit Saltwell microarchitecture
- Hyperthreading
  - Supported except the N2550 model
- Die size and transistor count
  - Not revealed

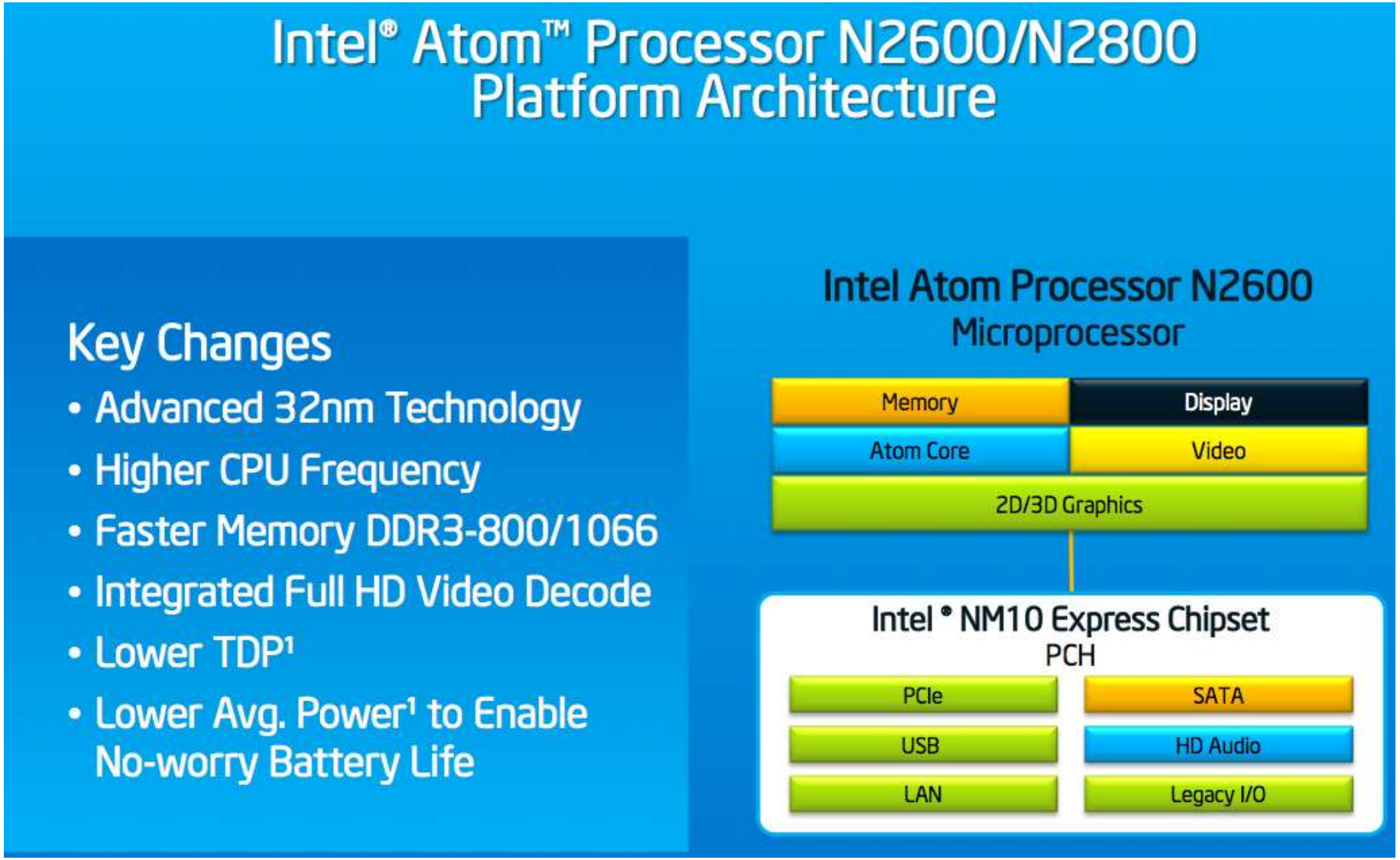
3.4 The Cedar Trail-D/M platform (5)

Improvements of the Cedar Trail-M platform over the previous Pine Trail platform-1 [76]

Pine Trail platform



Improvements of Cedar Trail-D/M features vs. the previous Pine Trail platform-2 [76]



3.4 The Cedar Trail-D/M platform (7)

Improvements of Cedar Trail-D/M features vs. the previous Pine Trail platform-3 [77]

	N450/N455	N570	N2600	N2800
Targeting fanless	No	No	Yes	No
Number of cores	1	2	2	2
Frequency	1.66GHz	1.66GHz	1.60GHz	1.86GHz
Cache	1x 512K L2	2x 512K L2	2x 512K L2	2x 512K L2
Max C-state	C4E	C4E	C6	C6
2-thread support	✓ 2 threads total	✓ 4 threads total	✓ 4 threads total	✓ 4 threads total
XD Bit	✓	✓	✓	✓
Gfx Frequency	200MHz / DX9	200MHz / DX9	400MHz / DX9	640MHz / DX9
Memory Support	DDR2/3-667	DDR3-667	DDR3-800	DDR3-1066
Kit TDP	8W	10W	5W	8W
Kit Average Power	~2.27W[1]	~2.40W[1]	~1.90W[1]	~2.62W[1]
Production/PV Timeline	In production	In Production	In Production	In Production
Validated Chipset	Intel® NM10 Express Chipset	Intel® NM10 Express Chipset	Intel® NM10 Express Chipset	Intel® NM10 Express Chipset

Cedar Trail-M Dual Core improvement over Pine Trail-M Dual Core

[1] N455/N570 Average power is based on QS samples measurements; and N2600/N2800 Average power in based on QS samples measurements

intel

3.4 The Cedar Trail-D/M platform (8)

Main features of the Cedar Trail-D/M platform

	Cedar Trail-D/M		Bay Trail - D	Bay Trail - M
Launched	Q3/2011		Q3 2013	Q3 2013
Focus	Entry Level DTs	Notebooks	Entry level DTs All-in-One DTs (AIO)	Notebooks/"2 in 1's
Processor	Cedarview – D/ M		Valleyview - D	Valleyview - M
Models	D2701-D2500	N2800-N2100	J2900/J2850/J1900/ J18xx/J1750	N35xx/N29xx/N28xx
Technology	32nm		22nm	
Die size				
No. of trans.				
Micro-arch.	Saltwell		Silvermont (Out-Of-Order)	
32/64-bit	64-bit		64-bit	
No. of cores	2C	1C/2C	2C/4C	
HT	HT (except D2500)		no	
fc [GHz]	2.13-1.86	1.86/1.6	Up to 2.41 GHz	Up to 2.16 GHz
L2	2x512 kB		2x1 MB for 4 cores/1 MB for one core	
No. of mem.ch.	Single channel (64-bit)		Dual channels (64-bit)	
Memory up to	DDR3-1066/800		DDR3L-1333	DDR3L-1066/1333
GPU	GMA 3650/GMA 3600 (Power VR SGX 545)		Gen. 7	
DX	DX 9.0C		DX 11	
GPU clock (base)		640/400 MHz	688 MHz	313 MHz
ISP	--		ISP	
Display output	VGA, eDP, DP1.1, HDMI 1.3a, LVDS		VGA, DP 1.2, HDMI 1.4a, MIPI-DSI	
Proc. TDP	10 W	6.5/3.5 W	≤ 10 W	≤7.5 W
FSB	DMI x4 (Actually 4/2 PCIe lanes in both dir.)	DMI x2	–	
Socket	BGA 559		FCBGA1170	
Chipset	NM 10		no, SoC	
OS	Windows XP Windows 7 MeeGo 1.2 Windows Embedded CE		Windows 7 Windows 8 non CS Linux	Windows 7 Windows 8 non CS Windows 8 (32-bit)

3.4 The Cedar Trail-D/M platform (9)

Platform innovations introduced along with the Cedar Trail D/M platform

- Wireless display
- Intel Rapid Start Technology and
- Sensor implementations,

as discussed next.

3.4 The Cedar Trail-D/M platform (10)

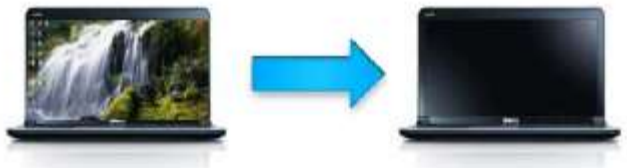
Wireless display [78]

Aim: wireless transfer of entry level desktop or netbook content on the TV screen

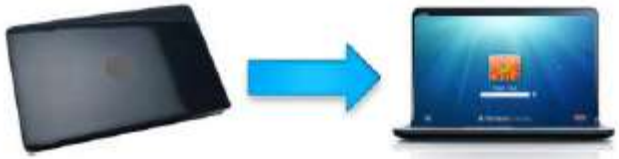
3.4 The Cedar Trail-D/M platform (11)

Intel Rapid Start Technology [78]

Wake ups from the hibernate state become almost as quick as waking up from the sleep state.



1. User places system in Standby
2. After configured period of time, information in DRAM moves to non-volatile memory

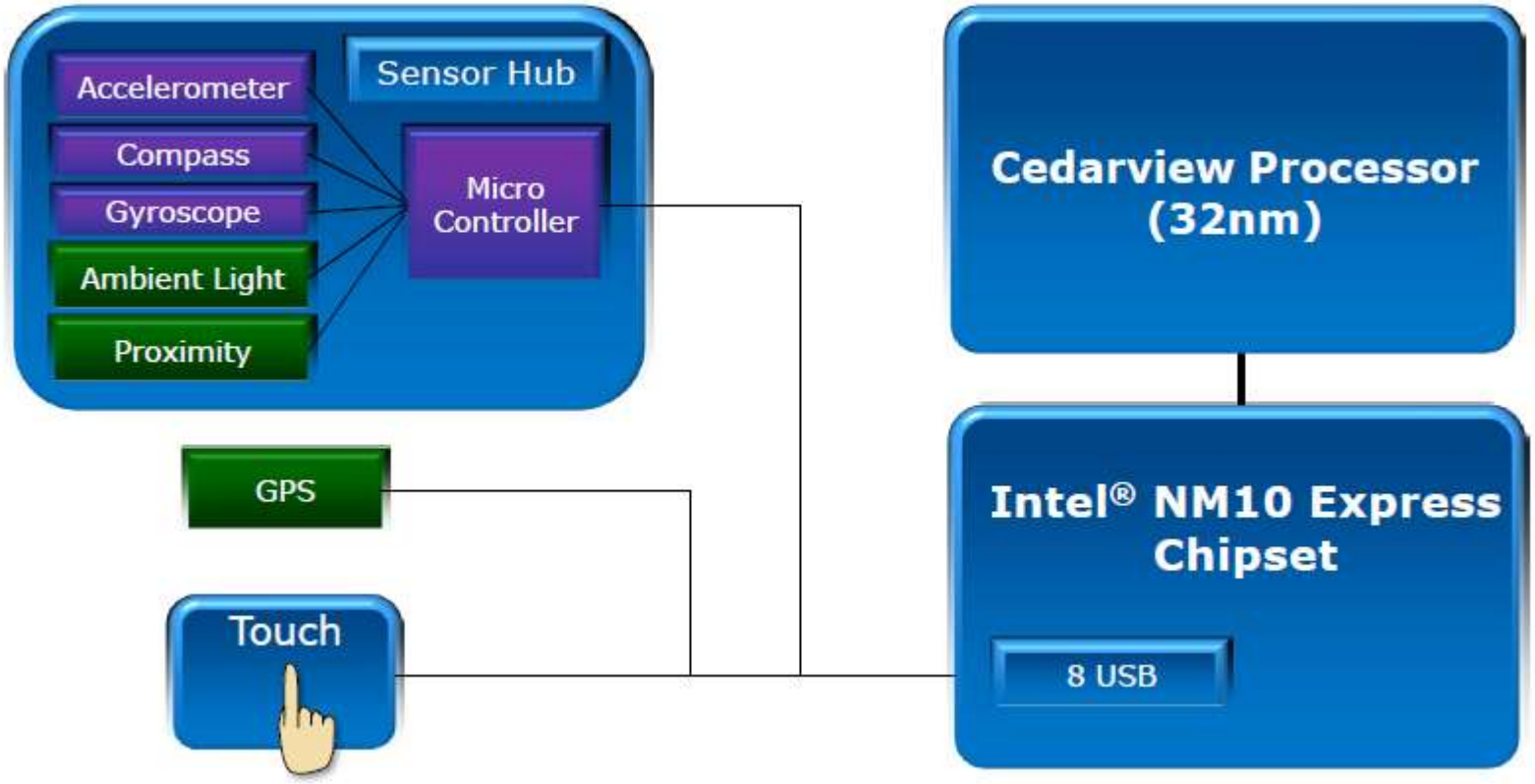


3. User powers on PC
4. Information moved back to DRAM
5. Operating system resumes like Standby

3.4 The Cedar Trail-D/M platform (12)

Sensors implementation [78]

Sensors may be attached via an USB sensor hub.



3.4 The Cedar Trail-D/M platform (13)

Assessment of the Cedar Trail-M platform [79]

- The Cedarview processors are only a few percent faster than the previous Pineview processors in real-life applications and are not much faster than AMD's Bobcat-based Zacate processors.
- The new graphics core was supposed to support DX10.1 graphics.
- Presumable, due to driver problems Cedar Trail-M at last was released only with DX9 support, so it does not provide any significant improvement over the previous one.
- Nevertheless, there is a valuable reduction in power consumption.
- All in all, it can be stated that the Cedar Trail-M platform is not fundamentally better than its predecessor, the Pine Trail platform and did not achieve any market success.

3.5 The Bay Trail D/M platforms

3.5 The Bay Trail D/M platforms

- Announced

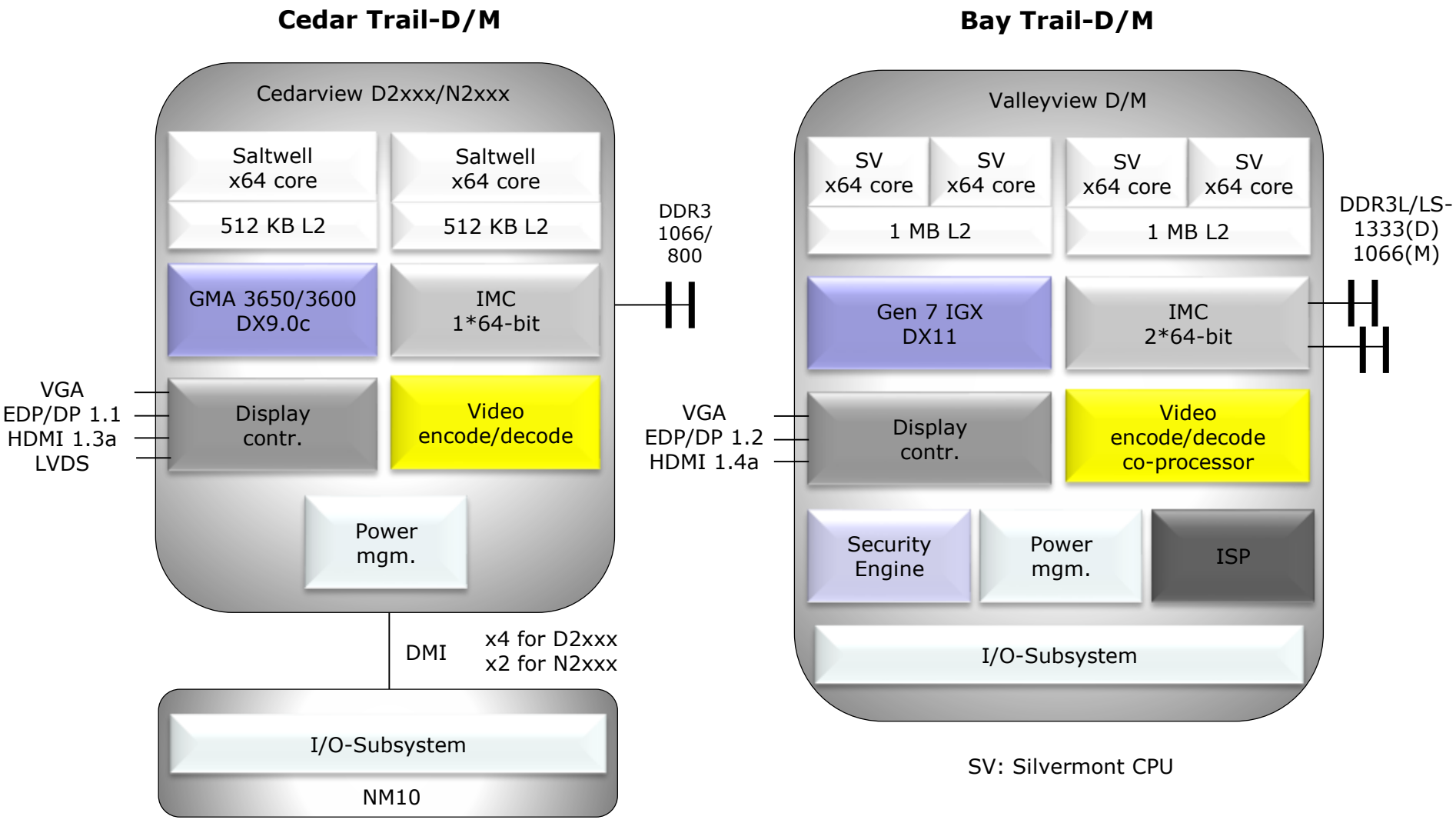
  first in 1/2013 at the CES (Consumer Electronic Show).
- Launched: 9/2013.
- Based on the 22 nm Silvermont CPU core.
- Supports both Windows 8.1 and Android.

3.5 The Bay Trail D/M platforms (2)

Target market segments of the Bay Trail-D/M platforms [80]

3.5 The Bay Trail D/M platforms (3)

Simplified block diagrams of the Bay Trail-D/M and Cedar Trail-D/M platforms



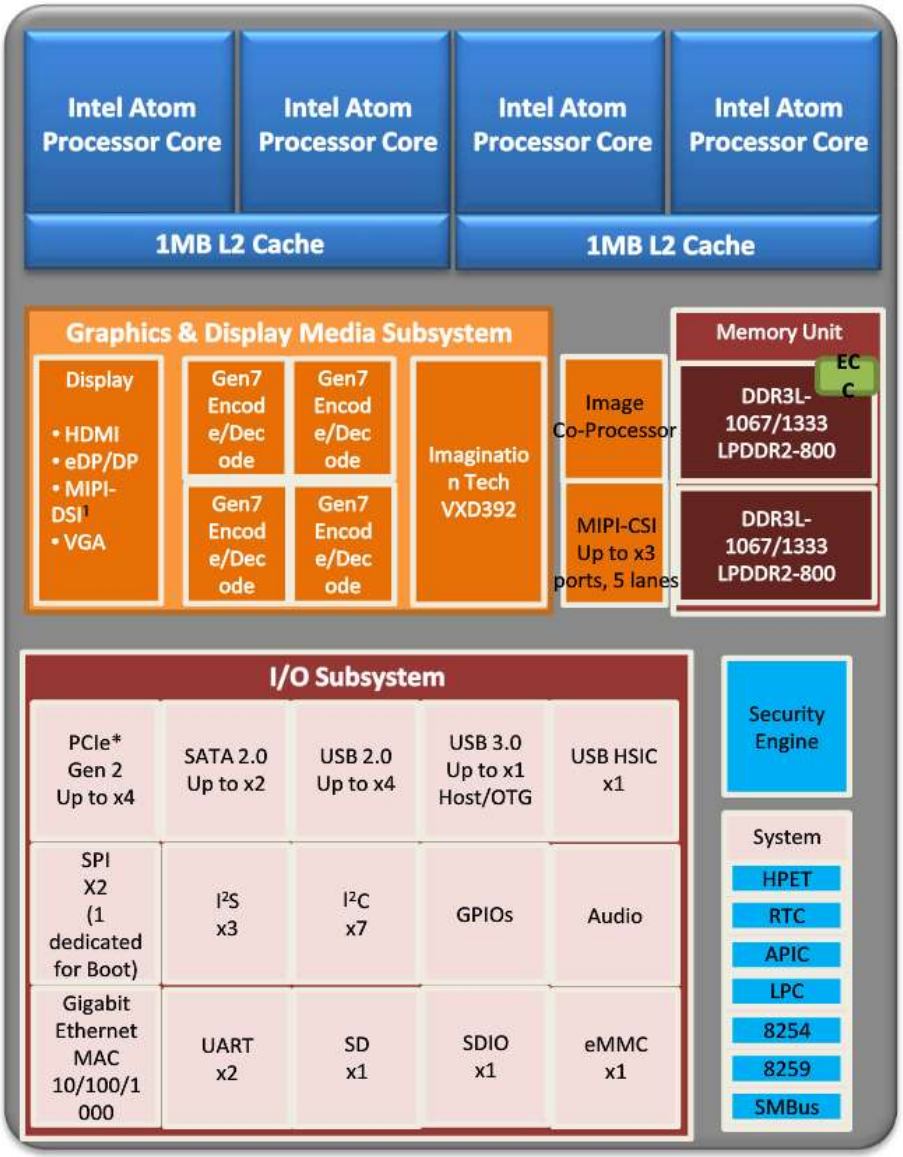
3.5 The Bay Trail D/M platforms (4)

Key features of the Bay Trail-D/M platforms

- SOC implementation
- Based on the 22 nm Silvermont core
- The Silvermont core has out-of-order issue
- No hyperthreading
- Dual-core modules – up to two modules
- DX11 capable graphics
- Video encode/decode coprocessor
- Security Engine
- ISP (Integrated Signal processor)

3.5 The Bay Trail D/M platforms (5)

More detailed block diagram of the Valleyview-D/M SOC [81]



3.5 The Bay Trail D/M platforms (6)

Main features of the Bay Trail-D/M platforms [81]

CORE
- 22nm Process Technology Intel® Atom™ processor
- Estimated Speeds – 1.2GHz to 2.4GHz
- 1, 2 and 4 core SKUs
- 512Kb L2 cache per core
- Intel® 64 architecture, Intel® Virtualization Technology, XD Bit
- Extended Temp SKUs
- AEC Q100 Auto Qualified SKUs

MEMORY
- Dual & Single Channel SKUs
- DDR3L-1067/1333, ECC capable in single channel mode
- LPDDR2-800
- Max 8GB
- 32/64 bit width

GRAPHICS, DISPLAY & MEDIA
- 4 Intel Gen 7 Graphics Engines, x2 Display Pipes
  - Decode - H.264, MPEG1, MPEG2, MPEG4, VC1/WMV9
  - Encode – H.264, MPEG2
- 1 Integrated Imagination Technology* VXD392 Decode Engine
  - Decode - H.264, JPEG, VP8

I/O HIGHLIGHTS
- PCI Express* Gen II - Up to x4 lanes
- Intel® High Definition Audio or Low Power Audio
- Image Co-Processor
- MIPI-CSI Camera Interface
- Security Engine
  - Secure Boot
  - Blu-Ray* Content Protection (*currently for automotive use*)
- Wide Range of I/O (e.g. SATA2, USB 2.0 Host, USB 3.0, SDIO, SPI, I^2C, I^2S, UARTs)

3.5 The Bay Trail D/M platforms (7)

Main features of the Bay Trail-D and Bay Trail-M platforms-1

	Cedar Trail-D/M		Bay Trail - D	Bay Trail - M
Launched	Q3/2011		Q3 2013	Q3 2013
Focus	Entry Level DTs	Notebooks	Entry level DTs All-in-One DTs (AIO)	Notebooks/"2 in 1's
Processor	Cedarview – D/ M		Valleyview - D	Valleyview - M
Models	D2701-D2500	N2800-N2100	J2900/J2850/J1900/ J18xx/J1750	N35xx/N29xx/N28xx
Technology	32nm		22nm	
Die size				
No. of trans.				
Micro-arch.	Saltwell		Silvermont (Out-Of-Order)	
32/64-bit	64-bit		64-bit	
No. of cores	2C	1C/2C	2C/4C	
HT	HT (except D2500)		no	
fc [GHz]	2.13-1.86	1.86/1.6	Up to 2.41 GHz	Up to 2.16 GHz
L2	2x512 kB		2x1 MB for 4 cores/1 MB for one core	
No. of mem.ch.	Single channel (64-bit)		Dual channels (64-bit)	
Memory up to	DDR3-1066/800		DDR3L-1333	DDR3L-1066/1333
GPU	GMA 3650/GMA 3600 (Power VR SGX 545)		Gen. 7	
DX	DX 9.0C		DX 11	
GPU clock (base)		640/400 MHz	688 MHz	313 MHz
ISP	--		ISP	
Display output	VGA, eDP, DP1.1, HDMI 1.3a, LVDS		VGA, DP 1.2, HDMI 1.4a, MIPI-DSI	
Proc. TDP	10 W	6.5/3.5 W	≤ 10 W	≤7.5 W
FSB	DMI x4 (Actually 4/2 PCIe lanes in both dir.)	DMI x2	—	
Socket	BGA 559		FCBGA1170	
Chipset	NM 10		no, SoC	
OS	Windows XP Windows 7 MeeGo 1.2 Windows Embedded CE		Windows 7 Windows 8 non CS Linux	Windows 7 Windows 8 non CS Windows 8 (32-bit)

3.5 The Bay Trail D/M platforms (8)

Comparing main features of the Cedar Trail-D/M vs. the Bay Trail-D/M platforms [82]

	Cedar Trail-D/M	Bay Trail-D/M
Process	32nm	22nm
Processor Frequency	1.6GHz & 1.8GHz (DC)	≥2.7 GHz (QC) With Burst Technology[1]
Max C-state	C6	C1 (BYT-D) C7[1] (BYT M)
Memory	DDR3-800/1067 MHz up to 4GB	DDR3L & DDR3L RS SODIMM – 1066 MHz (BYT-M) - 1333 MHz (BYT-D) up to 8GB
Graphics	DX10.1, OGL 3.0 Gfx @ 400/640 MHz	Gen7 DX11, OGL 3.2 Gfx with Burst Technology[1]
Display	LVDS, HDMI 1.3a, eDP, DP 1.1, VGA	Internal: eDP External: HDMI 1.4a, DP 1.2, VGA 2500x1600 @ 60Hz max res
Video Encode/ Decode	No HW encode MPEG2, h.264, VC-1/WMV9 Up to 1080p decode	Full HW acceleration for encode of H.264, MPEG2, MVC Up to 1080p decode. MVC, VP8 & JPEG/MJPEG, MPEG2, h.264, VC-1/WMV9
I/O	PCIe 2.0 4x1 & 1x4, 2 SATA, 8 USB 2.0 , SPI, HD Audio	PCIe 2.0, SATA 2.0, USB 2.0 & USB3.0 (Host mode only), eMMC 4.5, SDIO 3.0, UART, I2S, I2C, SPI, HD Audio, LPE[1]
TDP Targets	Cedar View-M: ≤3.5W and ≤6.5W	Valleyview-M: ≤4-6.5W[2] (BYT-M); ≤10W[2] (BYT-M)
CPU/SOC	Intel® NM10 Express Chipset: 1.5W	N/A
PCH Total Kit	≤5W and ≤8W	≤4-6.5W[2] (BYT-M); ≤10W[2] (BYT-M)

1) Not available on all SKUs

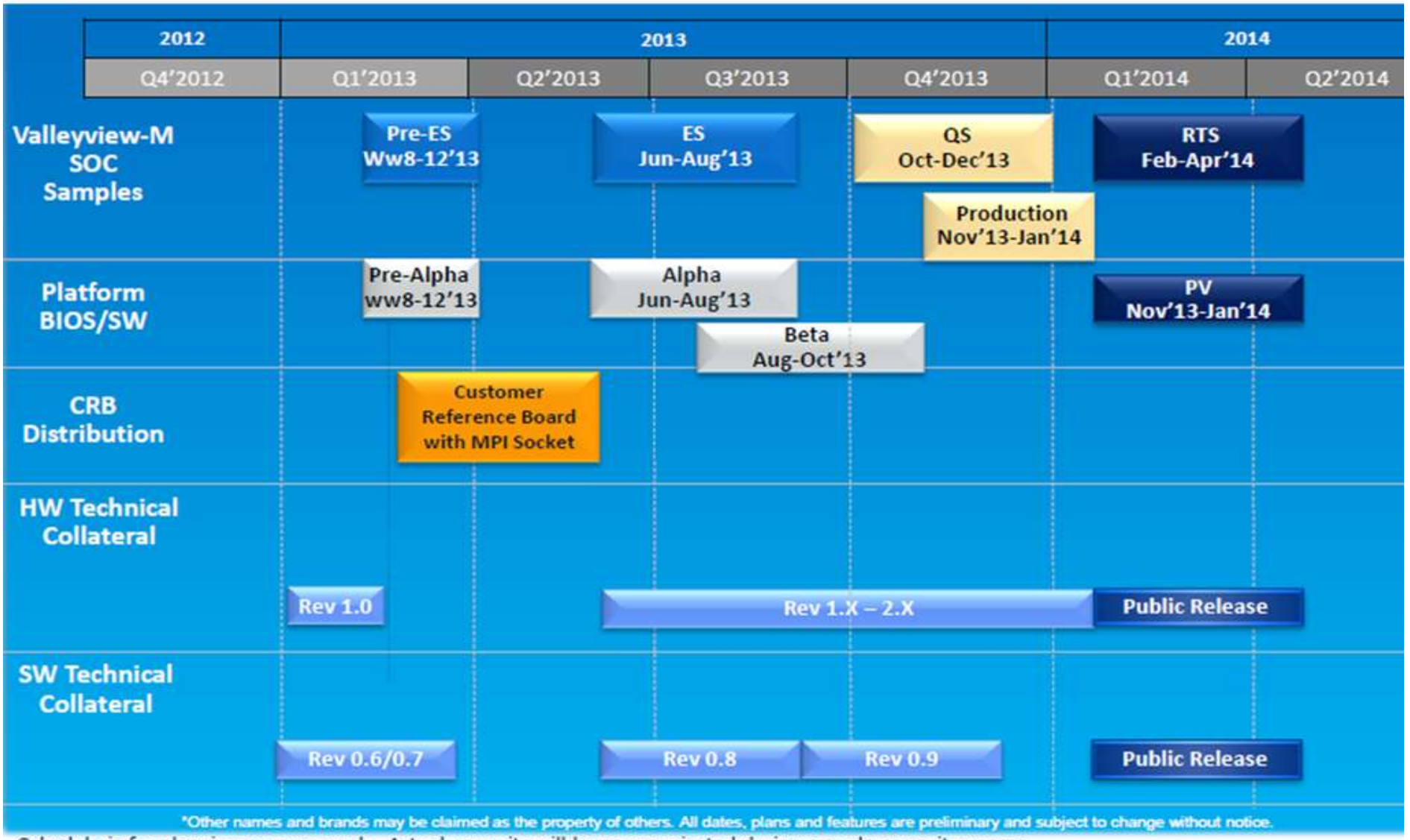
2) Target, pre-silicon estimate

3.5 The Bay Trail D/M platforms (9)

Price performance relation of Intel's Haswell and Bay Trail based notebooks [117]

3.5 The Bay Trail D/M platforms (10)

Bay Trail schedule [82]



Schedule is for planning purposes only. Actual commits will be communicated during sample commit process.

3.6 The Braswell platform

3.6 The Braswell platform

- Launched: 03/2015.
- Based on the 14 nm Airmont CPU.
- Supports Windows 7/Windows 8.1 and Windows 10.

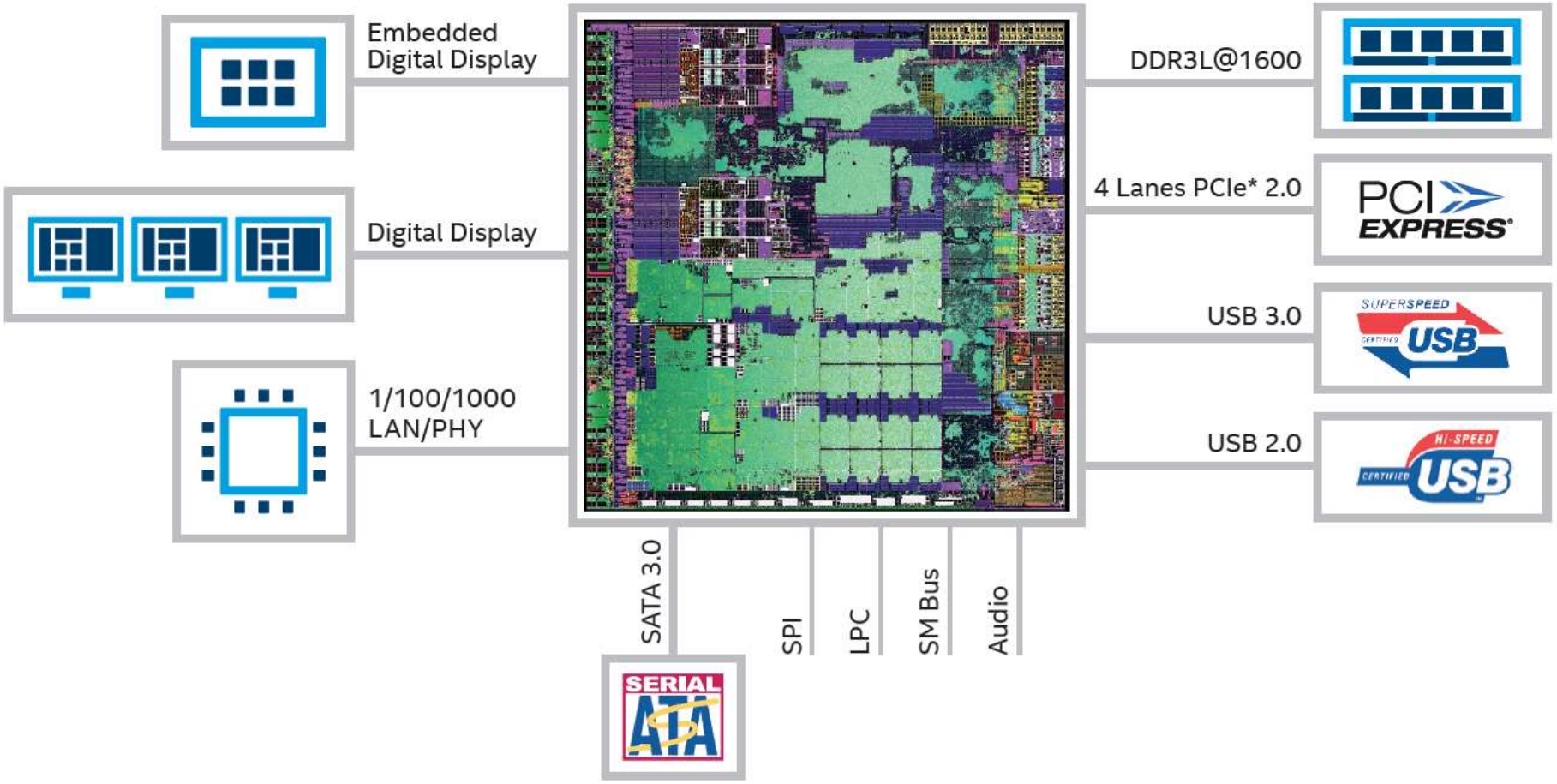
3.5 The Braswell platform (2)

Main features of the Braswell platform

	Braswell		Apollo Lake	
Launched	Q1/2015		Q3/2016	
Focus	Entry-level DTs	Notebooks/Convertibles	Entry level DTs	Notebooks/Convertibles
Processor	Braswell		Apollo Lake	
Models	J3710/J3160/J3060	N3710/N3700/ N3160/N3150/N30xx	J4205/J3455/J3355	N4200/N3400/N3300
Technology	14 nm		14 nm	
Die size				
No. of trans.				
Micro-arch.	Airmont		Goldmont	
32/64-bit	64-bit		64-bit	
No. of cores	2C/4C		2C/4C	
HT	no		no	
fc [GHz]	Up to 1.6 GHz		Up to 2.0 GHz	1.1 GHz
L2	1 MB/2 cores		1 MB/2 cores	
No. of mem.ch.	Dual channels (64-bit)		Dual channel (64-bit)	
Memory up to	DDR3L-1600		LPDDR4-2400	
GPU	Gen. 8 LP		Gen. 9 LP HD 505	
DX	DX 11.1		DX 12.0	
GPU clock (base)	Up to 400 MHz		250 MHz	200 MHz
ISP	ISP			
Display output	eDP, DP, HDMI		eDP, DP, HDMI, MIPI-DSI	
Proc. TDP	≤ 6.5 W	≤ 6 W	10 W	6 W
FSB	--		--	
Socket	FCBGA1170		FCBGA1296	
Chipset	no, SoC		No, SOC	
OS	Windows 7 (32/64-bit) Windows 8.1 (64-bit) Windows 10 (64-bit)		Windows 10 (64-bit)	

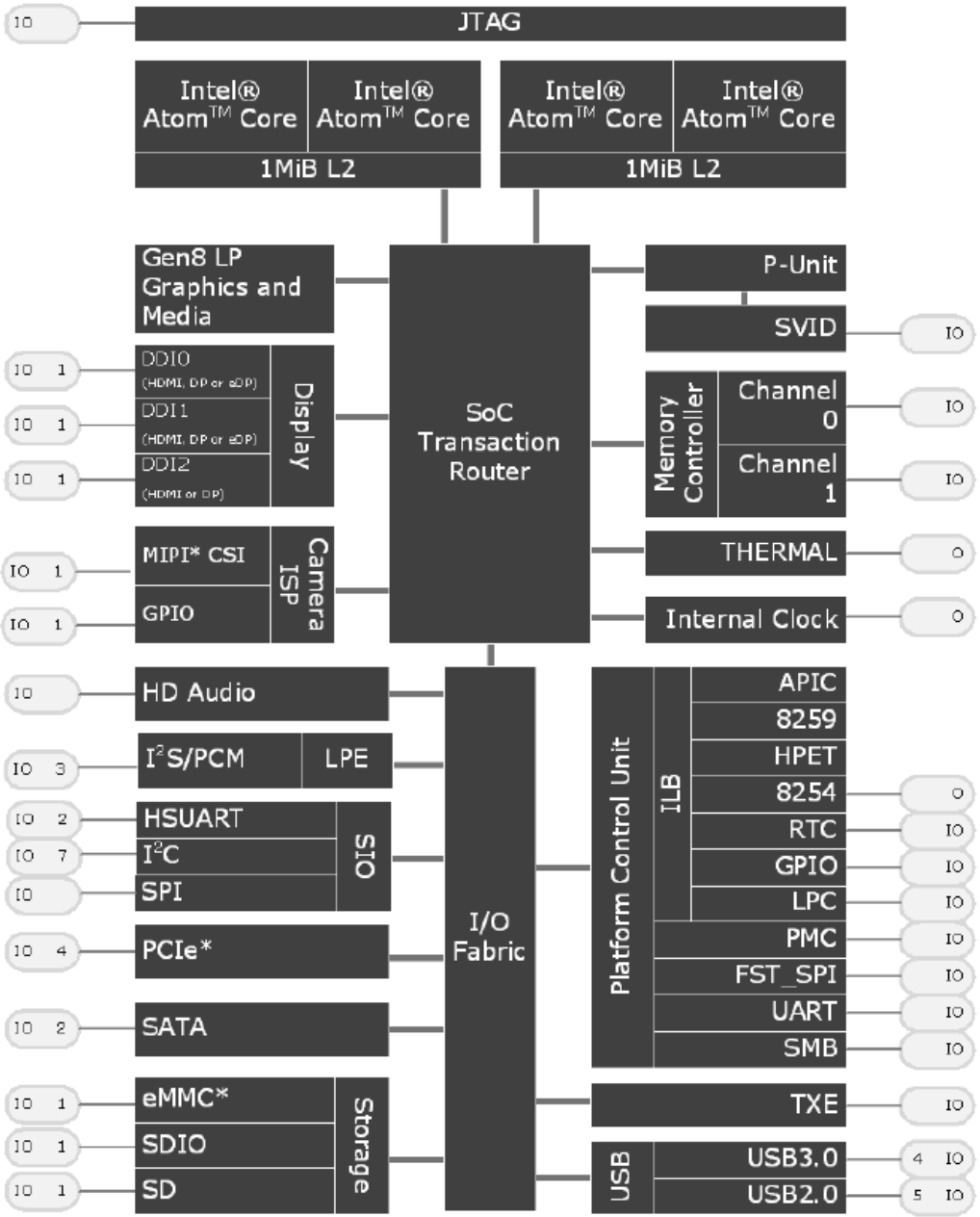
3.5 The Braswell platform (3)

Main components of the Braswell platform [154]



3.5 The Braswell platform (4)

Main components of the 4C Braswell SoC [155]



3.7 The Apollo Lake platform

3.7 The Apollo Lake platform

- Launched: Q3/2016.
- Based on the 14 nm Goldmont CPU.
- It intends compact, slim designs.
- Runs under Windows 10.

Aims of the Apollo Lake platform [156]

What Makes a Great Entry PC?

- Great choice for first-time buyers: education & small biz usage needs
- Performance for everyday content consumption and light productivity
- Great all work day battery life
- Graphics to handle your HD video entertainment

Apollo Lake Platform delivers the foundation for a great Entry design!

- A beautiful, sleek, portable design
- Affordable price

Intel® Processor for Entry Platforms (Apollo Lake)

IDF16

3.5 The Apollo Lake platform (3)

Benefits of the Apollo Platform for entry level DTs and notebooks [156]

Cost Savings Opportunities

$$$

- More cost reduction on power delivery (less VRs, PMIC options)
- More USB ports
- Mixed memory support
- Intel Sensor Solution
- MIPI Capabilities

CPU Performance

New architecture, improved CPU performance

Graphics Performance

Hardware accelerated codecs, Gen9 graphics engine

Battery Life

Improved battery life through lower over platform power

3.5 The Apollo Lake platform (4)

Apollo Lake features to "slim down" entry level PC and notebook designs [156]

- Smaller battery (while maintaining good battery life still thanks to great overall power on Apollo Lake)
- PMIC – Great lower cost power delivery option that can potentially save board area
- Solder down Wi-Fi* – Apollo Lake supports Intel® 802.11ac Wi-Fi solutions
- eMMC storage – Solder down storage
- Apollo Lake offers flexible memory options
  - DDR3L memory solder down option
  - LPDDR3 & LPDDR4 options
- MIPI camera – allows for thinner designs while potentially saving cost

PMIC: Power Management IC (for power supply)

eMMC: embedded Multi-Media Controller.

It refers to a package that includes both a flash memory and its controller integrated on the same silicon die.

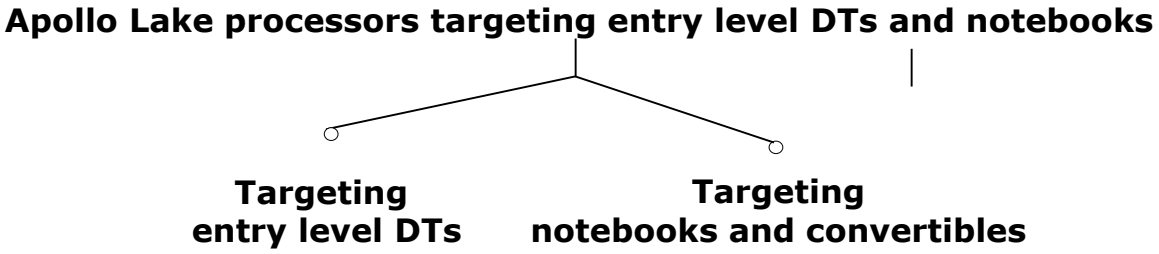
It is used instead of a 2.5 " HDD or an SSD.

802.11ac: High throughput (min. 1 Gbit/s) WiFi.

DDR3L: Low-voltage (1.25 V) low-power DDR memory.

3.5 The Apollo Lake platform (5)

Differentiation of Intel's J and N series Apollo Lake processors



3.5 The Apollo Lake platform (6)

Key features of Intel's Apollo Lake processors targeting desktops and notebooks [157]

S-Spec	MM#	Stepping	Processor Number	Functional Core	Core Speed		Integrated Graphics Core Speed		TDP (W)
					Burst Frequency Mode (BFM) 2C/1C	High Frequency Mode (HFM)	Burst Frequency	Base Frequency	
R2Y9	951483	B-0	Pentium® N4200	4	2.4 GHz/2.5 GHz	1.1 GHz	750 MHz	200 MHz	6
R2YA	951484	B-0	Celeron® N3450	4	2.1 GHz/2.2 GHz	1.1 GHz	700 MHz	200 MHz	6
R2YB	951485	B-0	Celeron® N3350	2	2.3 GHz/2.4 GHz	1.1 GHz	650 MHz	200 MHz	6
R2ZA	951843	B-1	Pentium® J4205	4	2.5 GHz/2.6 GHz	1.5 GHz	800 MHz	250 MHz	10
R2Z9	951842	B-1	Celeron® J3455	4	2.2 GHz/2.3 GHz	1.5 GHz	750 MHz	250 MHz	10
R2Z8	951841	B-1	Celeron® J3355	2	2.4 GHz/2.5 GHz	2.0 GHz	700 MHz	250 MHz	10
R2Z5	951830	B-1	Pentium® N4200	4	2.4 GHz/2.5 GHz	1.1 GHz	750 MHz	200 MHz	6
R2Z6	951833	B-1	Celeron® N3450	4	2.1 GHz/2.2 GHz	1.1 GHz	700 MHz	200 MHz	6
R2Z7	951834	B-1	Celeron® N3350	2	2.3 GHz/2.4 GHz	1.1 GHz	650 MHz	200 MHz	6

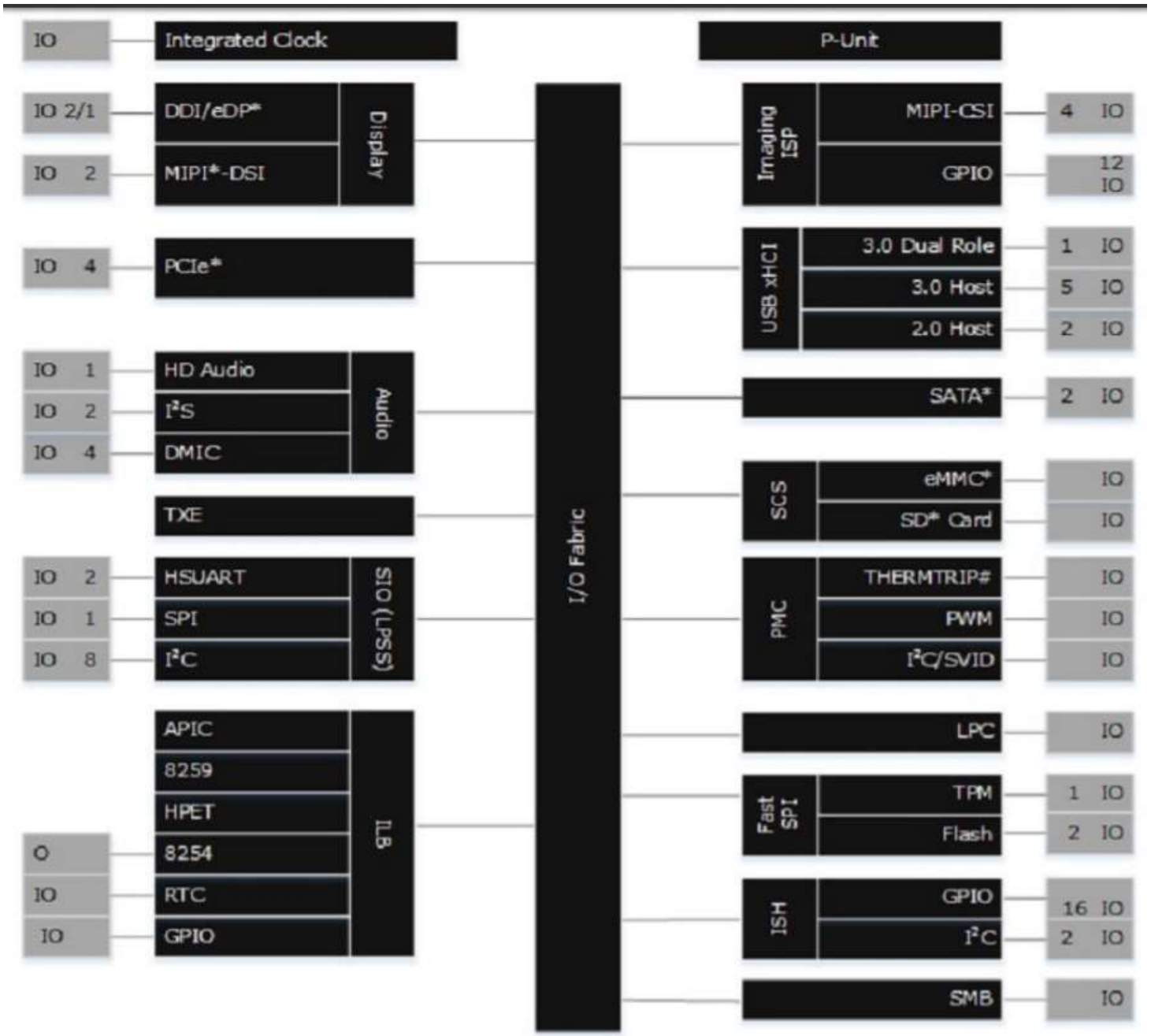
3.5 The Apollo Lake platform (7)

Main features of the Apollo Lake platform

	Braswell		Apollo Lake	
Launched	Q1/2015		Q3/2016	
Focus	Entry-level DTs	Notebooks/Convertibles	Entry level DTs	Notebooks/Convertibles
Processor	Braswell		Apollo Lake	
Models	J3710/J3160/J3060	N3710/N3700/ N3160/N3150/N30xx	J4205/J3455/J3355	N4200/N3400/N3300
Technology	14 nm		14 nm	
Die size				
No. of trans.				
Micro-arch.	Airmont		Goldmont	
32/64-bit	64-bit		64-bit	
No. of cores	2C/4C		2C/4C	
HT	no		no	
fc [GHz]	Up to 1.6 GHz		Up to 2.0 GHz	1.1 GHz
L2	1 MB/2cores		1 MB/2 cores	
No. of mem.ch.	Dual channels (64-bit)		Dual channel (64-bit)	
Memory up to	DDR3L-1600 LPDDR4-2400		DDR4-2400 LPDDR4-2400	
GPU	Gen. 8 LP		Gen. 9 LP HD 505	
DX	DX 11.1		DX 12.0	
GPU clock (base)	Up to 400 MHz		250 MHz	200 MHz
ISP	ISP			
Display output	eDP, DP, HDMI		eDP, DP, HDMI, MIPI-DSI	
Proc. TDP	≤ 6.5 W	≤ 6 W	10 W	6 W
FSB	--		--	
Socket	FCBGA1170		FCBGA1296	
Chipset	no, SoC		No, SOC	
OS	Windows 7 (32/64-bit) Windows 8.1 (64-bit) Windows 10 (64-bit)		Windows 10 (64-bit)	

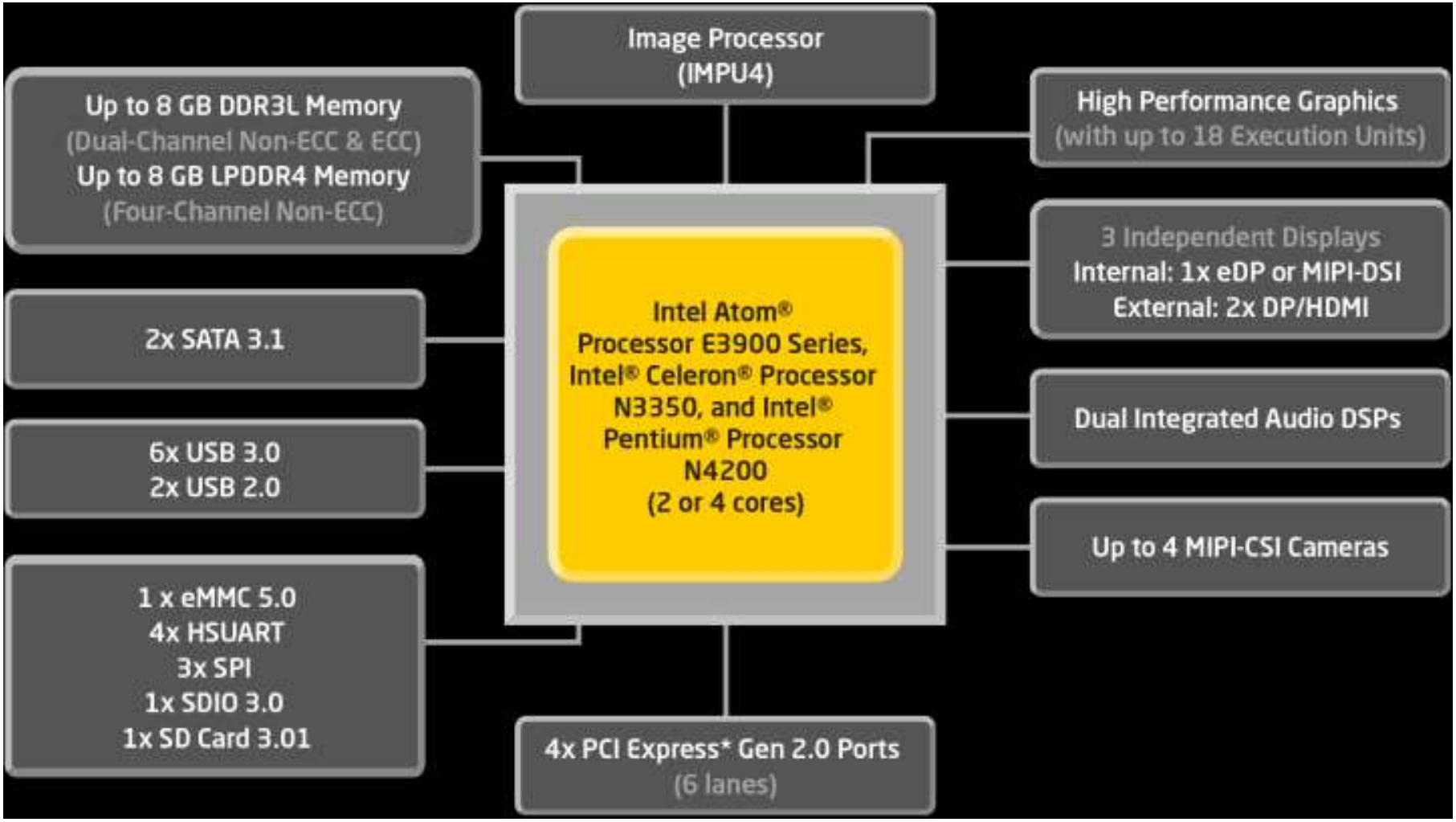
3.5 The Apollo Lake platform (8)

Block diagram of Intel's Apollo Lake processors targeting desktops and notebooks [157]



3.5 The Apollo Lake platform (9)

Block diagram of a platform based on Intel's Apollo Lake SoC [158]



3.8 The Gemini Lake platform

3.8 The Gemini Lake platform

- Launched: 12/2017.
  - Based on the 14 nm Goldmont Plus CPU.
  - L2 cache size increased from 1 MB/2 cores (Goldmont CPU) to 2 MB/2 cores (Goldmont Plus CPU).
  - It provides a low-power platforms for inexpensive entry level desktops and notebooks (or in a wider interpretation mobile computers).
- It runs under Windows 10.

3.8 The Gemini Lake platform (2)

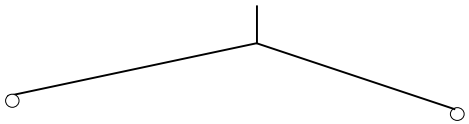
Contrasting selected features of the Gemini Lake and the Apollo Lake lines [159]

Intel Gemini Lake vs Apollo Lake		
Desktop	Gemini Lake: Pentium Silver J5005	Apollo Lake: Pentium J4205
uArch	**Goldmont+**	Goldmont
Cores	4	4
Base CPU	1.5 GHz	1.5 GHz
Turbo CPU	**2.8 GHz**	2.6 GHz
Cache	**4 MB**	2 MB
iGPU	**UHD 605**	UHD 505
EUs	18	18
Turbo iGPU	800 MHz	800 MHz
TDP	10W	

3.8 The Gemini Lake platform (3)

Differentiation of Intel's J and N series Gemini-Lake processors

Gemini Lake processors targeting entry level DTs and notebooks



J-series	**N-series**
Targeting entry level DTs	Targeting notebooks and convertibles
Pentium Silver J5005 Celeron J4100/J4005	Celeron N4100/N4000
(Windows 10 (64-bit)	(Windows 10 (64-bit)

3.8 The Gemini Lake platform (4)

Key features of Intel's Gemini Lake processors targeting entry level DTs [160]

	INTEL® PENTIUM® SILVER PROCESSOR J5005	INTEL® CELERON® PROCESSOR J4105	INTEL® CELERON® PROCESSOR J4005
Max Processor Frequency	Up to 2.8GHz	Up to 2.5GHz	Up to 2.7GHz
Number of Processors Core/Thread	4/4	4/4	2/2
Cache Size (MB)	4MB	4MB	4MB
Number of Memory Channels	2	2	2
Memory Type	DDR4-2400, LPDDR4-2400	DDR4-2400, LPDDR4-2400	DDR4-2400, LPDDR4-2400
Graphics Dynamic Frequency (GHz)	Up to 800MHz	Up to 750MHz	Up to 700MHz
Intel UHD Graphics	Intel® UHD Graphics 605	Intel® UHD Graphics 600	Intel® UHD Graphics 600

3.8 The Gemini Lake platform (5)

Key features of Intel's Gemini Lake processors targeting notebooks [160]

PENTIUM® SILVER AND CELERON® MOBILE

	INTEL® PENTIUM® SILVER PROCESSOR N5000	INTEL® CELERON® PROCESSOR N4100	INTEL® CELERON® PROCESSOR N4000
Max Processor Frequency	Up to 2.7GHz	Up to 2.4GHz	Up to 2.6GHz
Number of Processors Core/Thread	4/4	4/4	2/2
Cache Size (MB)	4MB	4MB	4MB
Number of Memory Channels	2	2	2
Memory Type	DDR4-2400, LPDDR4-2400	DDR4-2400, LPDDR4-2400	DDR4-2400, LPDDR4-2400
Graphics Dynamic Frequency (GHz)	Up to 750MHz	Up to 700MHz	Up to 650MHz
Intel UHD Graphics	Intel® UHD Graphics 605	Intel® UHD Graphics 600	Intel® UHD Graphics 600

3.8 The Gemini Lake platform (6)

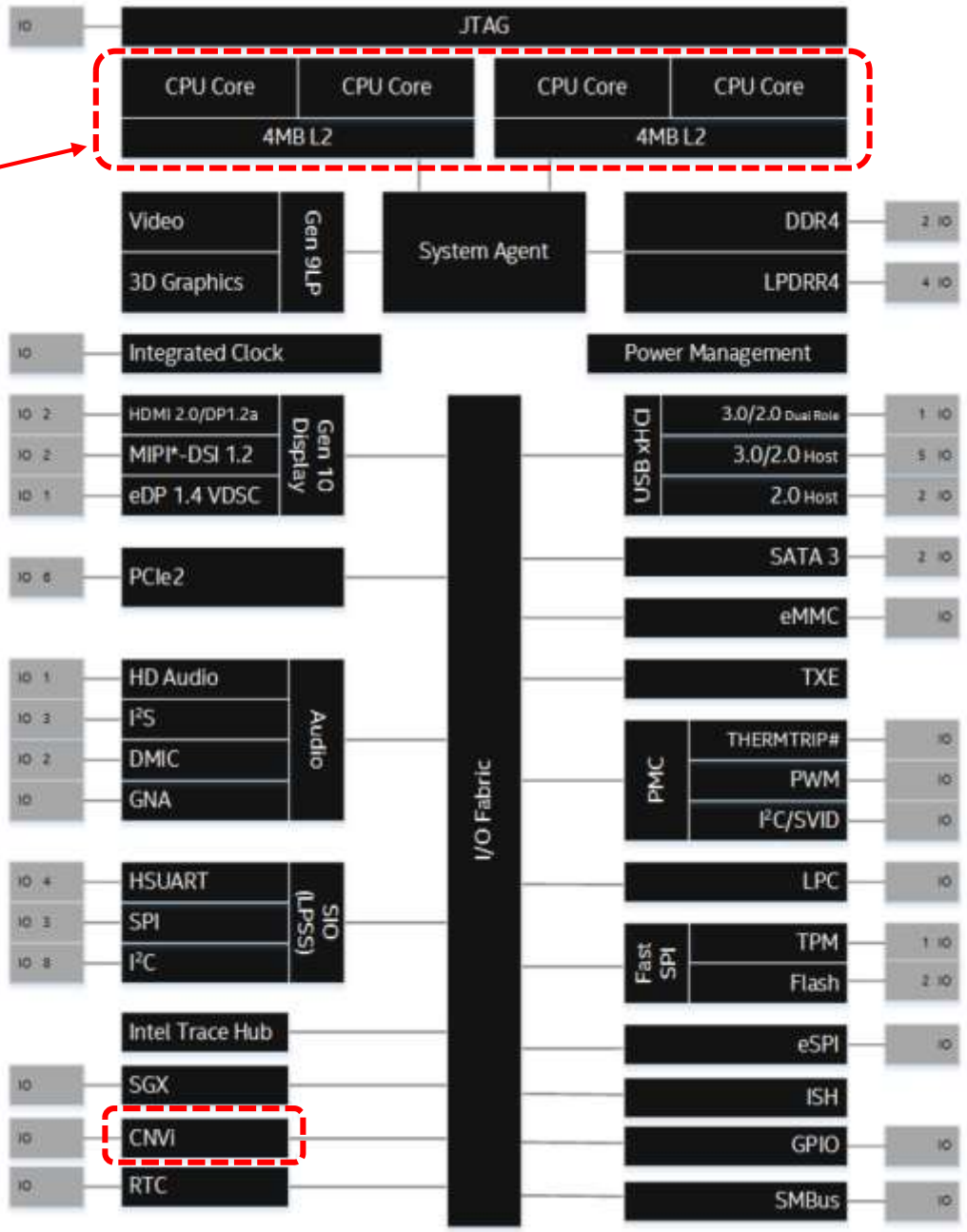
Main features of the Gemini Lake platform

	Apollo Lake		Gemini Lake	
Launched	Q3/2016		12/2016	
Focus	Entry level DTs	Notebooks/Convertibles	Entry level DTs	Notebooks/Convertibles
Processor	Apollo Lake		Gemini Lake	
Models	J4205/J3455/J3355	N4200/N3400/N3300	J5005/J4105/J4005	N5000/N4100/N4000
Technology	14 nm		14 nm	
Die size				
No. of trans.				
Micro-arch.	Goldmont		Goldmont Plus	
32/64-bit	64-bit		64-bit	
No. of cores	2C/4C		2C/4C	
HT	no		no	
fc [GHz]	Up to 2.0 GHz	1.1 GHz	Up to 2.0 GHz	1.1 GHz
L2	1 MB/2 CPU coress		1 MB/2 CPU cores?	
No. of mem.ch.	Dual channel		Dual channel	
Memory up to	DDR3L-1600 LPDDR4-2400		DDR4-2400 LPDDR4-2400	
GPU	Gen. 9 LP HD 505		Gen. 9 LP UHD 605/600	
DX				
GPU clock (base)	250 MHz	200 MHz	250 MHz	200 MHz
ISP				
Display output	eDP, DP, HDMI, MIPI-DSI		eDP, DP, HDMI, MIPI-DSI	
Proc. TDP	10 W	6 W	10 W	6 W
FSB	--		--	
Socket	FCBGA1296		FCBGA1090	
Chipset	No, SOC		No, SOC	
OS	Windows 10 (64-bit)		Windows 10 (64-bit)	

3.8 The Gemini Lake platform (7)

Block diagram of the Gemini Lake processor [161]

Probably there is a mistake and all 4 CPU cores share a single 4 MB L2 cache or there are two dual-core modules where both cores of a module share a 2 MB L2 cache.



3.8 The Gemini Lake platform (8)

CNVi (Connectivity Integration Architecture) [162]

- It is an important I/O-related extension introduced by Intel along with the Gemini Lake and Coffee Lake processors.
- With CNVi selected functional blocks of an RF chip (supporting WiFi and BT) will either be integrated into the main processor (in the case of the low-cost Gemini Lake chip) or on the accompanying PCH (in the case of the mainstream/high-end Coffee Lake).
- The remaining functional units (e.g. AD/DAs or baseband filters are implemented on a Companion RF (CRF) module.
- This reduces the bill of material (BoM) cost, power consumption and size.

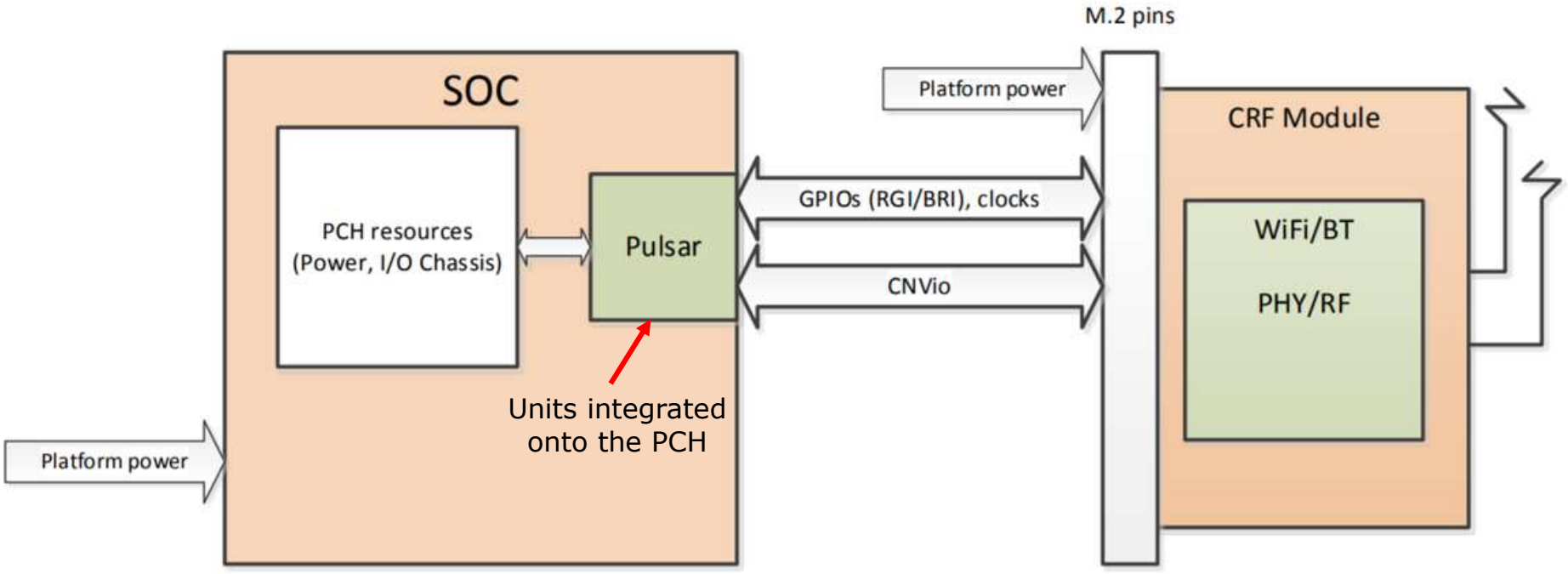
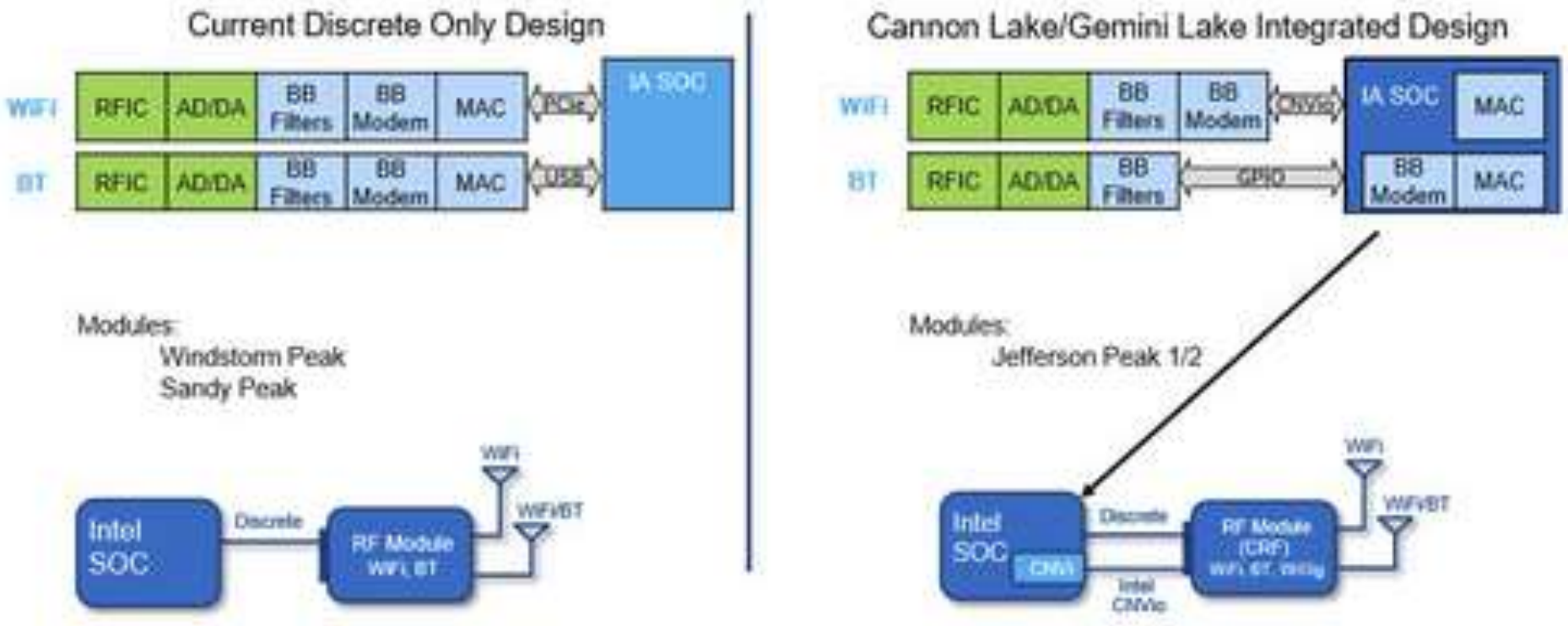


Figure: Partial integration of an RF chip on a PCH (in case of the Coffee Lake processor) [162]

3.8 The Gemini Lake platform (9)

Principle of integrating parts of the RF chip (WiFi and BT) on the CPU die [163]



- In case of WiFi only the Media Access Control (MAC) hardware will be integrated into the CPU chip, the baseband modem/filters and analog components will remain in a standalone module.
- The Bluetooth integration is tighter, both the Bluetooth MAC and the baseband modem will be integrated into the chip, whereas the baseband filters and RF components will remain outside of the chip in a separate module [163].

3.8 The Gemini Lake platform (10)

The CRF module [164]

Intel provides CRF modules (e.g. the Wireless-AC 9560) in two formats:

- either as an M2 card
- or a compact bridge chip

as shown below.

Figure: CRF modules implemented on an M2 card or as a compact bridge chip [164]

3.8 The Gemini Lake platform (11)

Main features of Gemini Lake processors [159]

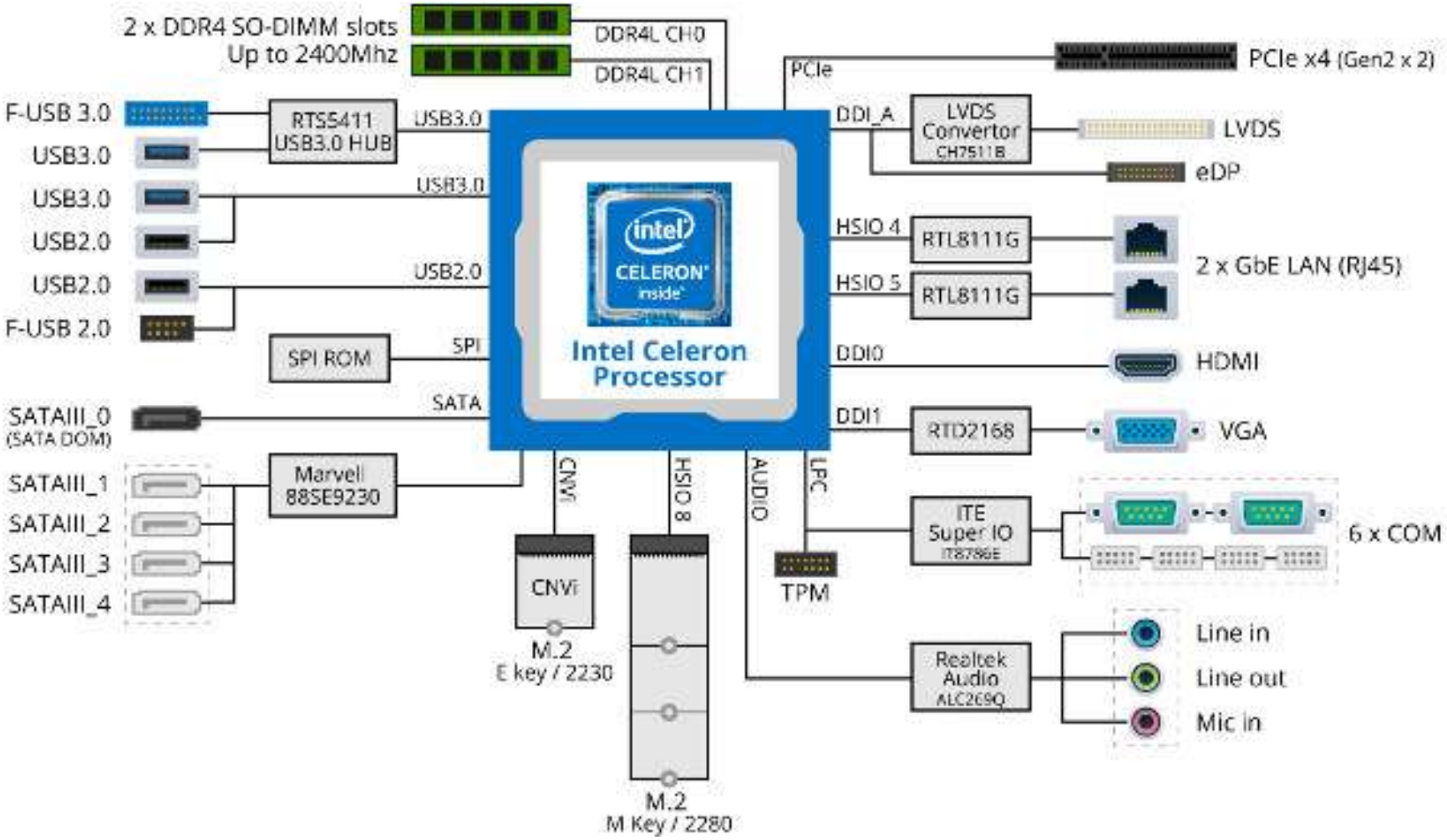
Gemini Lake Lineup						
	Desktop J-Series			Mobile N-Series		
	Pentium Silver J5005	Celeron J4105	Celeron J4005	Pentium Silver N5000	Celeron N4100	Celeron N4000
Cores	4		2	4		2
Base CPU	1.5 GHz	1.5 GHz	2.0 GHz	1.1 GHz	1.1 GHz	1.1 GHz
Turbo CPU	2.8 GHz	2.5 GHz	2.7 GHz	2.7 GHz	2.4 GHz	2.6 GHz
Cache	4 MB					
CPU uArch	Goldmont Plus					
iGPU	UHD 605	UHD 600		UHD 605	UHD 600	
iGPU EUs	18	12		18	12	
iGPU Freq	800	750	700	750	700	650
TDP	10 W			6.5 W		
SDP	-			4.8 W		
RAM	128-bit DDR4/LPDDR3/LPDDR4 memory controller, up to 2400 MT/s, up to 8 GB					
PCIe 2.0	6 Lanes					
Packaging	FCBGA1090 25×24 mm					
Tray Price	$161	$107	$107	$161	$107	$107

3.8 The Gemini Lake platform (12)

Presumed die shot of the Gemini processor [165]

3.8 The Gemini Lake platform (13)

Block diagram of a Mini-ITX motherboard powered by an Gemini Lake processor [166]



It is actually the block diagram of the Gigabyte MZGLKAI motherboard.

3.8 The Gemini Lake platform (14)

View of a Gemini Lake proc. powered Mini-ITX motherboard (Gigabyte MZGLKAI) [166]

4. Atom-based platforms targeting tablets

- 4.1 Introduction and overview of Intel's Atom-based platforms targeting tablets
- 4.2 The Menlow platform
- 4.3 The Oak Trail platform
- 4.4 The Clover Trail platform
- 4.5 The Clover Trail+ platform as used for tablets
- 4.6 The Bay Trail-T platform
- 4.7 The Cherry Trail platform

4.1 Introduction and overview of Intel’s Atom-based platforms targeting tablets

4.1 Introduction and overview of Intel's Atom-based platforms targeting tablets

4.1 Introduction to Atom-based platforms targeting tablets (2)

Emergence of tablets

Visioning tablets

Tablets were envisioned by Steve Jobs already in 1983 saying

> ”Apple’s strategy is really simple. What we want to do is we want to put an incredibly great computer in a book that you can carry around with you and learn how to use in 20 minutes.
>
> ... And we really want to do it with a radio link in it so you don’t have to hook up to anything and you’re in communication with all of these larger databases and other computers” [107].

4.1 Introduction to Atom-based platforms targeting tablets (3)

Designs leading to rapid spreading of tablets around 2010

From 2009 on: Android-based tablets arrived the market from many vendors.

2010: Apple's iPad with 9.7 " touch screen and Wi-Fi or additionally wireless 3G broadband internet connection (mobile internet connection), operating under iOS [108].

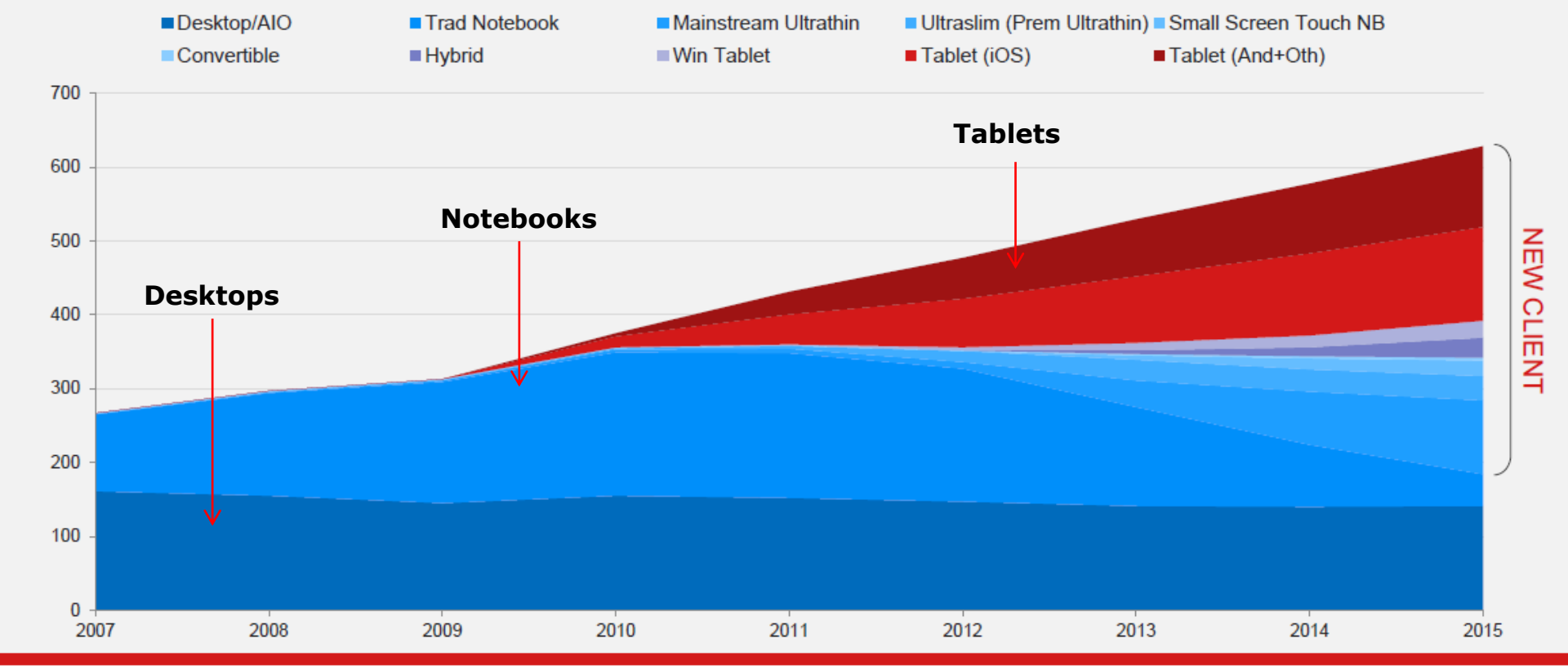
Figure: Steve Jobs introducing the iPad in 2010 [107]

Implementation alternatives of tablets [35]

4.1 Introduction to Atom-based platforms targeting tablets (5)

Rapid increase of tablet sales in the first half of the 2010's

Besides smartphones, touchscreen tablets including a number of design alternatives that provide partly also keyboard/mouse input (like convertibles and hybrids) have recently the highest growth potential, as indicated in the Figure below (12/1012) [4].

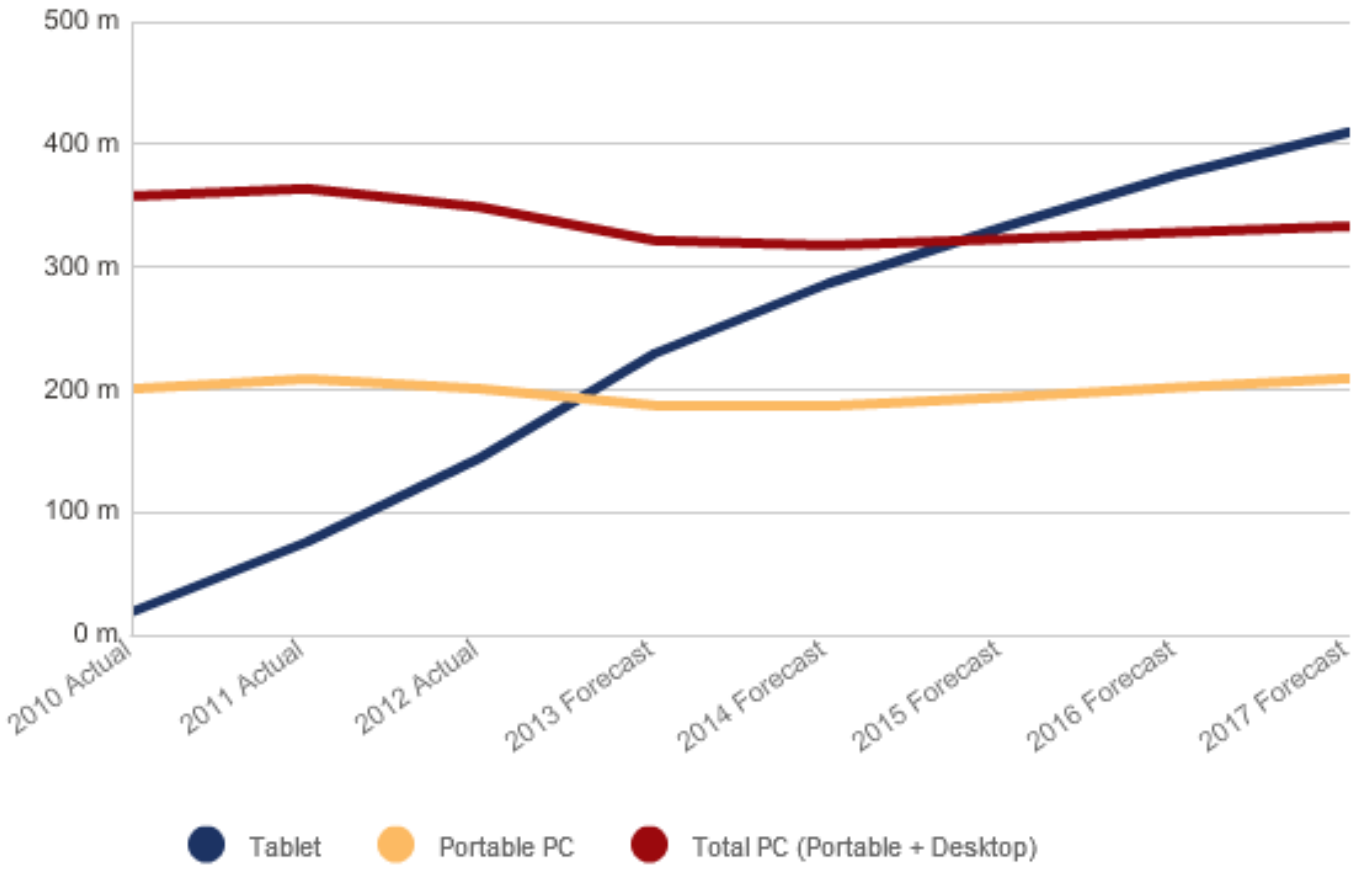


Sources: IDC AMD Extended Forecast Client World Wide by Country March 2013, IDC AMD Extended Forecast Tablet December 2012

Figure: Yearly worldwide sales figures of desktops, notebooks and tablets [4]

4.1 Introduction to Atom-based platforms targeting tablets (6)

Worldwide tablet and PC (portable and desktop) sales [109]



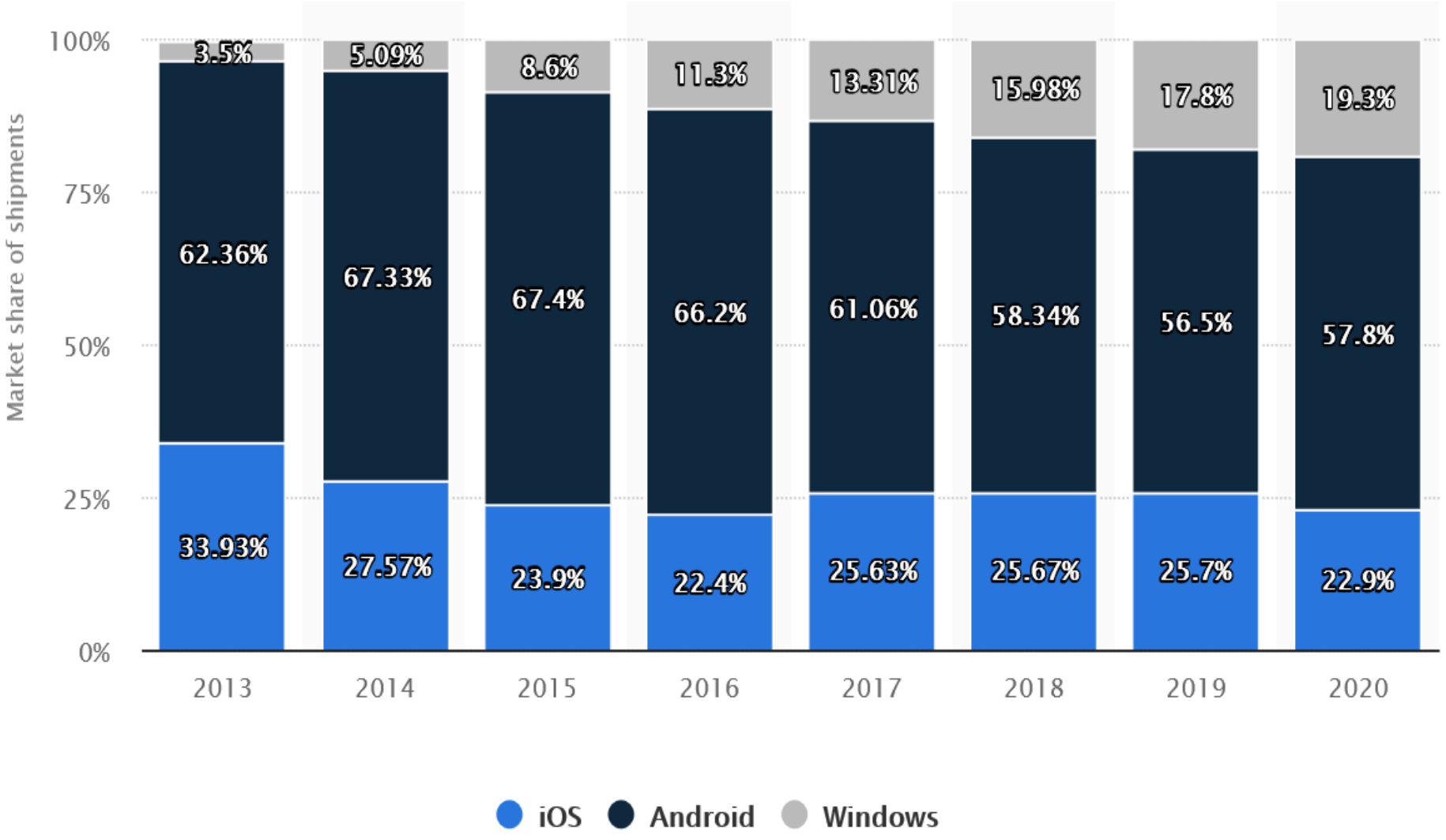
4.1 Introduction to Atom-based platforms targeting tablets (7)

2016 worldwide tablet shipments (in million units) and market shares by vendors [167]

Vendor	2Q16 Unit Shipments	2Q16 Market Share	2Q15 Unit Shipments	2Q15 Market Share	Year-Over-Year Growth
1. Apple	10.0	25.8%	11.0	24.9%	-9.2%
2. Samsung	6.0	15.6%	8.0	18.2%	-24.5%
3. Lenovo	2.5	6.6%	2.5	5.6%	3.1%
4. Huawei	2.2	5.6%	1.3	2.9%	71.0%
5. Amazon	1.6	4.0%	0.1	0.3%	1208.9%
Others	16.4	42.4%	21.3	48.2%	-22.9%
Total	38.7	100.0%	44.1	100.0%	-12.3%

4.1 Introduction to Atom-based platforms targeting tablets (8)

Global market share of tablet OSs 2013-2017 and forecast until 2020 [168]



4.1 Introduction to Atom-based platforms targeting tablets (9)

Intel's worldwide market share in tablet application processors [190], [191], [192]

Intel 's subsidies paid for OEMs

- In the first years of 2010 Intel paid significant subsidies (~ 50 $/tablet) to netbook and tablet manufacturers to achieve their switch from ARM based processors to x86 Atom processors.

Achieved market share e.g. in 1Q/2015 due to paying subsidies

- In 1Q/2015 Intel achieved the 3. place in the worldwide market share in tablet application processor revenue, as the Table below shows.

Tablet application processors worldwide market share 1Q/2015 (revenue) [193]	
Apple (USA)	28 %
Qualcomm (USA)	16 %
Intel (USA)	14 %
MediaTek (Taiwan)	
Samsung (S. Korea)	

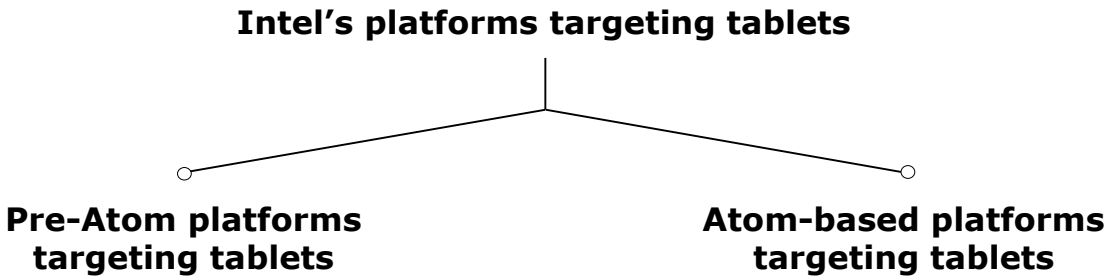
Table: Worldwide market share of application processors used in tablets in 1Q/2015 (based on revenue) [193]

Subsidy: szubvenció

*

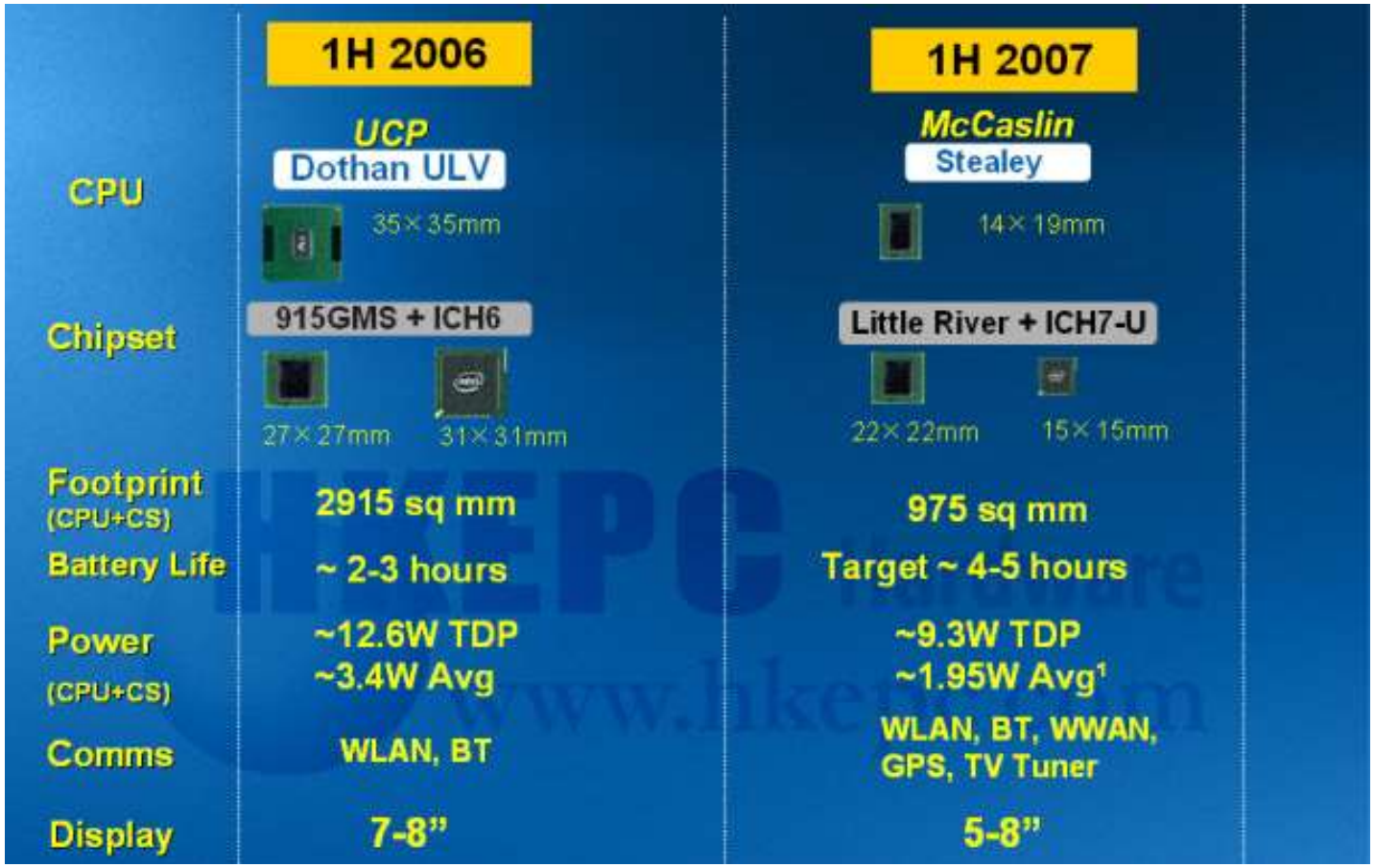
4.1 Introduction to Atom-based platforms targeting tablets (10)

Intel's platforms targeting tablets



4.1 Introduction to Atom-based platforms targeting tablets (11)

Intel's pre-Atom platforms targeting tablets [83]



4.1 Introduction to Atom-based platforms targeting tablets (12)

Remark

The UCP platform included 32-bit Pentium M Dothan (2. core) ULV (Ultra Low Voltage) processors whereas
the McCaslyn platform made use of 32-bit Pentium M Dothan derived processors, designated as A100/A110 (Stealy processors).

All these processors were manufactured by 90 nm technology.

Main features of the UCP and McCaslin platforms [84]

UMPC Platform Comparison

Feature	UCP	McCaslin
Processor	Intel® Celeron® M Processor ULV	Stealey
Frequency	900MHz	800MHz, 600MHz
L2 Cache	512K	512K
Advanced Technologies Capability	Execute Disable Bit	Enhanced Intel SpeedStep® Technology Deeper Sleep Support (C4) Execute Disable Bit
Footprint (CPU+CS)	2915mm²	975mm²
Battery Life	~ 2 - 3 hrs	Target 4 – 5 hrs
Platform Support	Mobile Intel 915 Express Chipset Family	Little River
Power (CPU & CS)	~12.6W TDP ~3.4W Avg	~9.3W TDP ~1.95W Avg[1]
Comms	WLAN, BT	WLAN, BT, WWAN, GPS, TV Tuner
LCD	7-8"	5-8"
Targeted Launch	Mar'06	April 18, 2007

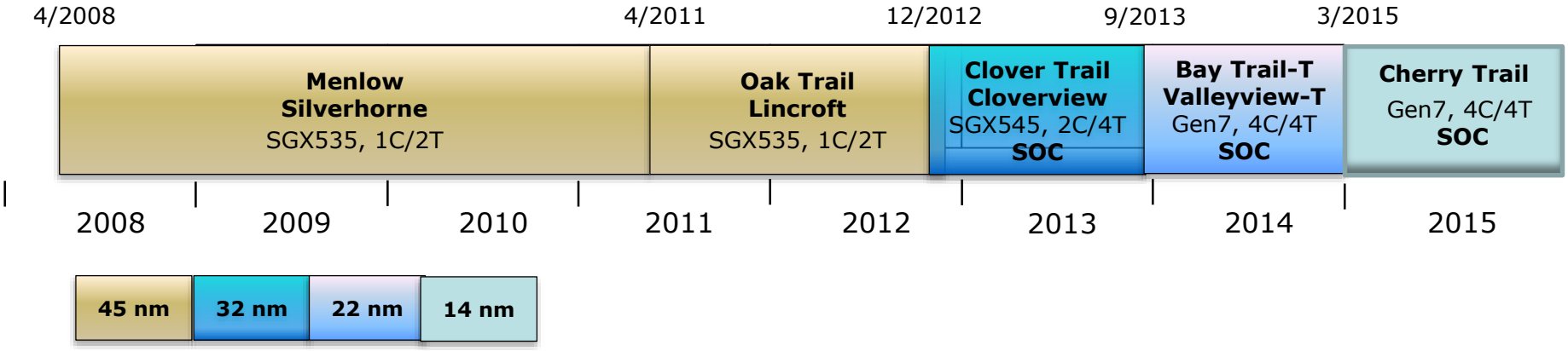
4.1 Introduction to Atom-based platforms targeting tablets (14)

Key features of the A100 and A110 processors [85]

Processor	A100	A110
Clock	600MHz	800MHz
FSB	400MHz	400MHz
Cache	512KB Level 2	512KB Level 2
TDP	3W	3W
Package	14x19mm	14x19mm

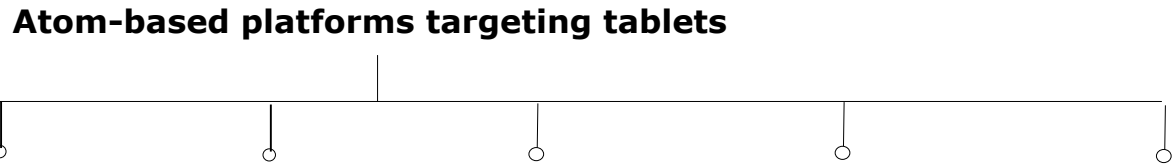
4.1 Introduction to Atom-based platforms targeting tablets (15)

Intel's Atom-based platforms (based on [86])



4.1 Introduction to Atom-based platforms targeting tablets (16)

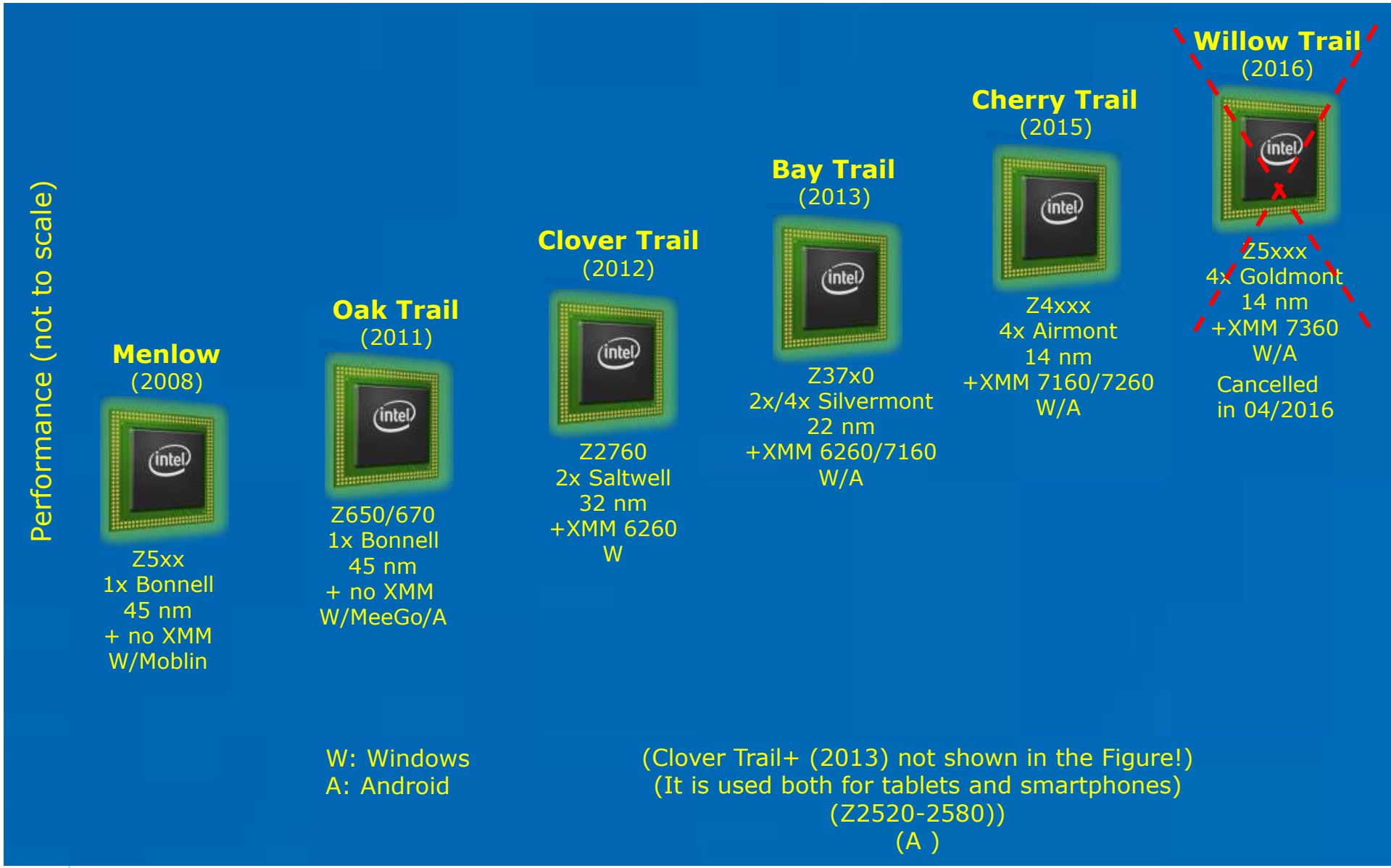
Overview of Atom-based platforms targeting tablets



	Menlow	Oak Trail	Clover Trail	Clover Trail+	Bay Trail-T	Cherry Trail
Intro.	04/2008	04/2011	09/2012	02/2013	Q1/2014	03/2015
Proc.	Silverthorne	Lincroft	Cloverview	Cloverview	Valleyview-T	x5/x7
Techn.	45 nm	45 nm	32 nm	32 nm	22 nm	14 nm
Microarch.	Bonnell	Bonnell	Saltwell	Saltwell	Silvermont	Airmont
32/64-bit	32-bit	32-bit	32-bit	32-bit	64-bit	64-bit
No. of cores	1C	1C/2C	2C	2C	2C/4C	4C
Chipset	U515W	SM35	SOC	SOC	SOC	SOC
OS	Windows XP Windows Vista Windows 7 Moblin 1	Windows 7 Home Premium MeeGo Android	Windows 8 Pro Windows 8	Android 4.2	Windows 8.1 CS Android 4.4.2	Windows 10 Home 64-bit Android 5.1

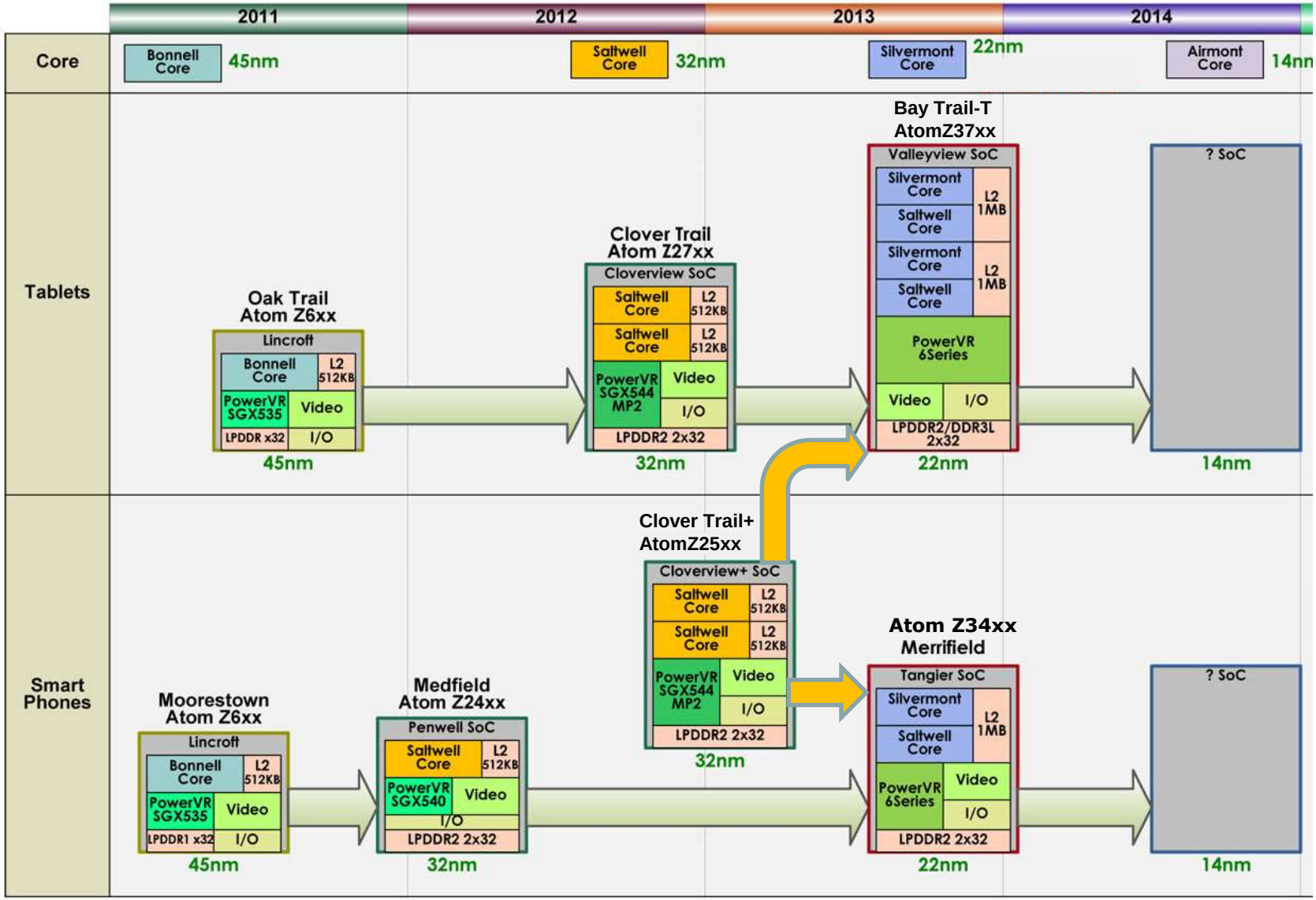
4.1 Introduction to Atom-based platforms targeting tablets (17)

Intel's platforms targeting tablets (based on [43])



4.1 Introduction to Atom-based platforms targeting tablets (18)

Overview of Intel's tablet and smartphone platforms (without the Menlow and Cherry Trail platform) [110]



4.1 Introduction to Atom-based platforms targeting tablets (19)

Main features of Intel's Atom based tablet platforms -1

	Menlow	Oak Trail	Clover Trail	Clover Trail+	Bay Trail -T
Available	04/2008	04/2011	12/2012	02/2013	Q9/2013
Focus	MIDs	Tablets	Tablets	Smartphones/tablets	Tablets
Processor	Silverthorne	Lincroft	Cloverview	Cloverview	Valleyview -T
Models	Z5xx	Z650/Z670	Z2760	Z2520-Z2580	Z36xx, Z37xx(D)
Technology	45nm	45nm	32nm	32nm	22nm
Die size	26 mm^2	65 mm2	64 mm2		
No. of trans.	47 mtrs	140 mtrs	432 mtrs		
Micro-arch.	Bonnell	Bonnell	Saltwell	Saltwell	Silvermont
32/64-bit	32-bit	32-bit	32-bit	32-bit	64-bit
1C/2C	1C	1C	2C	2C	2C/4C
HT	HT	HT	HT	HT	no HT
fc [GHz]	0.8-2.13	1.20/1.25	1.50 (1.80 Turbo)	Up to 1.2-2.0 (Turbo)	Up to 1.83-2.41 (Turbo)
L2	512 kB	512 kB	2x512 kB	2x512 kB	2x1 MB
No. of mem.ch.	Single channel MC on SCH	Single channel MC on proc. die (32-bit)	Dual channels MC on proc. die (32-bit)	Dual mem. ch. MC on proc. die (32-bit)	Single/dual mem. channels MC on proc. die (64-bit)
Memory	DDR2-533/400	DDR2-800	LPDDR2-800 (POP)	LPDDR2-1066 (POP)	LPDDR3-1066
GPU	GMA 500 (SGX 535) in PCH (US15W)	GMA 600 (SGX 535) on the proc.	Power VR SGX 545 on the proc	Power VR SGX 544 MP2 on the proc.	Gen 7 DX11 on the proc.
DX	DX 9.0c	DX 9.0c	DX 9.0c	DX 9.x	DX 11
Camera res.	—	—	8 Mpixel	16 Mpixel	
ISP	—	—	ISP 2300	ISP	ISP
Display output	LVDS, SDVO on U515W	LVDS or MIPI-DSI on proc. HDMI 1.3a on SM35	HDMI 1.3a, MIPI-CSI,-2 MIPI-DSI, MIPI-HSI	HDMI 1.3a, MIPI-CSI,-2 MIPI-DSI, MIPI.HSI	HDMI 1.4a, DP 1.2, eDP1.3, MIPI_CSI, MIPI-DSI
GPU clock	400/533 Mb/s	400 MHz	533 MHz	300-533 MHz	
Proc. TDP	0.65-2.5 W	3.0 W	1.7W	2.0-3.0 W	2.0-2.4 W (SDP)
FSB	400/533 MT/s	400 MT/s per dir. cDMI (8-bit)	—	—	—
Socket	PBGA441	BGA 518	FC-MB4760	BGA 760	UTFCBGA1380
Chipset	U515W (Poulsbo)	SM 35 (Whitney Point)	no, SOC	no, SOC	no, SOC
OS	Windows XP/Vista/7 Moblin 1	Windows 7 Home Premium MeeGo, Android	Windows 8 Pro Windows 8	Android 4.2	Windows 8.1 CS (32-bit) Android 4.2.2
Examples	Beng S6 Compal KAX15 Lenovo ideapad U8	Fujitsu Q550 Intel Studybook prototype Motion Computing's CL900 tablet	Acer Iconia W3/W510 Asus VivoTab Dell Latitude 10 HP Envy x2/ElitePad 900 Lenovo Thinkpad Tablet 2 Samsung Series 5 Slate	Asus MeMO Pad FHD 10 / Fonepad Note / Transformer Book Trio Samsung Galaxy Tab3	Acer W3-810 Asus Transformer Book Trio T100 Dell Venue/ Midland Lenovo Miix 8/ Miix 2 Toshiba Encore

4.1 Introduction to Atom-based platforms targeting tablets (20)

Main features of Intel's Atom based tablet platforms -2

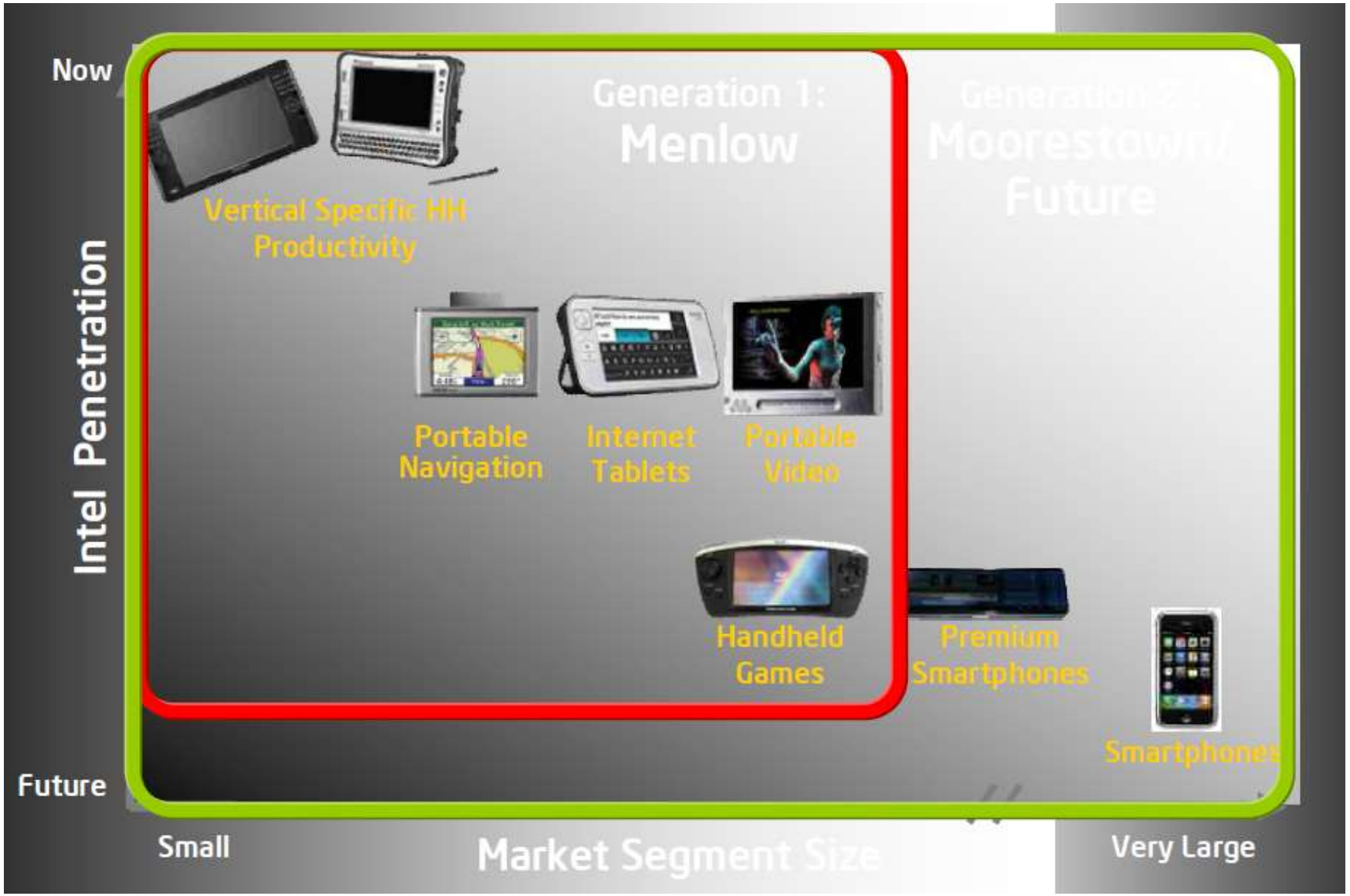
	Cherry Trail
Available	Q3/2015
Focus	Tablets
Processor	Valleyview -T
Models	X5-Z83xx/Z85xx, x7-Z87xx
Technology	14 nm
Die size	
No. of trans.	
Micro-arch.	Airmont
32/64-bit	64-bit
Core count	4C
HT	no HT
fc [GHz]	Up to 1.6 GHz
L2	1 MB/2 cores
No. of mem.ch.	Up to dual channels on proc. die (64-bit)
Memory	LPDDR3-1600
GPU	Gen 8-LP on the proc.
DX	DX 11.1
Camera res.	
ISP	ISP
Display output	HDMI 1.4b, DP 1.1a, eDP1.3, MIPI-DSI 1.01
GPU clock	200 MHz
Proc. TDP	2.0-2.4 W (SDP)
FSB	—
Socket	UTFCBGA1380
Chipset	no, SOC
OS	Windows 7/8/8.1/10 Android 5.1
Examples	HP ElitePad Microsoft Surface 3

4.2 The Menlow platform

4.2 The Menlow platform

- Announced: 4/2007
- First details about the Silverthorne processor disclosed at the ISSCC in 2/2008
- First Menlow based MID products (practically tablets): 4/2008
- Based on the 45 nm Bonnell CPU core, 32-bit ISA
- 2-chip implementation with the GPU placed onto the SCH (System Control Hub)
- Runs under Windows XP/Vista/Windows 7 and Moblin 1

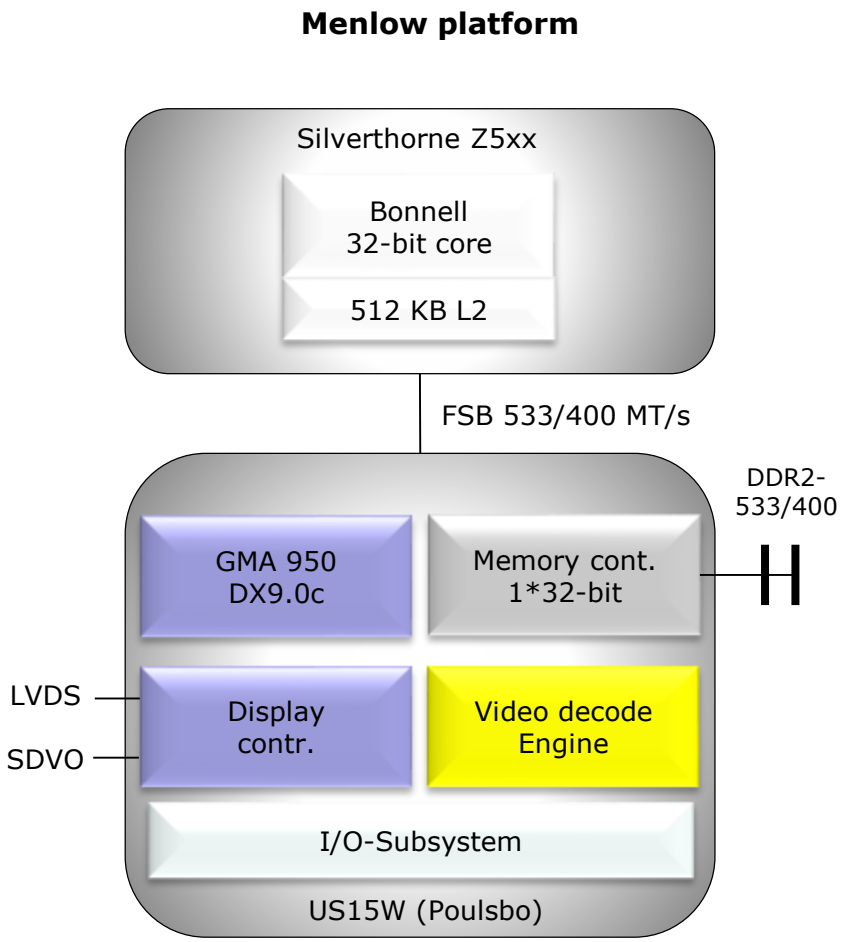
Target market segments of the Menlow platform [52]



Menlow-based MID devices (practically tablets) [87]

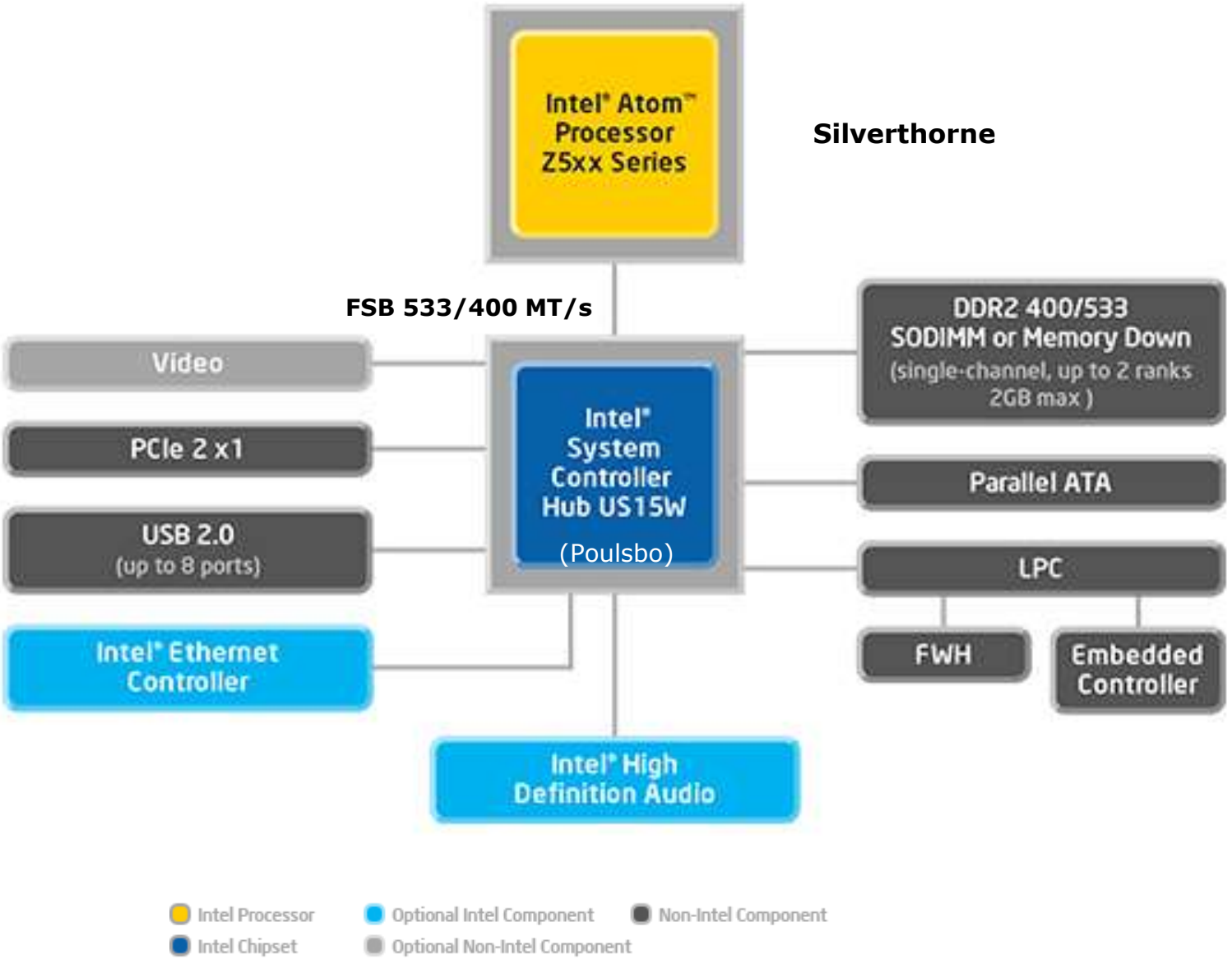
4.2 The Menlow platform (4)

Simplified block diagram of the Menlow platform

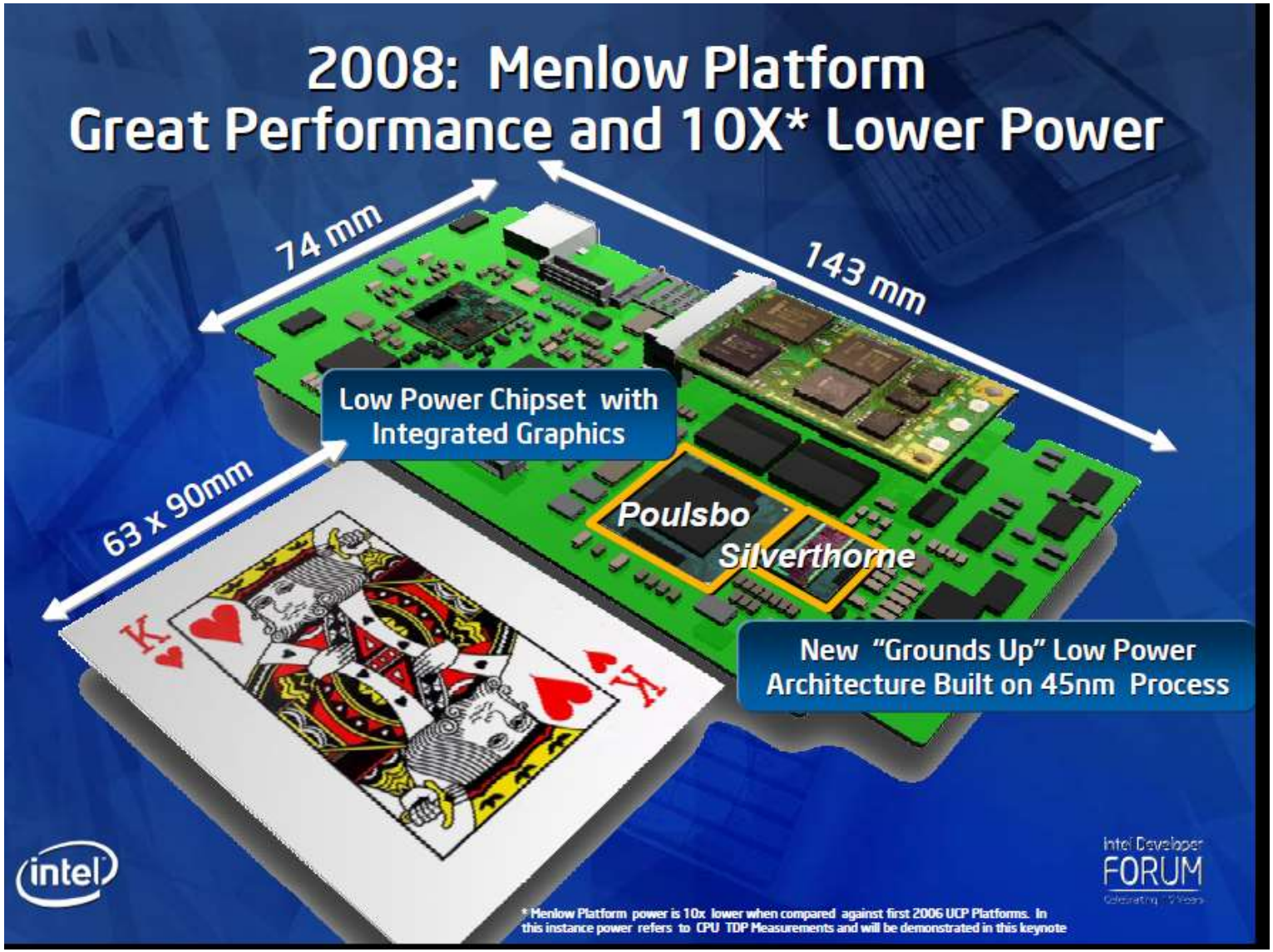


4.2 The Menlow platform (5)

Block diagram of the Menlow platform [88]



Example Menlow platform implementation [87]



Key features of the Silverthorne processor [52]

Intel® Atom™ Processor
(Formerly codenamed Silverthorne)

Intel's smallest processor built with the world's smallest transistors
- < 25 mm2 die size
- 13mm x 14mm x 1.6mm package
- Lead-free[1] and halide-free[2]
- 45nm High-K CMOS
- 47 million transistors

Drastic Power Reductions
- Intel's lowest power CPU
- 0.6-2.4 watts TdP[3]
- Low average power[4] (<220mW)
- Intel's Deep Power Down Technology (C6)
- Enhanced Intel Speed Step Technology
- Dynamic L2 Cache Sizing Supported

Fastest processor in sub 3W space
- 533MHz & 400MHz FSB
- HT Technology[3]
- Intel Digital Media Boost
- L2 Data Pre-fetcher
- Leading scores on industry benchmarks
- Outstanding web page rendering

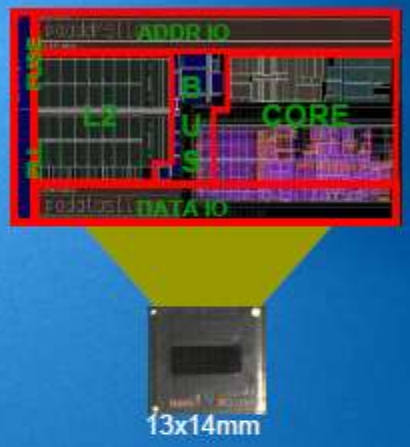
Ground Up Design with Partial Core 2 Duo (Merom) ISA Compatibility
- Intel Virtualization Technology
- Intel Advanced Thermal Manager
- Execute Disable Bit Support
- SSE3, SSSE3 Support

1. Intel 45nm product is manufactured on a lead-free process. Lead-free per EU RoHS Directive (2002/95/EC, Annex A). Some RoHS exemptions may apply to other components used in the product package.
2. Applies to components containing flame retardants & PVC only. Halogens are below 900 PPM bromine, 900 PPM chlorine, and 1500 PPM combined bromine and chlorine.
3. HT Technology can add 200mW of power above quoted TDP for HT SKUs when multi-threaded applications are run.
4. Average power is defined as measured CPU power whilst running BAPCo MobileMark'05 Office Productivity suite on Microsoft* Windows* XP for a period of 90min at 50°C .

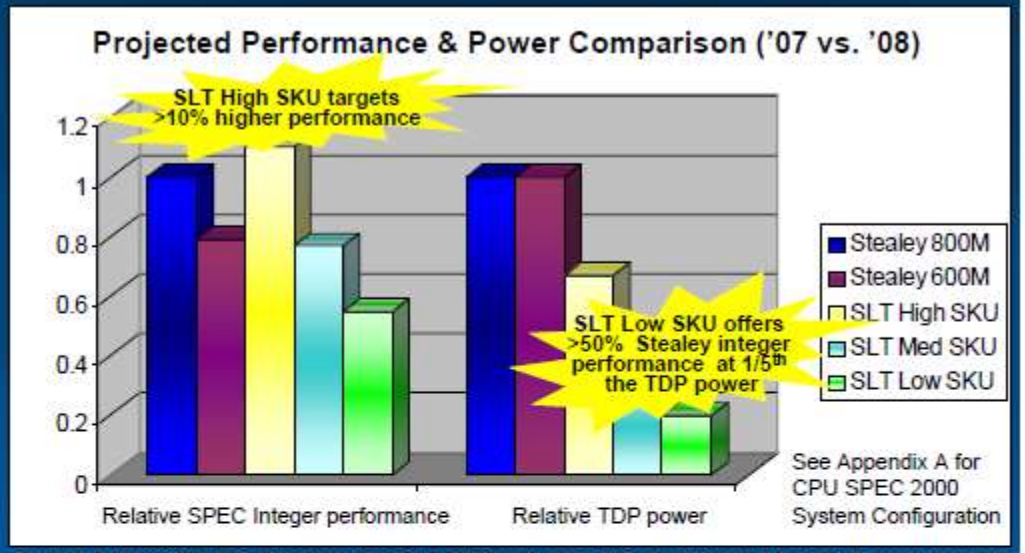
Performance and power improvements of the Silverthorne processor [99]

Intel Confidential

Silverthorne CPU



13x14mm



Source: Intel Q1'07 projection based on Pre-Si Silverthorne estimates. Stealey based on measured data

- New In-order execution simplifies design & reduces power
- Pipeline optimized to execute Macro-ops improves efficiency
- Multi-threading support can provide scalable performance and increased power / performance efficiency
- Silverthorne supports SSE3 which can improve performance on multimedia and gaming applications
- New sleep state (C6) and other architectural power management enhancements can improve battery life

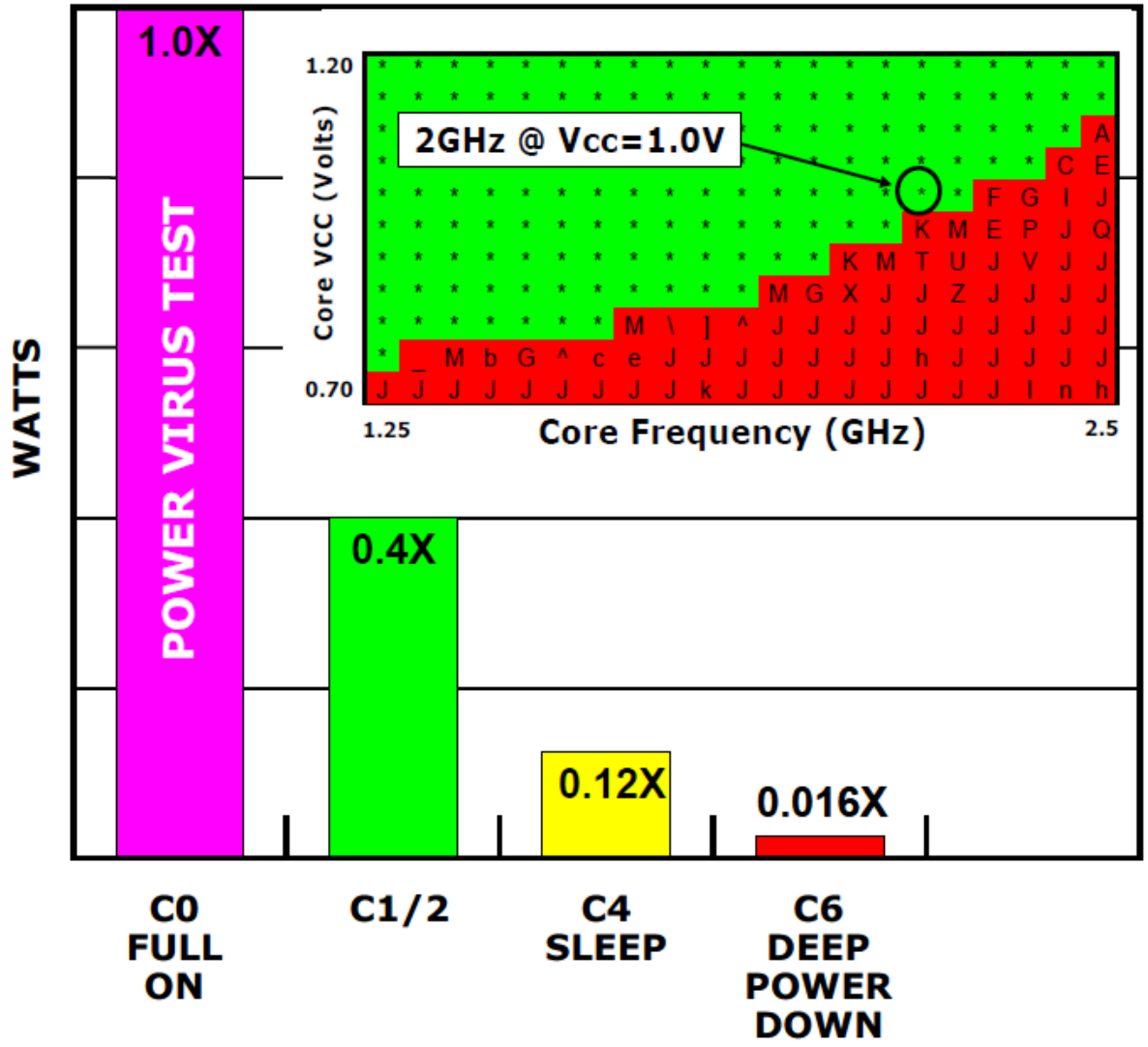
Silverthorne's efficient engine delivers Compelling Performance-per-Watt advantages for MID

1 Silverthorne (SLT) executes two instructions per clock

All plans, features and dates are preliminary and subject to change without notice

4.2 The Menlow platform (9)

C-state power consumption of the Bonnell CPU-based Silverthorne processor [47]



4.2 The Menlow platform (10)

Main features of the Menlow tablet platform

	Menlow	Oak Trail	Clover Trail	Clover Trail+	Bay Trail -T
Available	04/2008	04/2011	12/2012	02/2013	Q9/2013
Focus	MIDs	Tablets	Tablets	Smartphones/tablets	Tablets
Processor	Silverthorne	Lincroft	Cloverview	Cloverview	Valleyview -T
Models	Z5xx	Z650/Z670	Z2760	Z2520-Z2580	Z36xx, Z37xx(D)
Technology	45nm	45nm	32nm	32nm	22nm
Die size	26 mm^2	65 mm2	64 mm2		
No. of trans.	47 mtrs	140 mtrs	432 mtrs		
Micro-arch.	Bonnell	Bonnell	Saltwell	Saltwell	Silvermont
32/64-bit	32-bit	32-bit	32-bit	32-bit	64-bit
1C/2C	1C	1C	2C	2C	2C/4C
HT	HT	HT	HT	HT	no HT
fc [GHz]	0.8-2.13	1.20/1.25	1.50 (1.80 Turbo)	Up to 1.2-2.0 (Turbo)	Up to 1.83-2.41 (Turbo)
L2	512 kB	512 kB	2x512 kB	2x512 kB	2x1 MB
No. of mem.ch.	Single channel MC on SCH	Single channel MC on proc. die (32-bit)	Dual channels MC on proc. die (32-bit)	Dual mem. ch. MC on proc. die (32-bit)	Single/dual mem. channels MC on proc. die (64-bit)
Memory	DDR2-533/400	DDR2-800	LPDDR2-800 (POP)	LPDDR2-1066 (POP)	LPDDR3-1066
GPU	GMA 500 (SGX 535) in PCH (US15W)	GMA 600 (SGX 535) on the proc.	Power VR SGX 545 on the proc	Power VR SGX 544 MP2 on the proc.	Gen 7 DX11 on the proc.
DX	DX 9.0c	DX 9.0c	DX 9.0c	DX 9.x	DX 11
Camera res.	–	–	8 Mpixel	16 Mpixel	
ISP	–	–	ISP 2300	ISP	ISP
Display output	LVDS, SDVO on U515W	LVDS or MIPI-DSI on proc. HDMI 1.3a on SM35	HDMI 1.3a, MIPI-CSI,-2 MIPI-DSI, MIPI-HSI	HDMI 1.3a, MIPI-CSI,-2 MIPI-DSI, MIPI.HSI	HDMI 1.4a, DP 1.2, eDP1.3, MIPI_CSI, MIPI-DSI
GPU clock	400/533 Mb/s	400 MHz	533 MHz	300-533 MHz	
Proc. TDP	0.65-2.5 W	3.0 W	1.7W	2.0-3.0 W	2.0-2.4 W (SDP)
FSB	400/533 MT/s	400 MT/s per dir. cDMI (8-bit)	–	–	–
Socket	PBGA441	BGA 518	FC-MB4760	BGA 760	UTFCBGA1380
Chipset	U515W (Poulsbo)	SM 35 (Whitney Point)	no, SOC	no, SOC	no, SOC
OS	Windows XP/Vista/7 Moblin 1	Windows 7 Home Premium MeeGo, Android	Windows 8 Pro Windows 8	Android 4.2	Windows 8.1 CS (32-bit) Android 4.2.2
Examples	Beng S6 Compal KAX15 Lenovo ideapad U8	Fujitsu Q550 Intel Studybook prototype Motion Computing's CL900 tablet	Acer Iconia W3/W510 Asus VivoTab Dell Latitude 10 HP Envy x2/ElitePad 900 Lenovo Thinkpad Tablet 2 Samsung Series 5 Slate	Asus MeMO Pad FHD 10 / Fonepad Note / Transformer Book Trio Samsung Galaxy Tab3	Acer W3-810 Asus Transformer Book Trio T100 Dell Venue/ Midland Lenovo Miix 8/ Miix 2 Toshiba Encore

4.2 The Menlow platform (11)

First introduced Silverthorne processor models [49]

	Clock Speed	TDP	Average Power	Idle Power (C6)	FSB	SMT	Price
Intel Atom Z500	800MHz	0.65W	160mW	80mW	400MHz	No	$45
Intel Atom Z510	1.1GHz	2W	220mW	100mW	400MHz	No	$45
Intel Atom Z520	1.33GHz	2W	220mW	100mW	533MHz	Yes	$65
Intel Atom Z530	1.60GHz	2W	220mW	100mW	533MHz	Yes	$95
Intel Atom Z540	1.86GHz	2.4W	220mW	100mW	533MHz	Yes	$160

Intel Solid State Disk implementation as a PoP package-1 [99]

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Intel PATA Solid State Disk[1]

- Intel PATA SSD solution for Menlow Platform
  - Storage Capacity: 2GB, 4GB, and 8GB (Q1 '09)
  - Performance and Power Targets[2]:
    - Read – 56MB / Write – 36MB
    - Power: ~20mw Idle ~200mw Stress
  - Target Package Size: 22x14x1.2mm
- Helps to achieve small form factor designs
- Designed to improve platform performance and battery life

Storage Based On Intel Advanced NAND Technology In Optimized Package For Small Designs

[1]Planning and Definition Phase POR expected in Q2'07
[2]Preliminary Data and Subject to Change

15

Intel Solid State Disk implementation as a PoP package-2 [99]

Updated slide

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What is Package-on-Package (PoP)?

DEFINITION

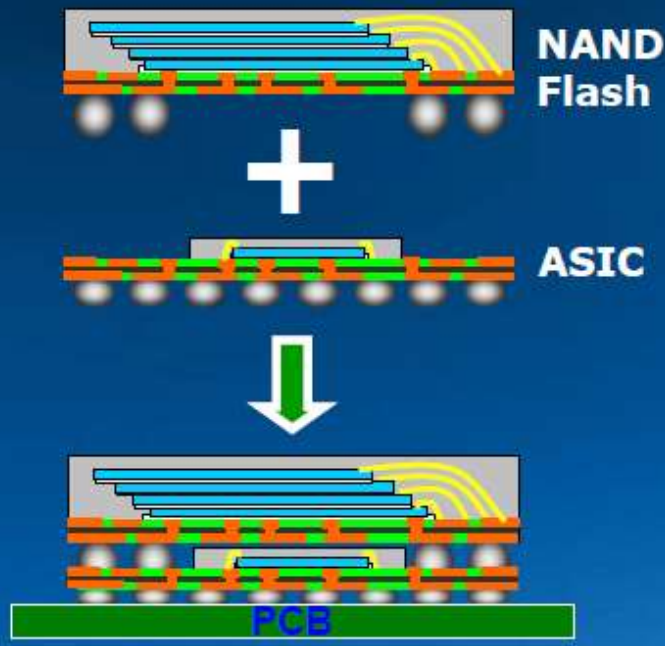
- Vertically integrates discrete logic and memory package: two separate packages, one BGA (ball grid array) resting on top of the other using a standard interface between them

ADVANTAGES

- Board space savings: smaller PCB footprint
- Product flexibility/reduced system level cost
- Simpler PCB design: easier signal routing
- Enhanced performance: improved signal integrity
- Higher product yield than single package

CERTIFIED

- Intel certified package technology (15x15mm)
- In HVM within cellular and handheld device industry



[1]Planning and Definition Phase POR expected in Q2'07
[2]Preliminary Data and Subject to Change

16

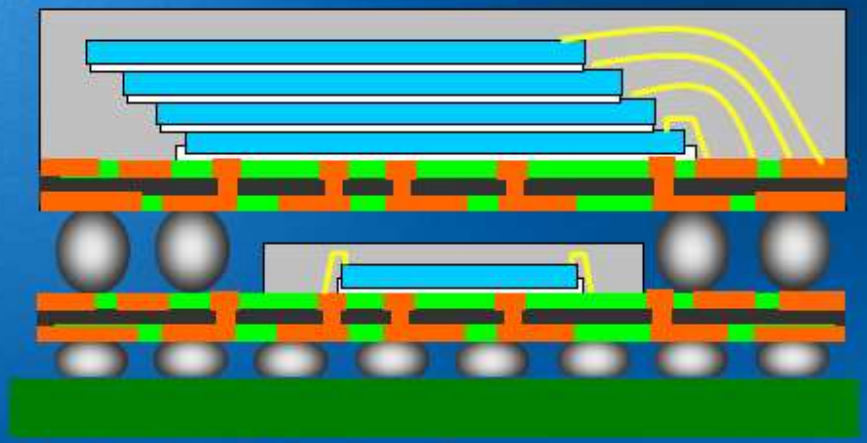
Intel Solid State Disk implementation as a PoP package-3 [99]

Updated slide

Intel Confidential

PoP Strategy for PATA On Motherboard (PoMB)

- **FIRST IMPLEMENTATION**
  - 2GB in 12x18x1.7mm
  - Schedule: ES Q3'07, QS Q4'07, PRQ Q1'08



NAND

Top Package Envelope
2GB, 4GB = 12x18
Up to 2x4 stacks

PATA Controller

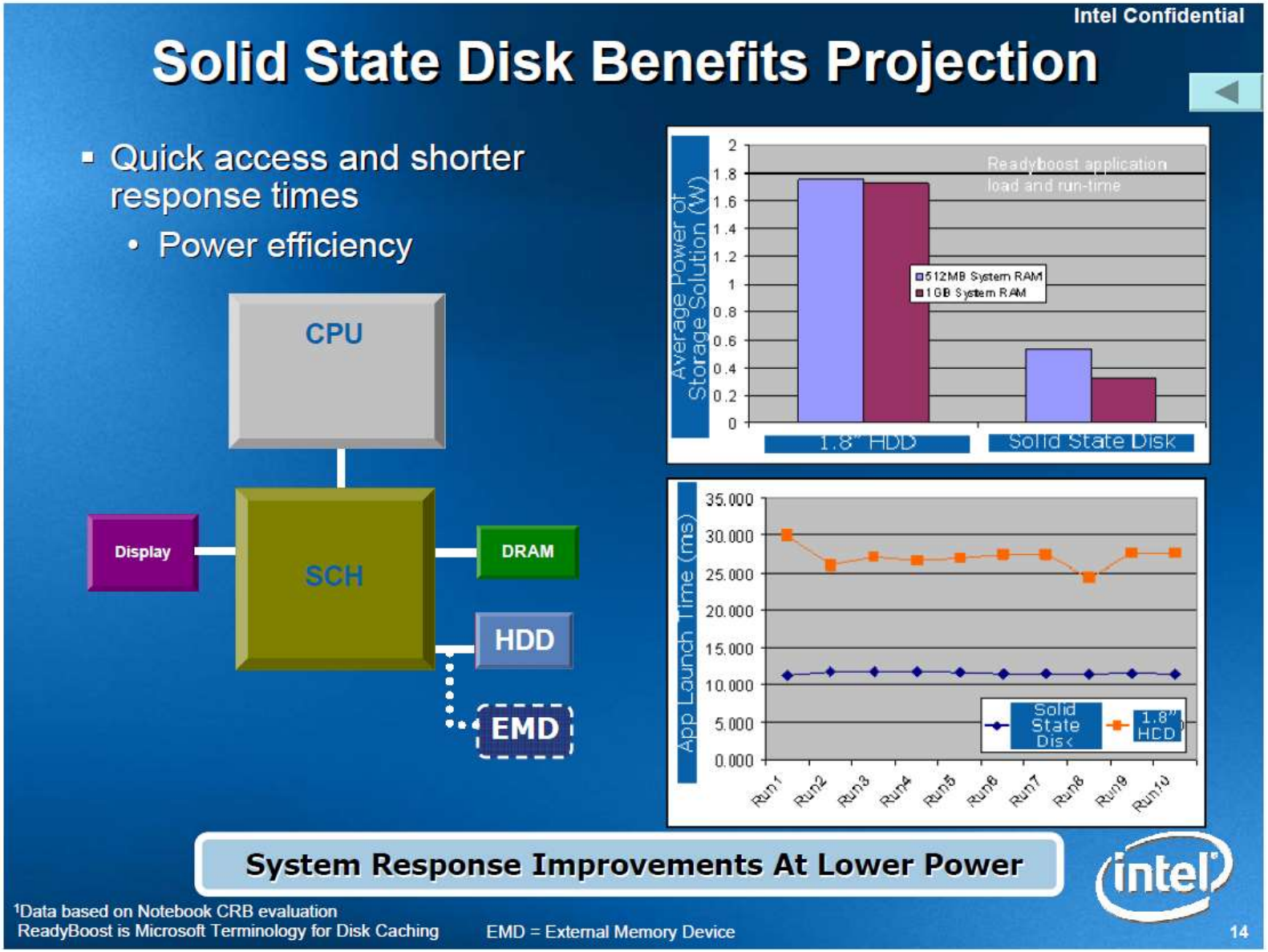
Bottom Package Envelope
12mmx12mm
~162 balls (for extra densities)

Preliminary Product Specs
-40 MB/s Read & 30 MB/s Write (SLC, sequential operations)
-Support for both SLC and MLC NAND

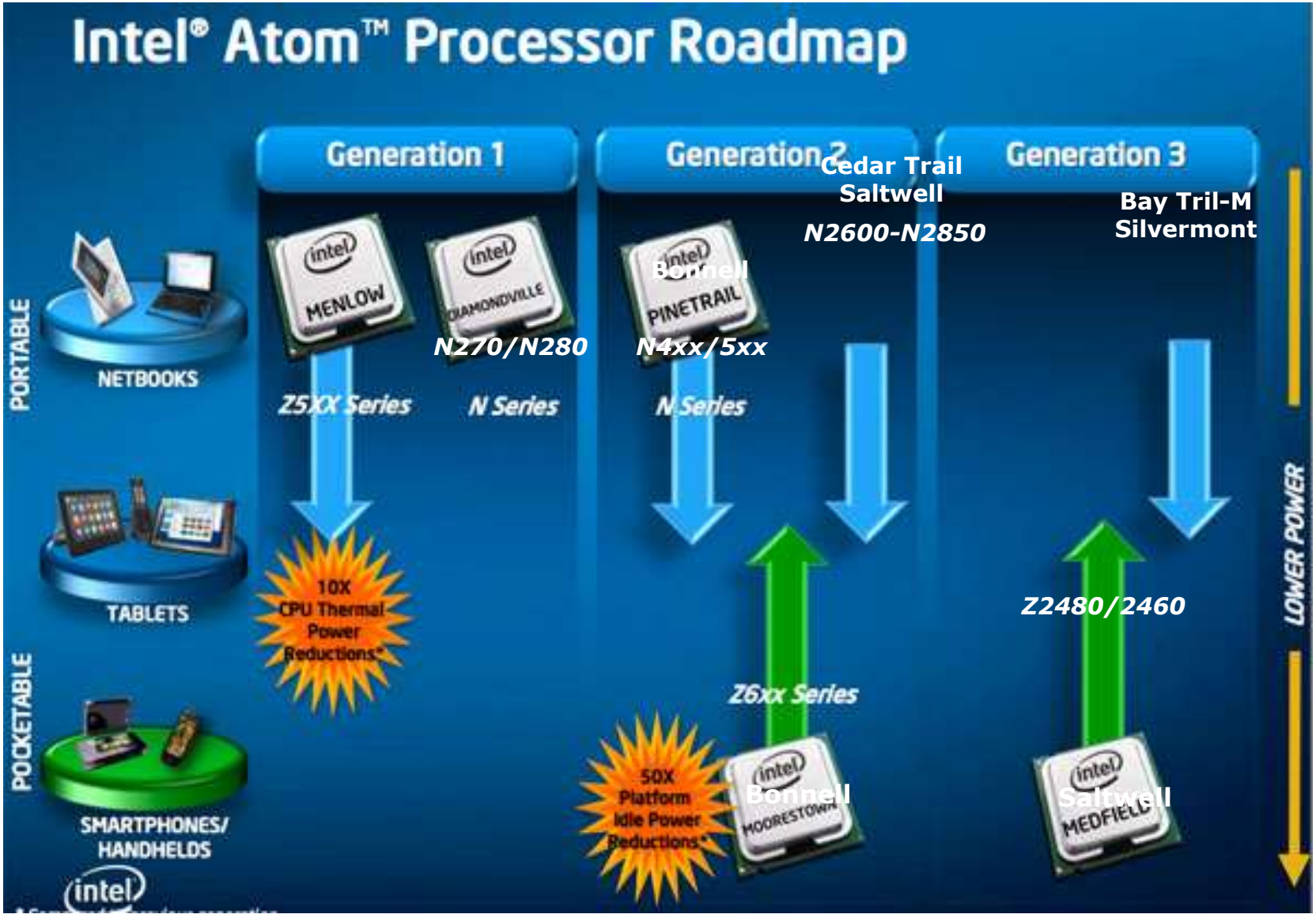
[1]Planning and Definition Phase POR expected in Q2'07
[2]Preliminary Data and Subject to Change

17

Intel Solid State Disk implementation as a PoP package-4 [99]



Intel Atom processor roadmap [89]



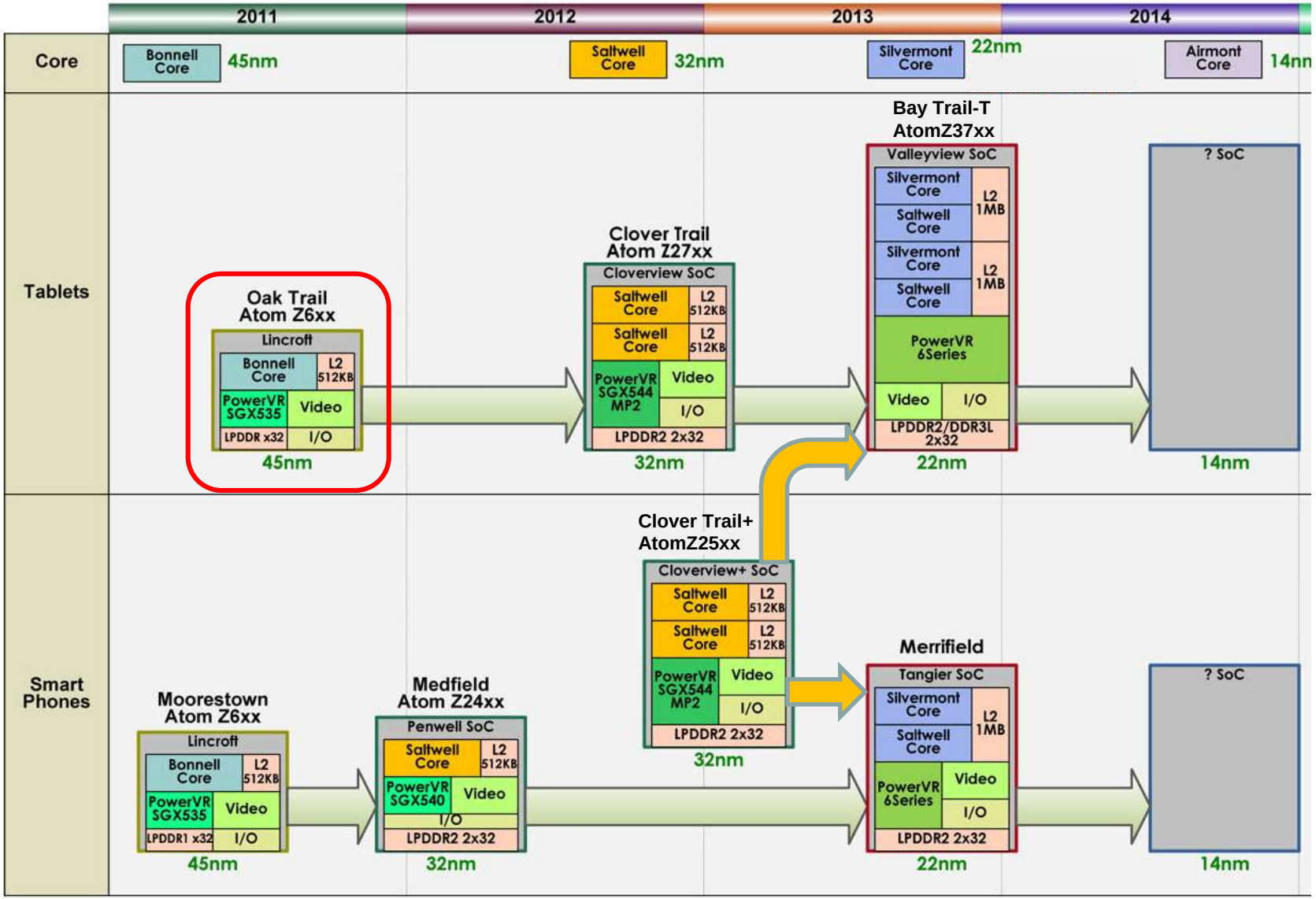
4.3 The Oak Trail platform

4.3 The Oak Trail platform

- Announced and available: 4/2011.
- It is a 2-chip platform consisting of
  - the Lincroft Z670/Z650 processor and
  - the SM35 (Whitney Point) PCH (Peripheral Control Hub), as the next Figure indicates.

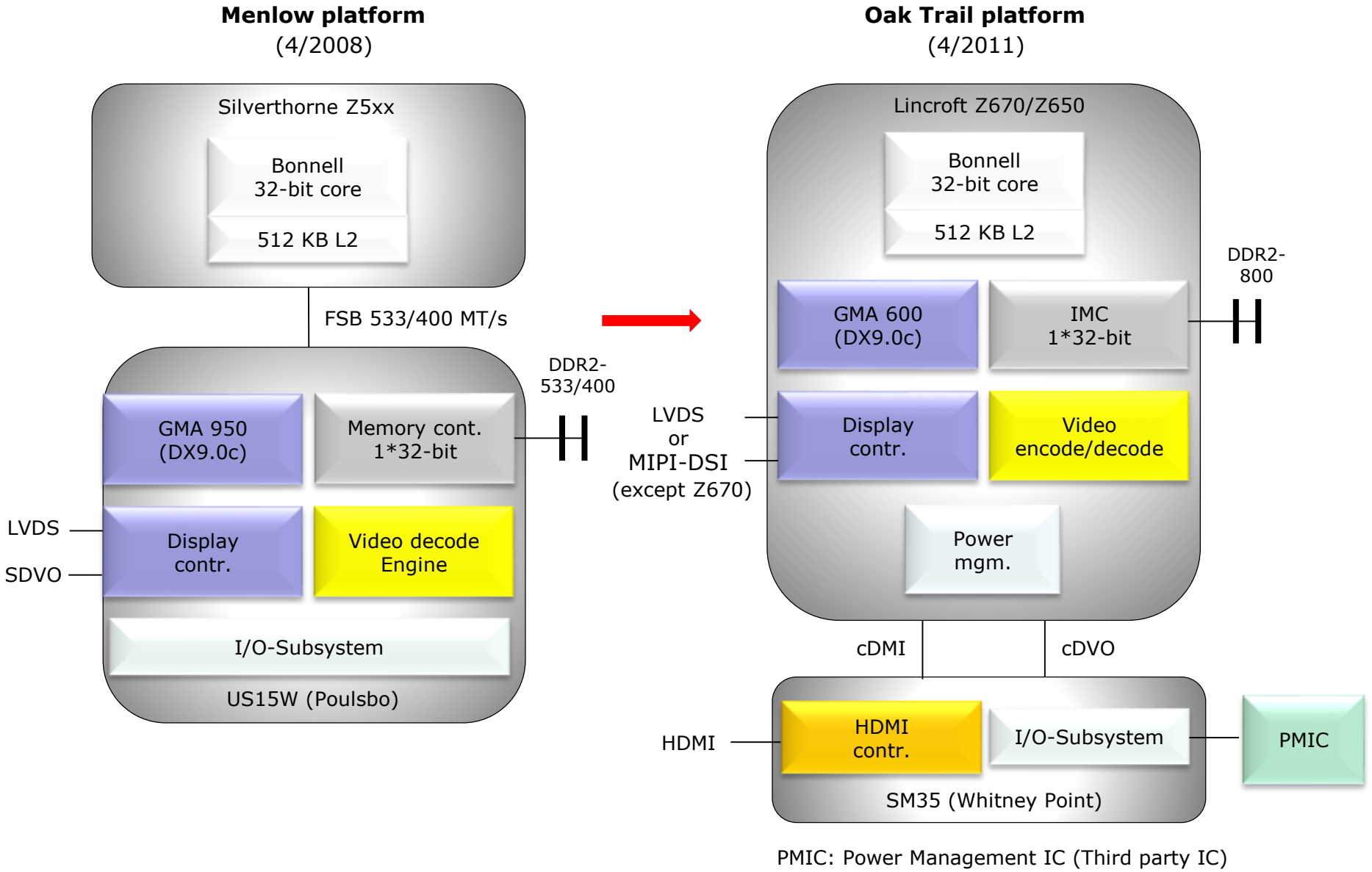
4.3 The Oak Trail platform (2)

Positioning the Oak Trail platform in Intel's tablet and smart phone platforms [110]



4.3 The Oak Trail platform (3)

Evolution of the Oak Trail platform



PMIC: Power Management IC (Third party IC)

4.3 The Oak Trail platform (4)

The Lincroft processor

- It is based on the 45 nm Bonnell CPU core executing the x86-32 ISA.
- It is a single core implementation, but integrates already the GPU, a single channel memory controller, the display control and video encode/decode, as shown below.

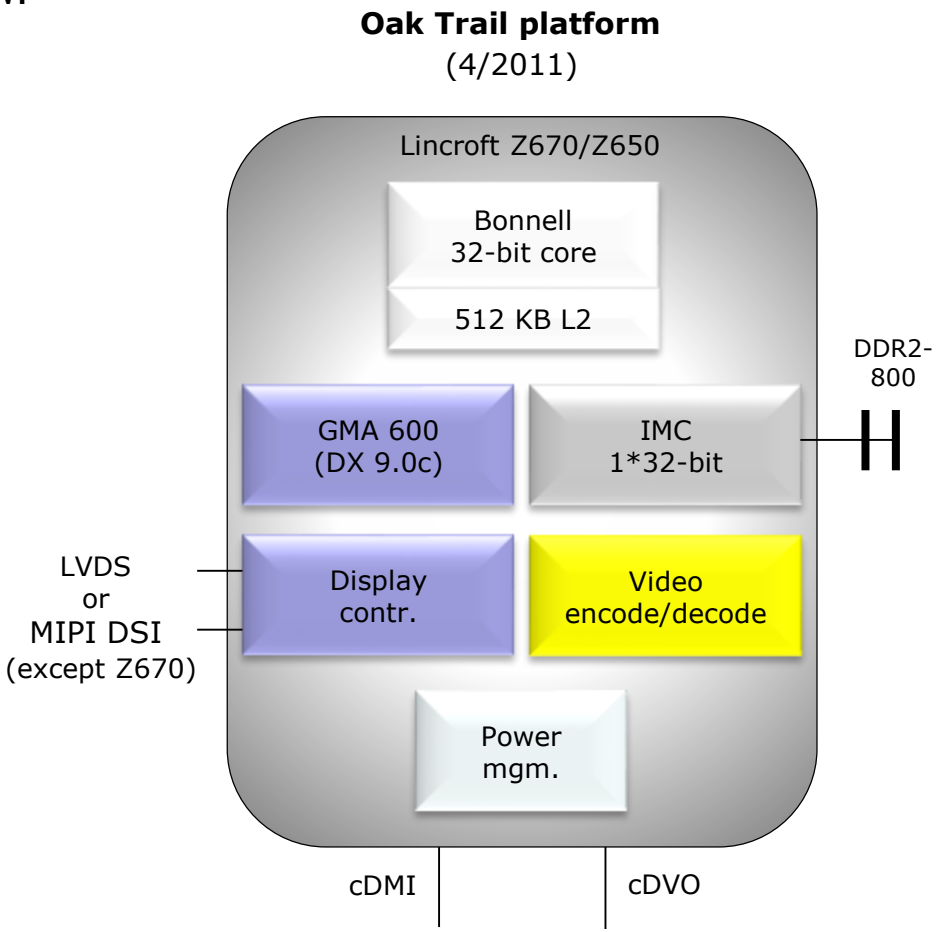


Figure: The Lincroft processor

4.3 The Oak Trail platform (5)

OS support

The Oak Trail platform may run under Windows 7, Android and MeeGo.

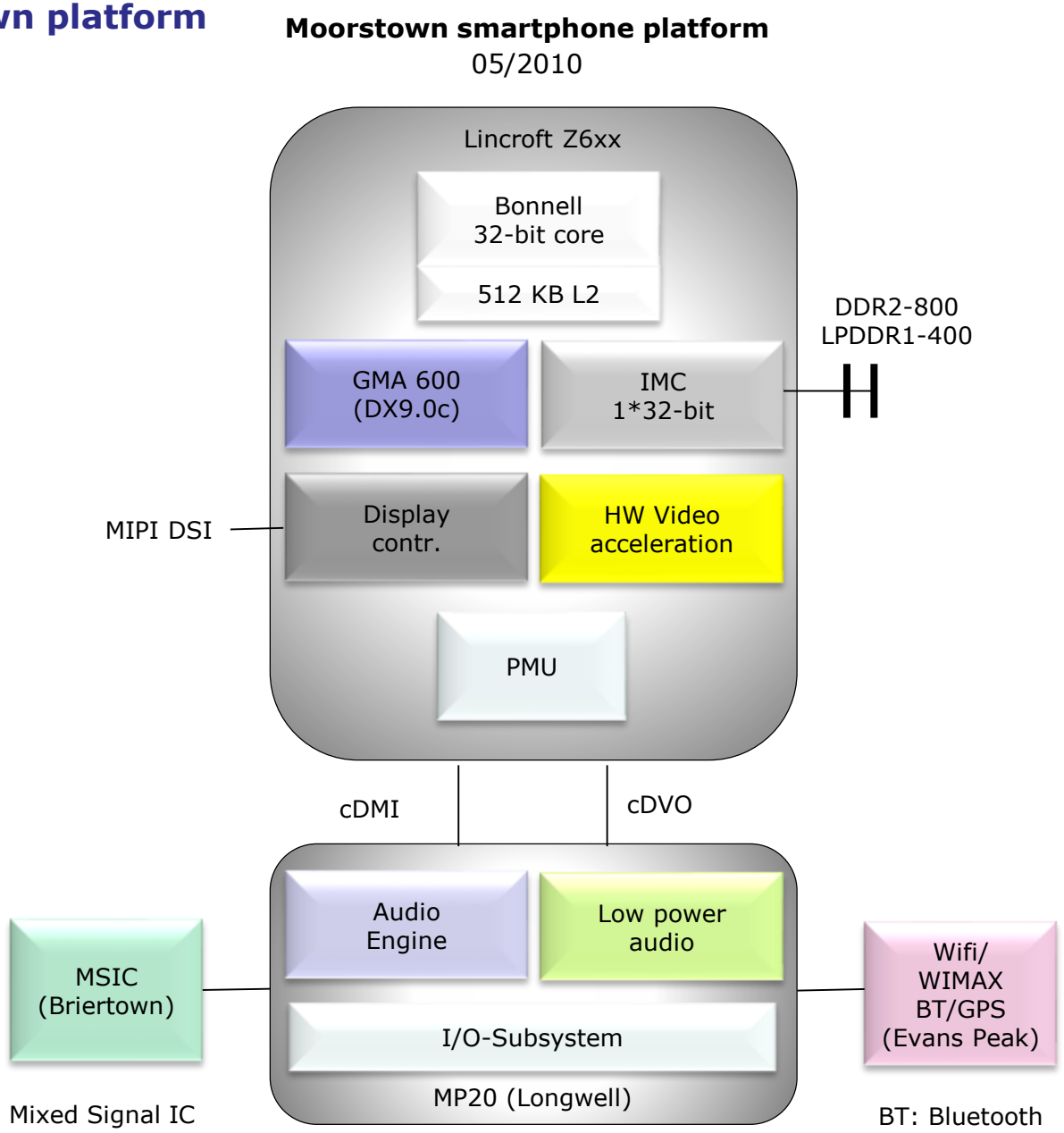
4.3 The Oak Trail platform (6)

Note

The Oak Trail tablet platform is based on the same Lincroft processor as the about one year earlier (5/2010) introduced Moorestown smartphone platform, as indicated next.

4.3 The Oak Trail platform (7)

The Moorestown platform



4.3 The Oak Trail platform (8)

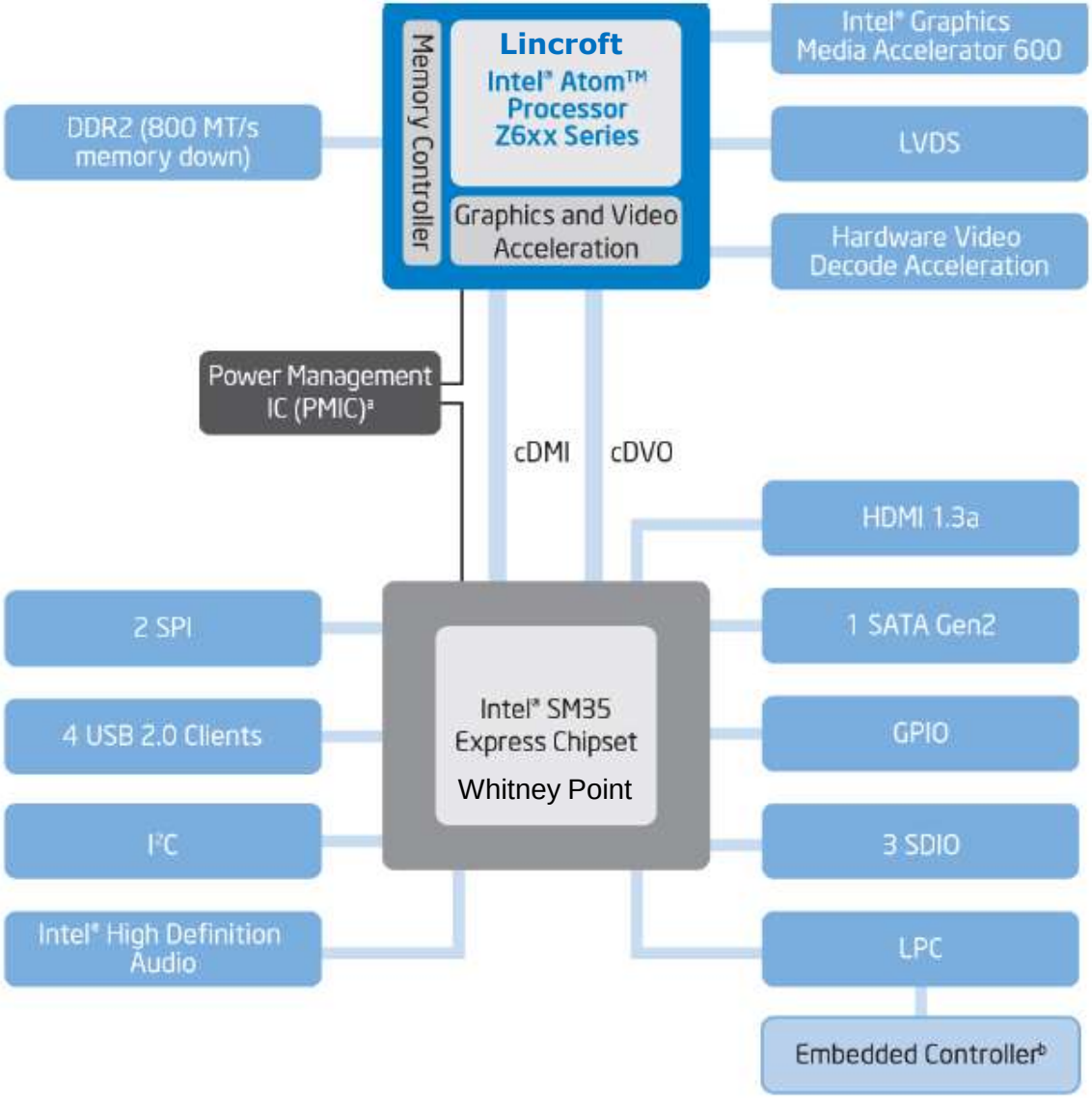
Key differences between the Moorestown smartphone and the Oak Trail tablet platform

Nevertheless, the Moorestown platform

- has a different companion chip (the MP20),
- has a number of additional performance and low power features, detailed in Section 5.2, and
- runs under the OSs Moblin, MeeGo and Android rather than Windos 7, Moblin and Android used for the Oak Trail platform.

4.3 The Oak Trail platform (9)

More detailed block diagram of the Oak Trail platform [90]



4.3 The Oak Trail platform (10)

The Power Management IC (PMIC)

It is a third party IC, like the one indicated below.

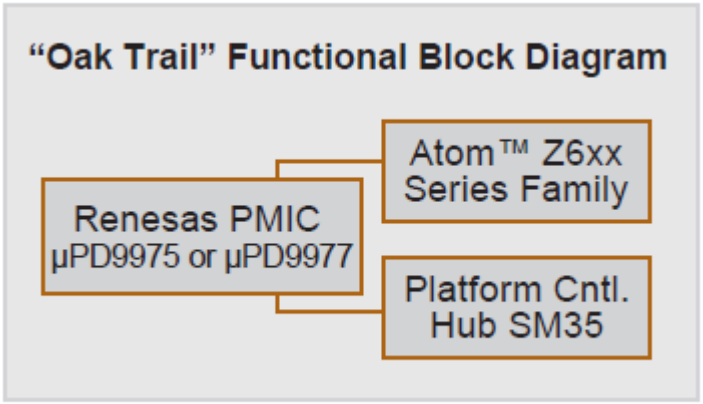


Figure: Example PMIC

The main task of the PMIC is to provide the requested regulated voltages for the power rails that supply the power gate domains and provide additional services, like multi-channel A/D-converters for temperature, power and voltage sensing and monitoring or real time clock.

4.3 The Oak Trail platform (11)

Main features of the Oak Trail tablet platform

	Menlow	Oak Trail	Clover Trail	Clover Trail+	Bay Trail -T
Available	04/2008	04/2011	12/2012	02/2013	Q9/2013
Focus	MIDs	Tablets	Tablets	Smartphones/tablets	Tablets
Processor	Silverthorne	Lincroft	Cloverview	Cloverview	Valleyview -T
Models	Z5xx	Z650/Z670	Z2760	Z2520-Z2580	Z36xx, Z37xx(D)
Technology	45nm	45nm	32nm	32nm	22nm
Die size	26 mm^2	65 mm2	64 mm2		
No. of trans.	47 mtrs	140 mtrs	432 mtrs		
Micro-arch.	Bonnell	Bonnell	Saltwell	Saltwell	Silvermont
32/64-bit	32-bit	32-bit	32-bit	32-bit	64-bit
1C/2C	1C	1C	2C	2C	2C/4C
HT	HT	HT	HT	HT	no HT
fc [GHz]	0.8-2.13	1.20/1.25	1.50 (1.80 Turbo)	Up to 1.2-2.0 (Turbo)	Up to 1.83-2.41 (Turbo)
L2	512 kB	512 kB	2x512 kB	2x512 kB	2x1 MB
No. of mem.ch.	Single channel MC on SCH	Single channel MC on proc. die (32-bit)	Dual channels MC on proc. die (32-bit)	Dual mem. ch. MC on proc. die (32-bit)	Single/dual mem. channels MC on proc. die (64-bit)
Memory	DDR2-533/400	DDR2-800	LPDDR2-800 (POP)	LPDDR2-1066 (POP)	LPDDR3-1066
GPU	GMA 500 (SGX 535) in PCH (US15W)	GMA 600 (SGX 535) on the proc.	Power VR SGX 545 on the proc	Power VR SGX 544 MP2 on the proc.	Gen 7 DX11 on the proc.
DX	DX 9.0c	DX 9.0c	DX 9.0c	DX 9.x	DX 11
Camera res.	—	—	8 Mpixel	16 Mpixel	
ISP	—	—	ISP 2300	ISP	ISP
Display output	LVDS, SDVO on U515W	LVDS or MIPI-DSI on proc. HDMI 1.3a on SM35	HDMI 1.3a, MIPI-CSI,-2 MIPI-DSI, MIPI-HSI	HDMI 1.3a, MIPI-CSI,-2 MIPI-DSI, MIPI.HSI	HDMI 1.4a, DP 1.2, eDP1.3, MIPI_CSI, MIPI-DSI
GPU clock	400/533 Mb/s	400 MHz	533 MHz	300-533 MHz	
Proc. TDP	0.65-2.5 W	3.0 W	1.7W	2.0-3.0 W	2.0-2.4 W (SDP)
FSB	400/533 MT/s	400 MT/s per dir. cDMI (8-bit)	—	—	—
Socket	PBGA441	BGA 518	FC-MB4760	BGA 760	UTFCBGA1380
Chipset	U515W (Poulsbo)	SM 35 (Whitney Point)	no, SOC	no, SOC	no, SOC
OS	Windows XP/Vista/7 Moblin 1	Windows 7 Home Premium MeeGo, Android	Windows 8 Pro Windows 8	Android 4.2	Windows 8.1 CS (32-bit) Android 4.2.2
Examples	Beng S6 Compal KAX15 Lenovo ideapad U8	Fujitsu Q550 Intel Studybook prototype Motion Computing's CL900 tablet	Acer Iconia W3/W510 Asus VivoTab Dell Latitude 10 HP Envy x2/ElitePad 900 Lenovo Thinkpad Tablet 2 Samsung Series 5 Slate	Asus MeMO Pad FHD 10 / Fonepad Note / Transformer Book Trio Samsung Galaxy Tab3	Acer W3-810 Asus Transformer Book Trio T100 Dell Venue/ Midland Lenovo Miix 8/ Miix 2 Toshiba Encore

Key features of the introduced Lincroft Z670/Z650 processors and the SM35 PCH [91]

Intel® Atom™ Processor Z6xx Series Available in 30 Days

	Core Freq	Graphics Speed	TDP	Temperature Range	Package
Intel® Atom™ processor Z670	1.5GHz	400MHz	3.0W	Commercial; 0° to 70° C	518-ball PCMB3 13.8x13.8mm
Intel® Atom™ processor Z650	1.2GHz	400MHz	3.0W	Commercial; 0° to 70° C	518-ball PCMB3 13.8x13.8mm

Intel® SM35 Express Chipset Available in 30 Days

	TDP	Temperature Range	Package
Intel® SM35 Express Chipset	0.75W	Commercial; 0° to 70° C	493-ball FCPGA 14x14mm

4.3 The Oak Trail platform (13)

Key innovations of the Oak Trail platform

There are only two key innovations to be mentioned over the previous Menlow platform, that are

- integration of key functional units onto the processor die, such as the GPU, a single channel memory controller, the display control and video encode/decode, and
- aggressive power gating of the processor chip.

This is somehow surprising since the Lincroft processor of the Moorestown smartphone platform provides for numerous innovations targeting performance increase and low power operation (discussed in Section 5.2) and these innovations did not appear in the Lincroft processor used in the Oak Trail platform.

4.3 The Oak Trail platform (14)

Power gating-1 [92]

- To reduce idle power the Lincroft chip is divided into nineteen power domains such that each functional unit acts as a power domain, except of the Atom core, as shown in the Figure below.
- If a functional unit is not in use the related power domain can be turned off by on-die power gates (power transistors).

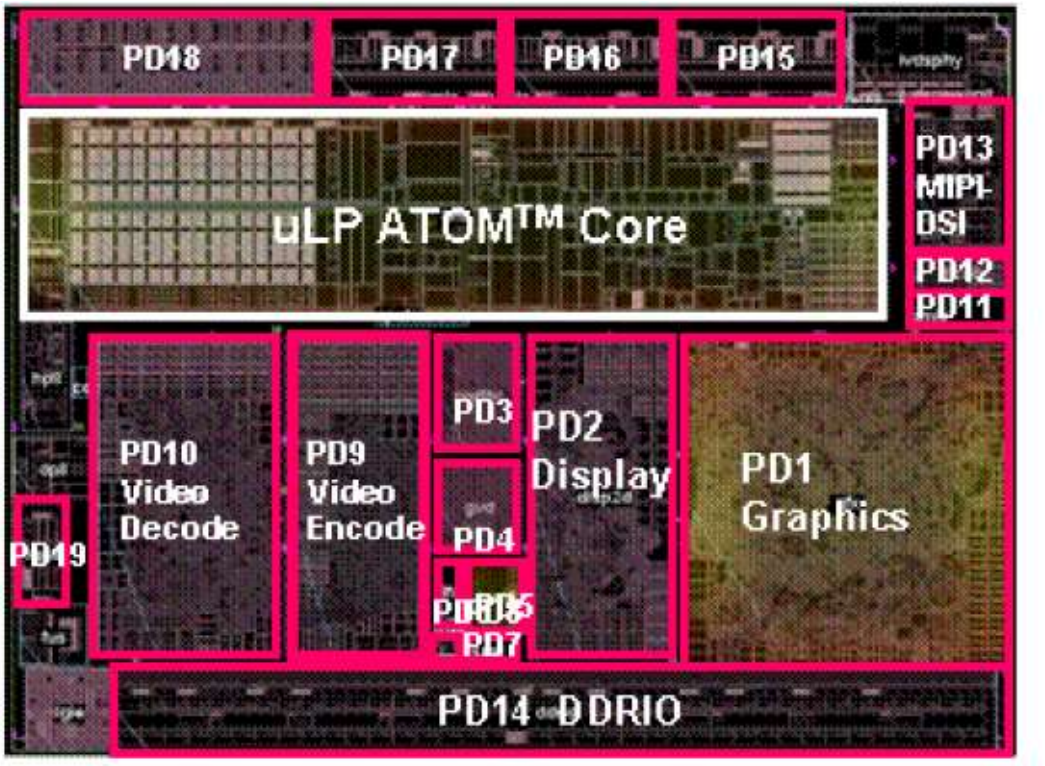


Figure: Powergated domains of the Lincoroft chip [92]

Power gating-2 [92]

- The embedded powergate cells are switched on or off by powergate control signals that are daisy chained, as indicated below.

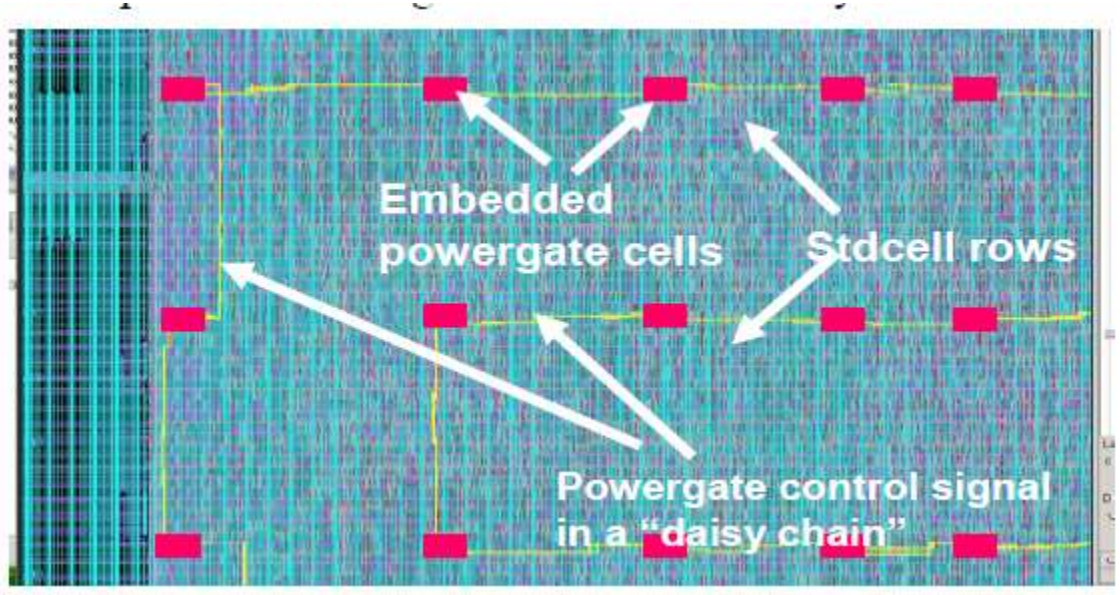


Figure: Distributed powergate cells in a powergated domain [92]

- Thus idle power is significantly reduced by shutting down unused portions of the chip.
- By contrast, the Atom core is power managed by C-states.

All-in-all, power gates cover about 70 % of the chip area.

Power gating-3 [93]

- There is a SW interface for power management of the powergated islands.
- HW manages the sequencing of the powergate control signals.

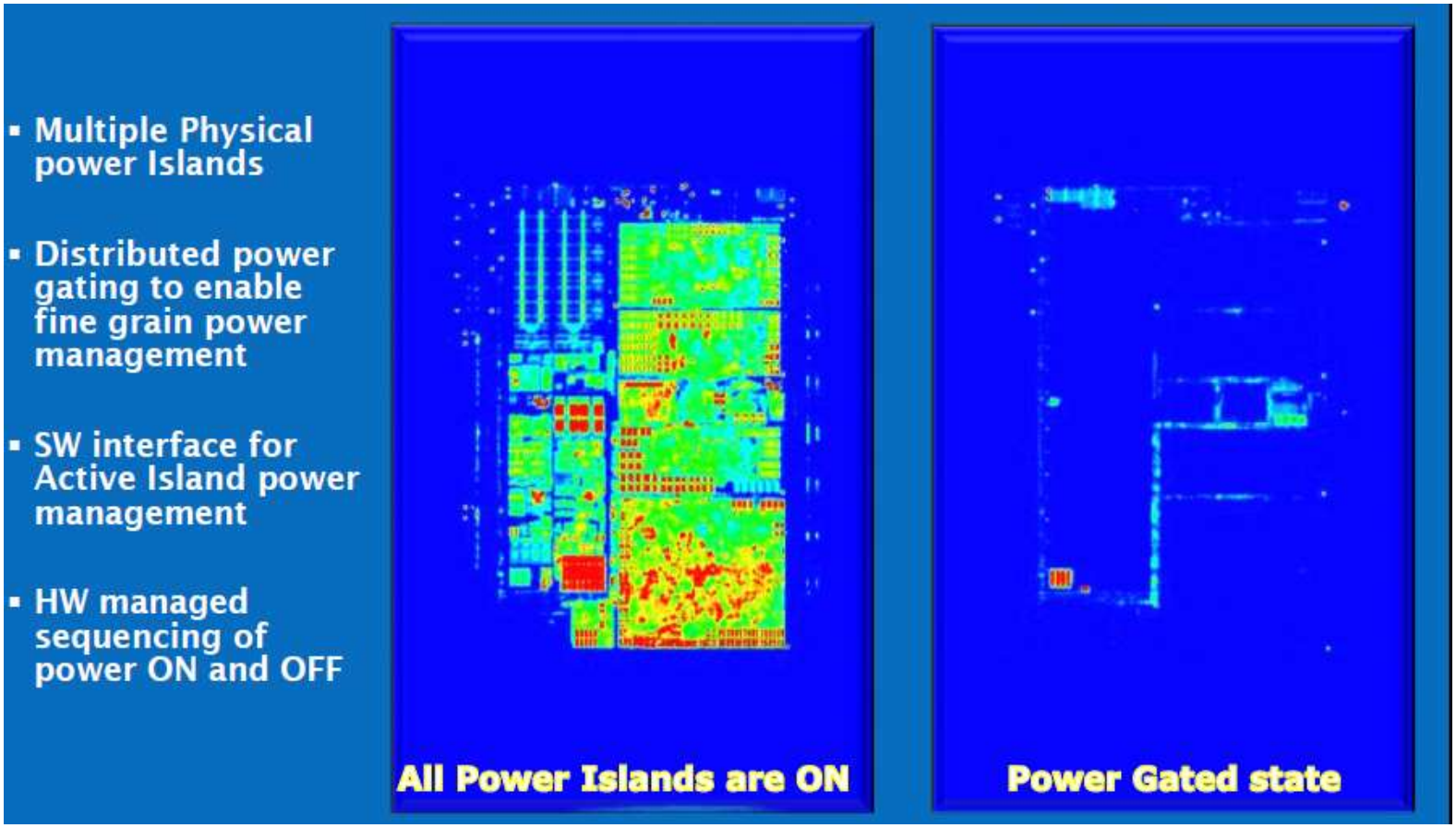


Figure: Infrared emission (IREM) image of a full on vs. powergated Licoln chip [93]

4.3 The Oak Trail platform (17)

Power gating-4 [93]

- Aggressive power gating enables up-to 50x reduction in idle power.

4.3 The Oak Trail platform (18)

Market reception of the Oak Trail platform

There are only a few tablet designs based on Intel's Oak Trail platform.

The vast majority of the tablets were designed further on with ARM-based processors and in a few cases based on AMD-s Brazos platform.

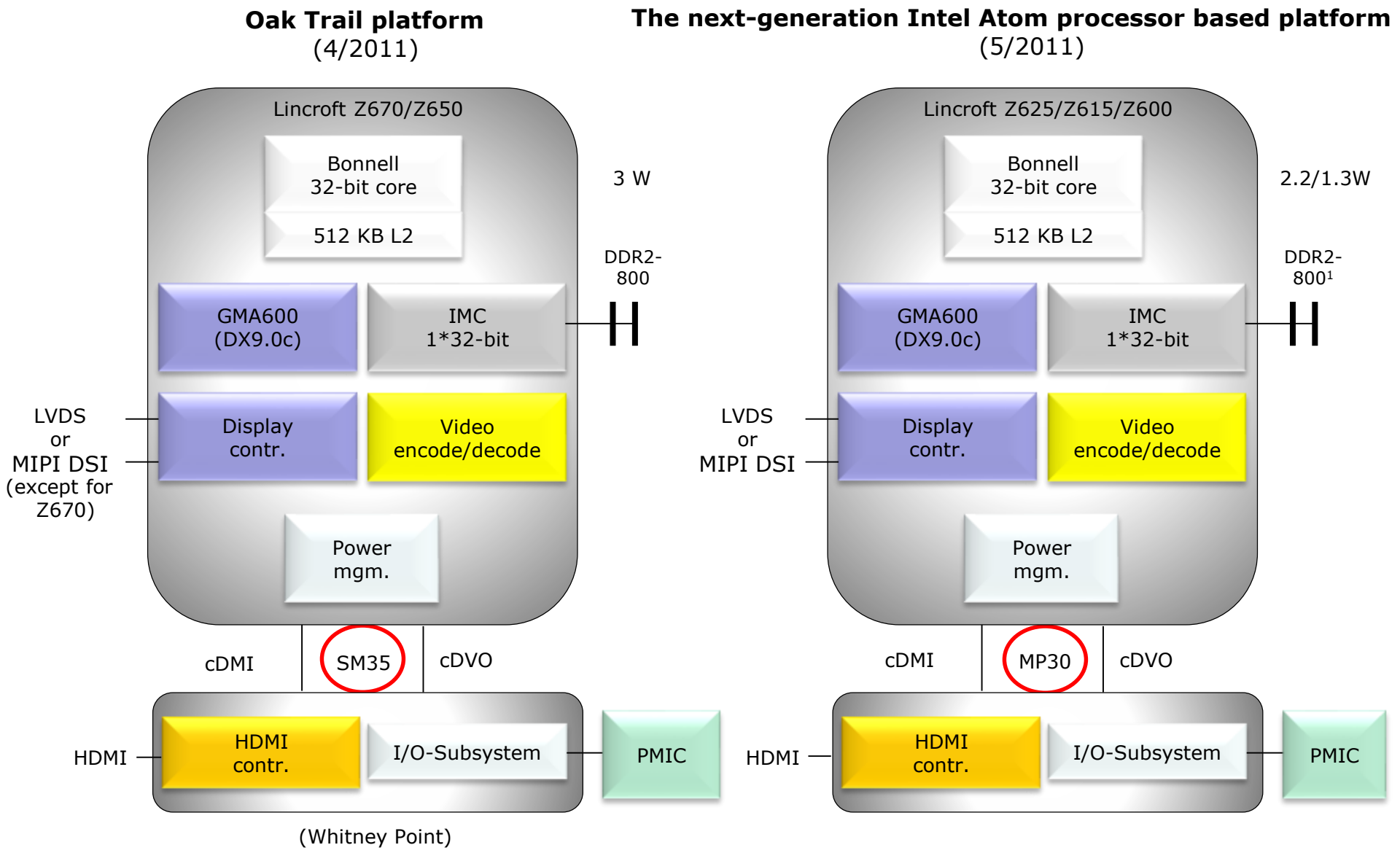
4.3 The Oak Trail platform (19)

Remark

We note that one month after the introduction of the Oak Trail platform Intel introduced another platform based on the Lincroft processor with a new companion PCH, designated as "The next-generation Intel Atom processor based platform", as shown below.

4.3 The Oak Trail platform (20)

Simplified block diagrams of the Oak Trail and the subsequently introduced platform



[1] LPDDR1-400 for Z600

4.3 The Oak Trail platform (21)

Features of "The next-generation Intel Atom processor based platform"

The new platform incorporates the Lincroft processor models Z600-Z625 and the MP30 PCH.

The Z600-Z625 models

- have less power consumption than the Z650/Z670 models of the Oak Trail platform,
- support MMX and SSSE3 in addition to the ISA extensions provided by the Z650/Z670 models,
- support the performance increasing and low power technologies of the Lincroft processor introduced along with the Moorstown smartphone platform, such as the Burst mode and the Smart Idle Technology, (see Section 5.2).

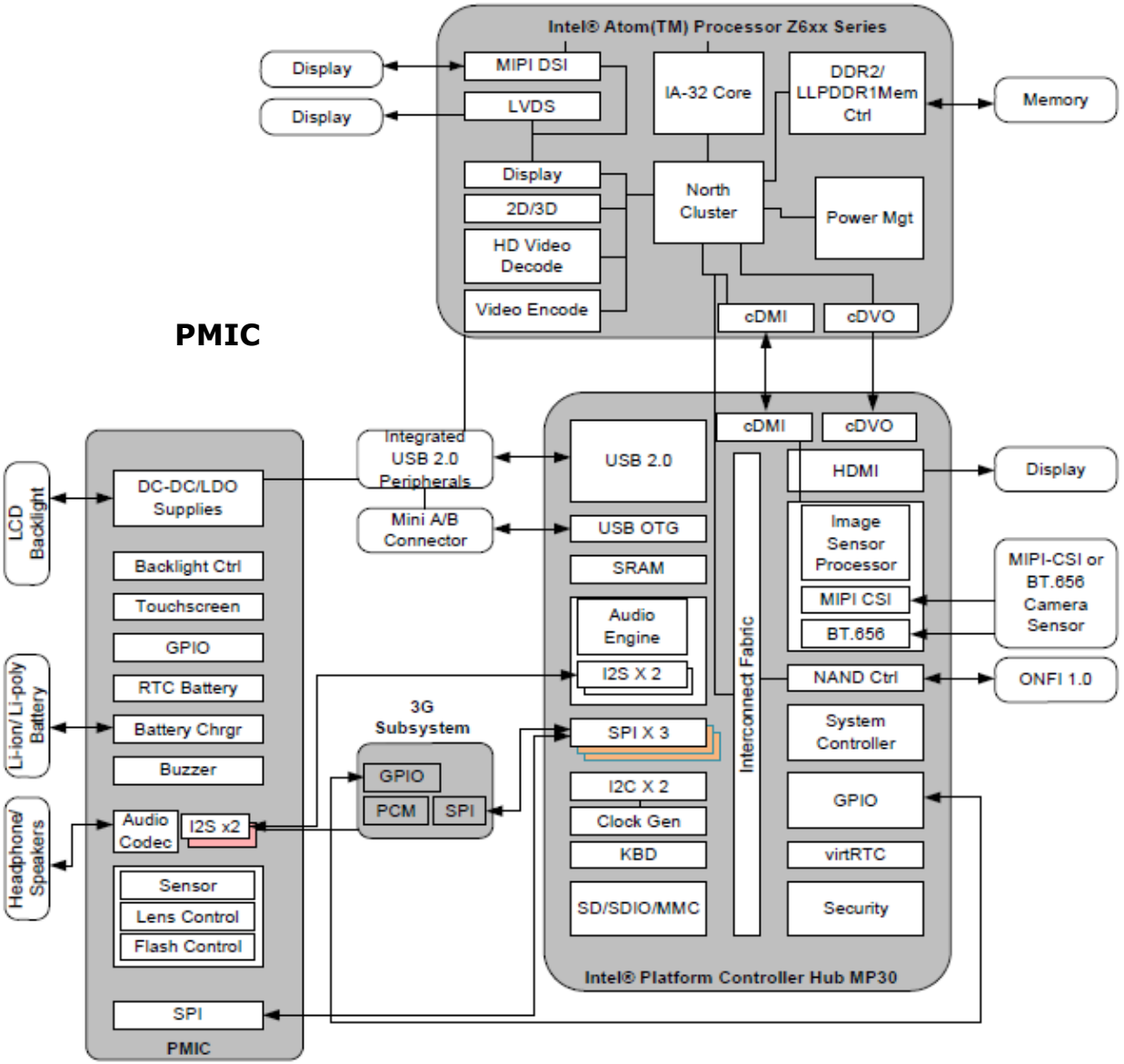
4.3 The Oak Trail platform (22)

The status of "The next-generation Intel Atom processor based platform"-2

- In public available documents Intel did not become specific neither about the brand name of the new platform nor its target application area.
- Nevertheless, considering the fact that Intel announced the Moorestown platform already in 5/2010 but did not ever specify the model numbers of the associated Lincroft processor, further on the fact that the Moorstown platform made use of the MP20 PCH and the new platform of the MP30 PCH, it can be concluded that the new platform was intended to become the real implementation of the Moorestown platform.
- On the other hand, due to the long delay of the Moorestown smartphone platform the nearing introduction of the next smartphone platform (the Medfield platform) with its improved features (32 nm technology, Saltwell CPU, SOC design) made superfluous the delayed real Moorestown platform.

4.3 The Oak Trail platform (23)

Block diagram of "the next-generation Intel Atom processor-based platform" [94] (5/2011)



Z625-Z600)
(Lincroft)

4.3 The Oak Trail platform (24)

Remark 2 [95]

In 3/2011 Intel's Senior Vice President and Leader of the Ultra Mobility Group, who was in charge of the tablet and smartphone development, Anand Chandrasekher resigned, by stating in a brief email "I have done what I wanted at Intel and I felt it was time to explore other opportunities."

In fact the real reason for Chandrasekher's leaving its position was that despite immense investments Intel could not achieve their goals in catching up with ARM-based devices in the tablet and especially smartphone space.

Moorestown was assessed by many industry observers as a complete flop and in the tablet sector could Intel achieve only a marginal market position with their Windows tablets.

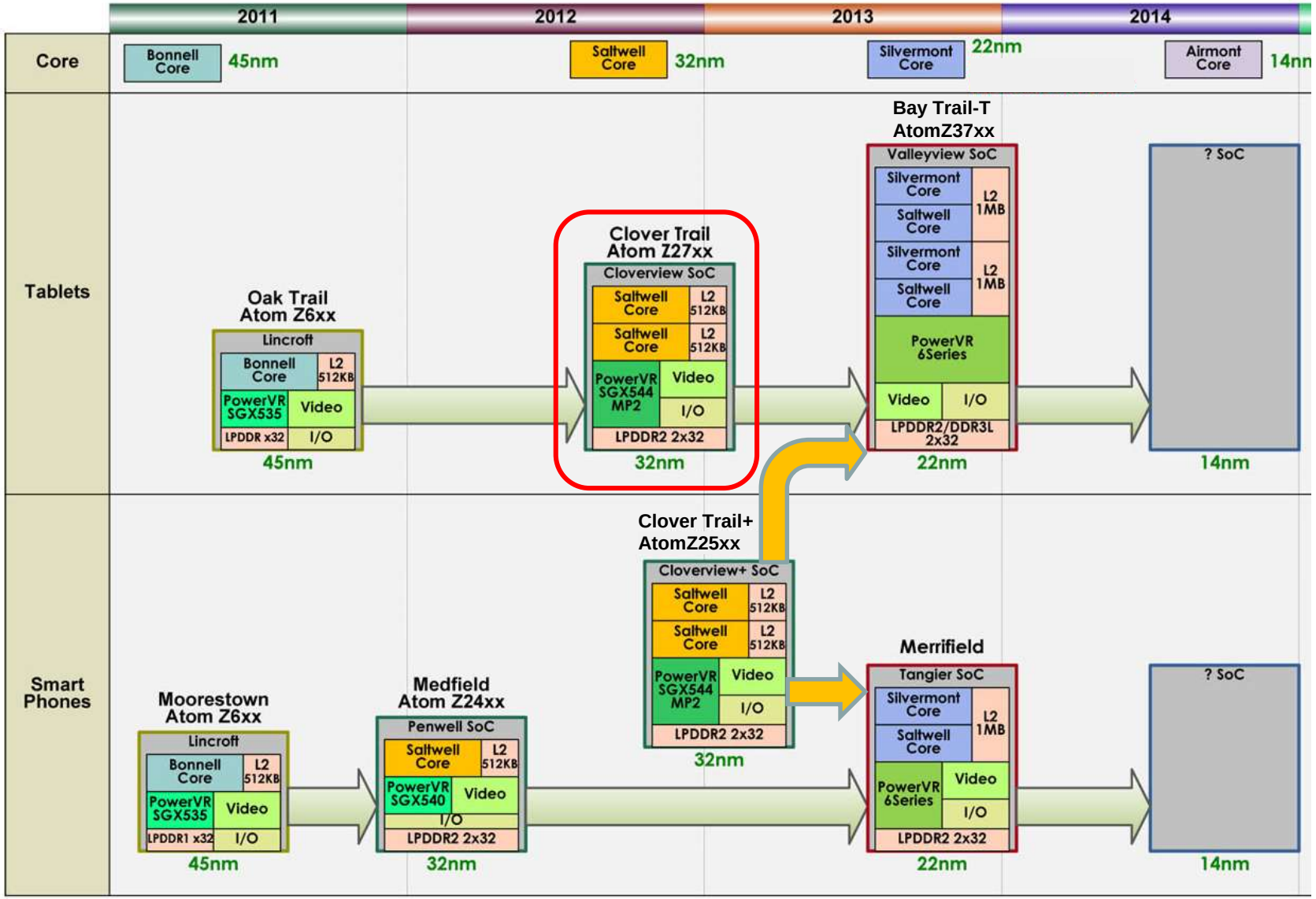
4.4 The Clover Trail platform

4.4 The Clover Trail platform

- Announced: 9/2012
- Available: ≈ 12/2012
- Based on the 32 nm Saltwell CPU, it is Intel's first SOC platform for tablets and convertibles, as indicated in the Figure.
- It is a platform for Windows tablets and convertibles.

4.4 The Clover Trail platform (2)

Positioning the Clover Trail platform in Intel's tablet and smart phone platforms [110]

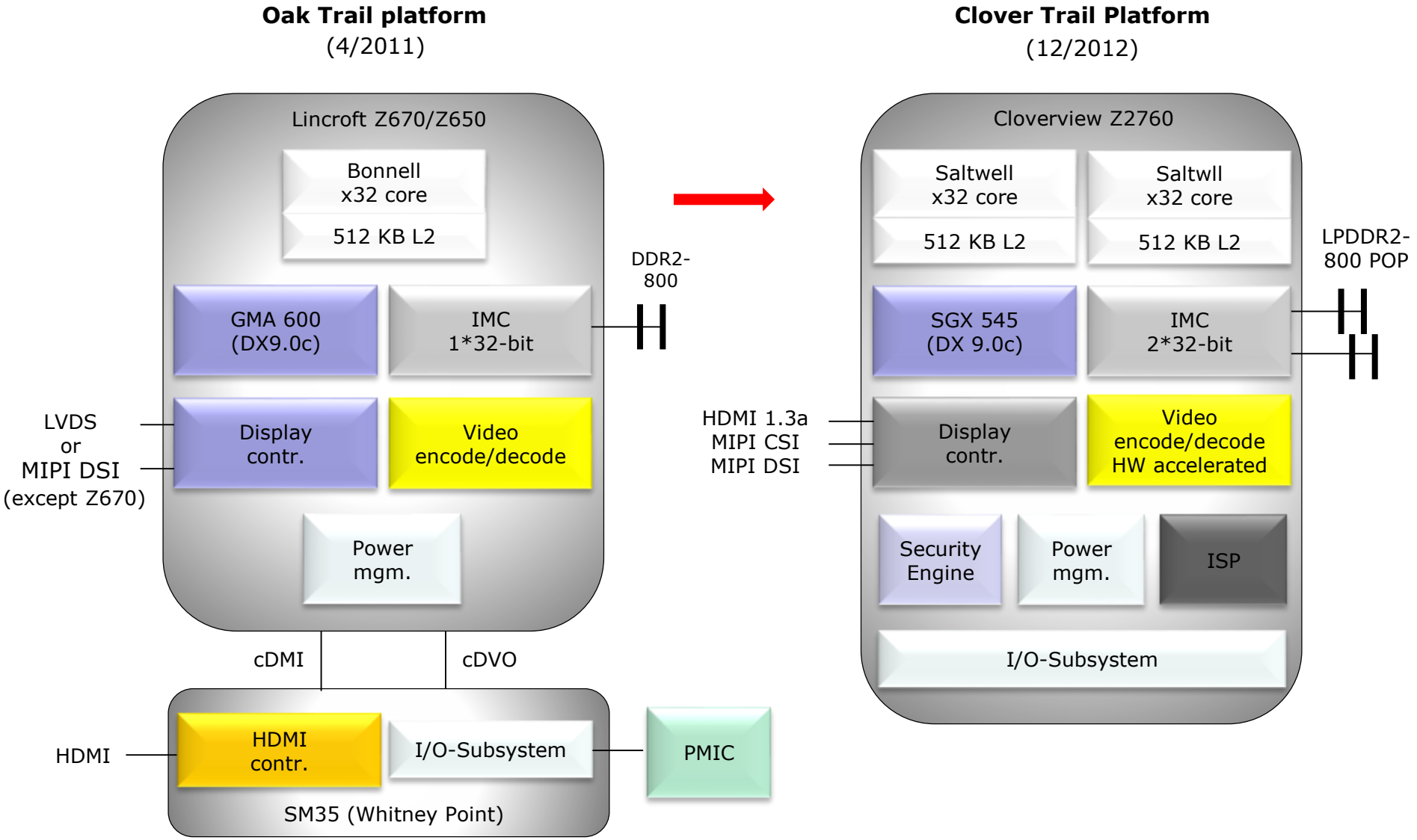


4.4 The Clover Trail platform (3)

Target market segments of Clover Trail: Windows 8-based tablets and convertibles [96]

4.4 The Clover Trail platform (4)

Evolution of the Clover Trail platform



PMIC: Power Management IC (Third party IC)

4.4 The Clover Trail platform (5)

The Cloverview processor

- It is based on the 32 nm Saltwell CPU core with the x86-32 ISA.
- It is a SOC implementation with integrating also the I/O functions of the SM35 PCH of the previous Oak Trail platform, as shown below.

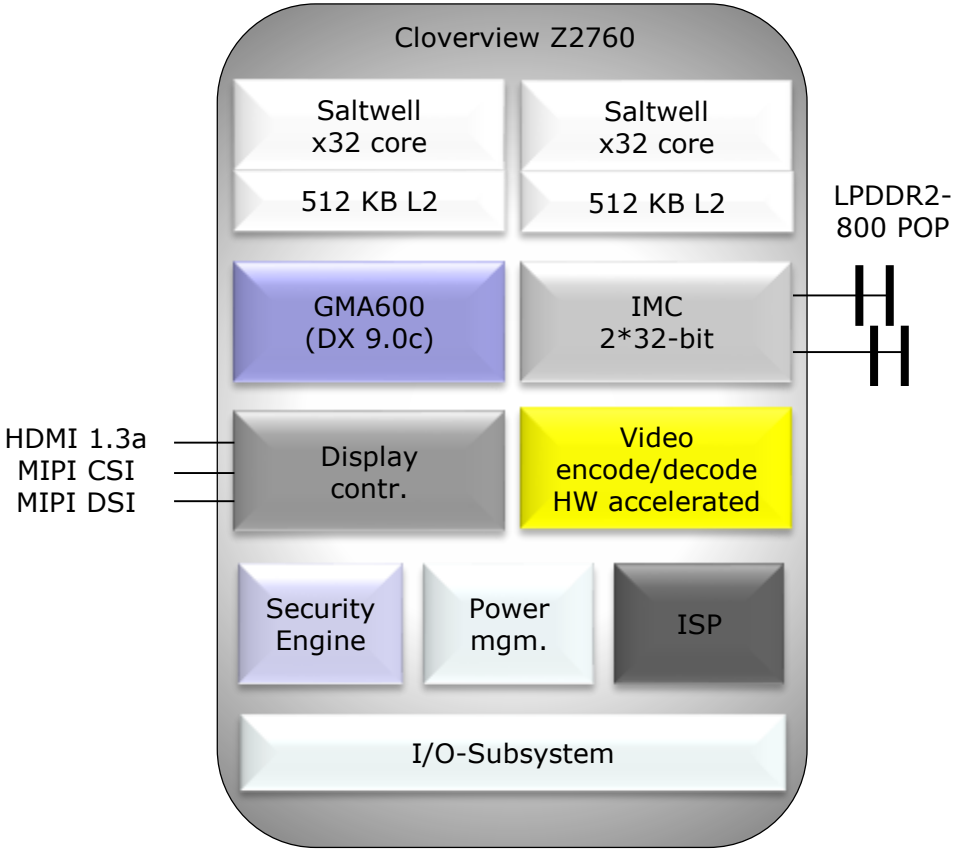
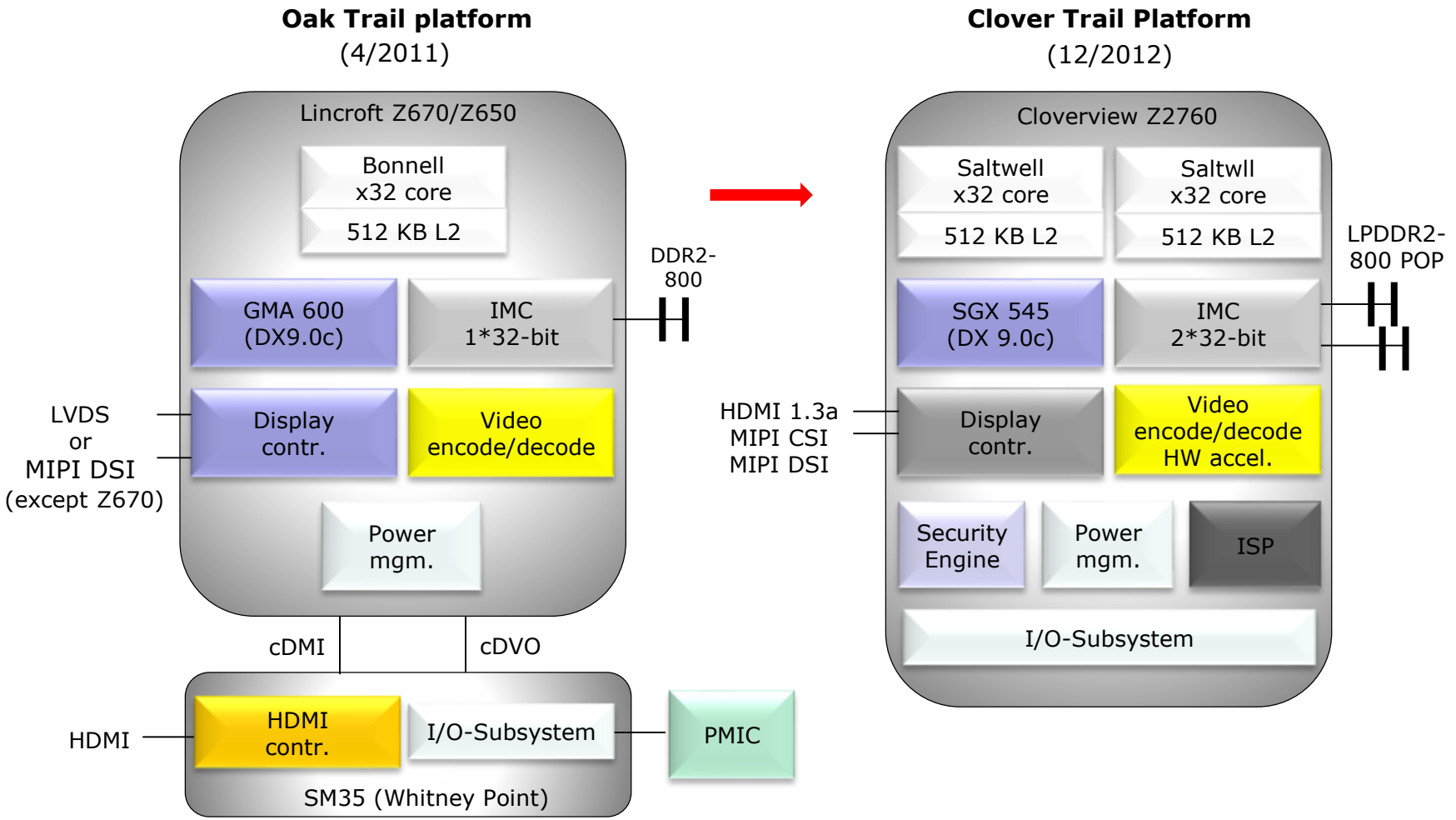


Figure: The Cloverview processor

4.4 The Clover Trail platform (6)

Main improvements of the Cloverview processor vs. the previous Lincroft processors-2

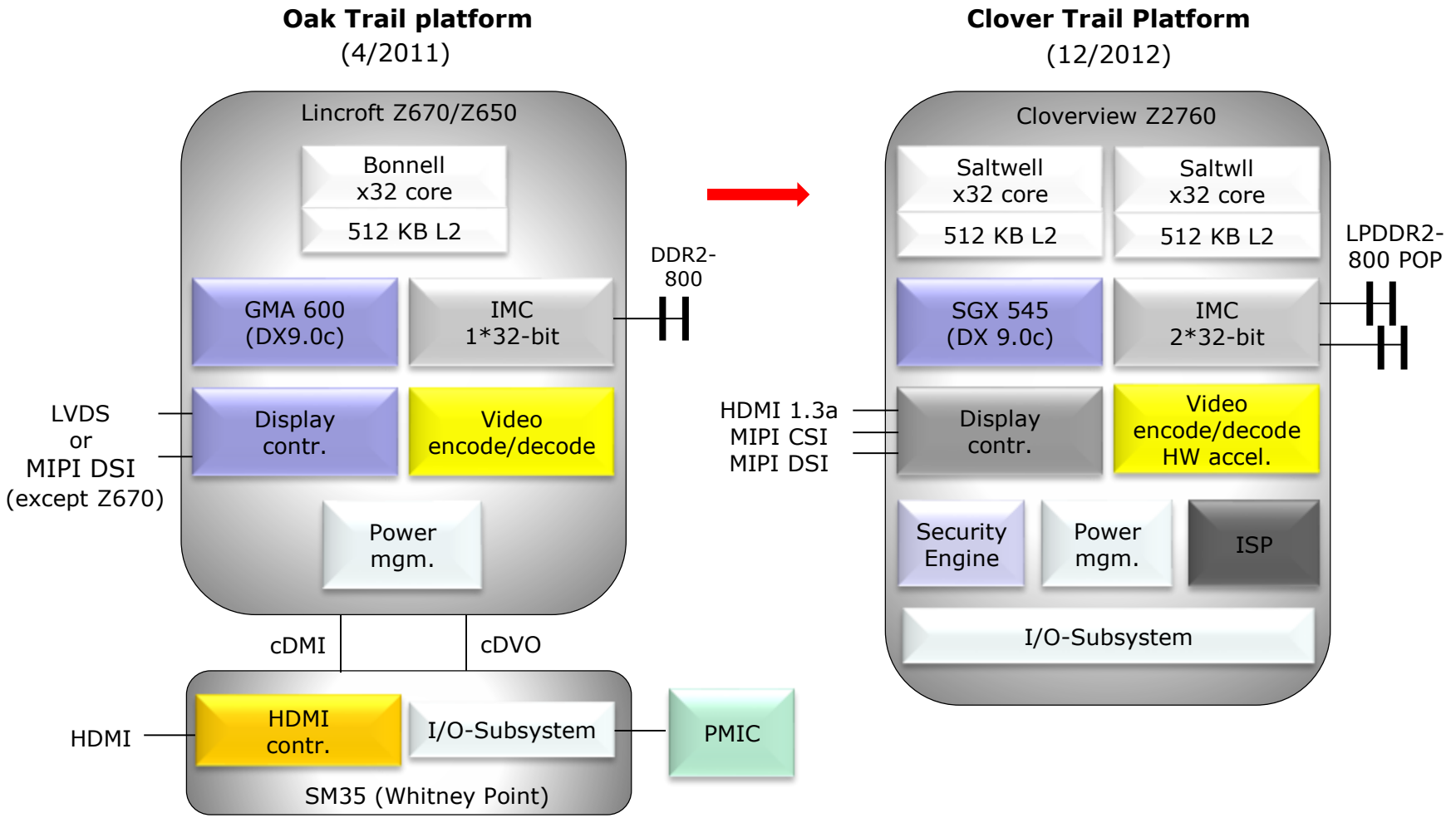
- There is a Security Engine,
- an Integrated Signal Processor (ISP), and
- an integrated I/O subsystem (implemented previously in the SM35 PCH).



4.4 The Clover Trail platform (7)

Main improvements of the Cloverview processor vs. the previous Lincroft processors-1

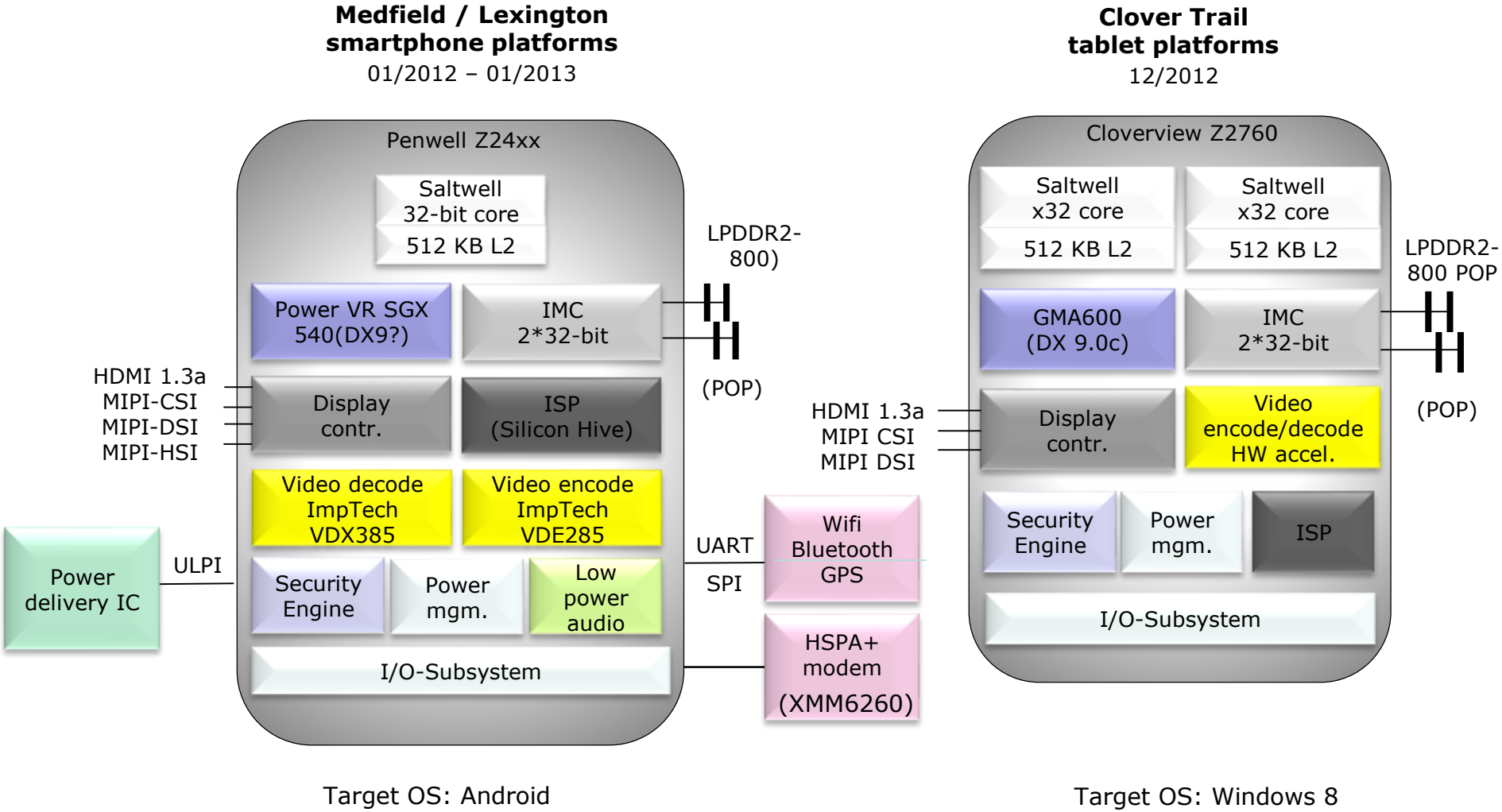
- It is based on the 32-nm Saltwell CPU rather than the 45 nm Bonnell CPU
- There is an integrated dual channel 32-bit memory controller for LPDDR2-800 memories,
- Video encoding/decoding is hardware accelerated



4.4 The Clover Trail platform (8)

Remark

Features and architecture of the Clover View processor targeting Windows 8 tablets is very similar to the Penwell processor targeting Android smartphones.



4.4 The Clover Trail platform (9)

OS support

The Clover Trail platform runs under Windows 8 and Windows 8 Pro.

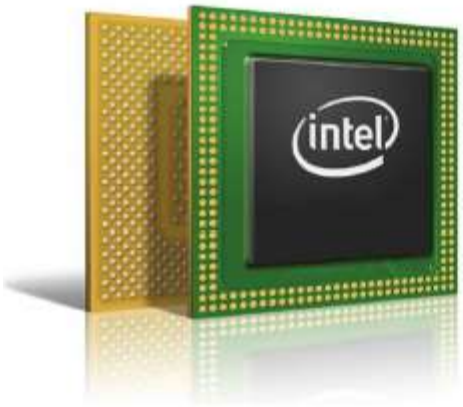
Remarks

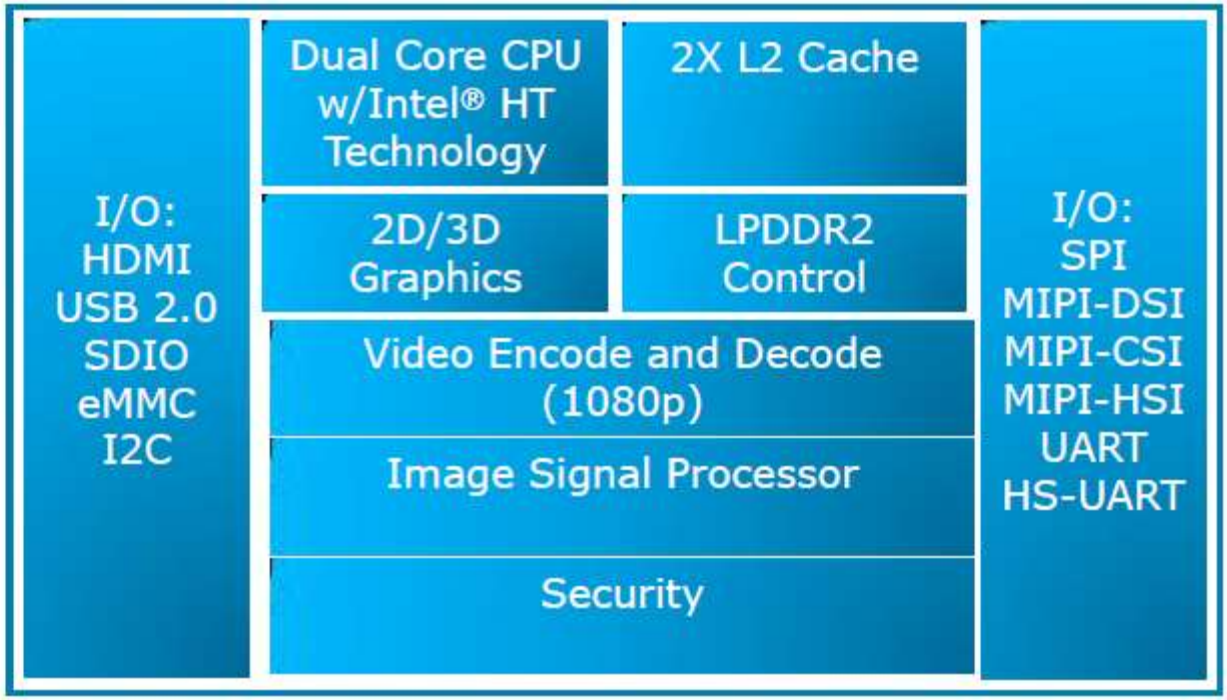
The Windows 8 OS was announced at CES 2011 (1/2011), whereas the stable release was made available for manufacturers in 8/2012 and for the general public in 10/2012.

The Windows 8.1 is expected to be available in 10/2013.

4.4 The Clover Trail platform (10)

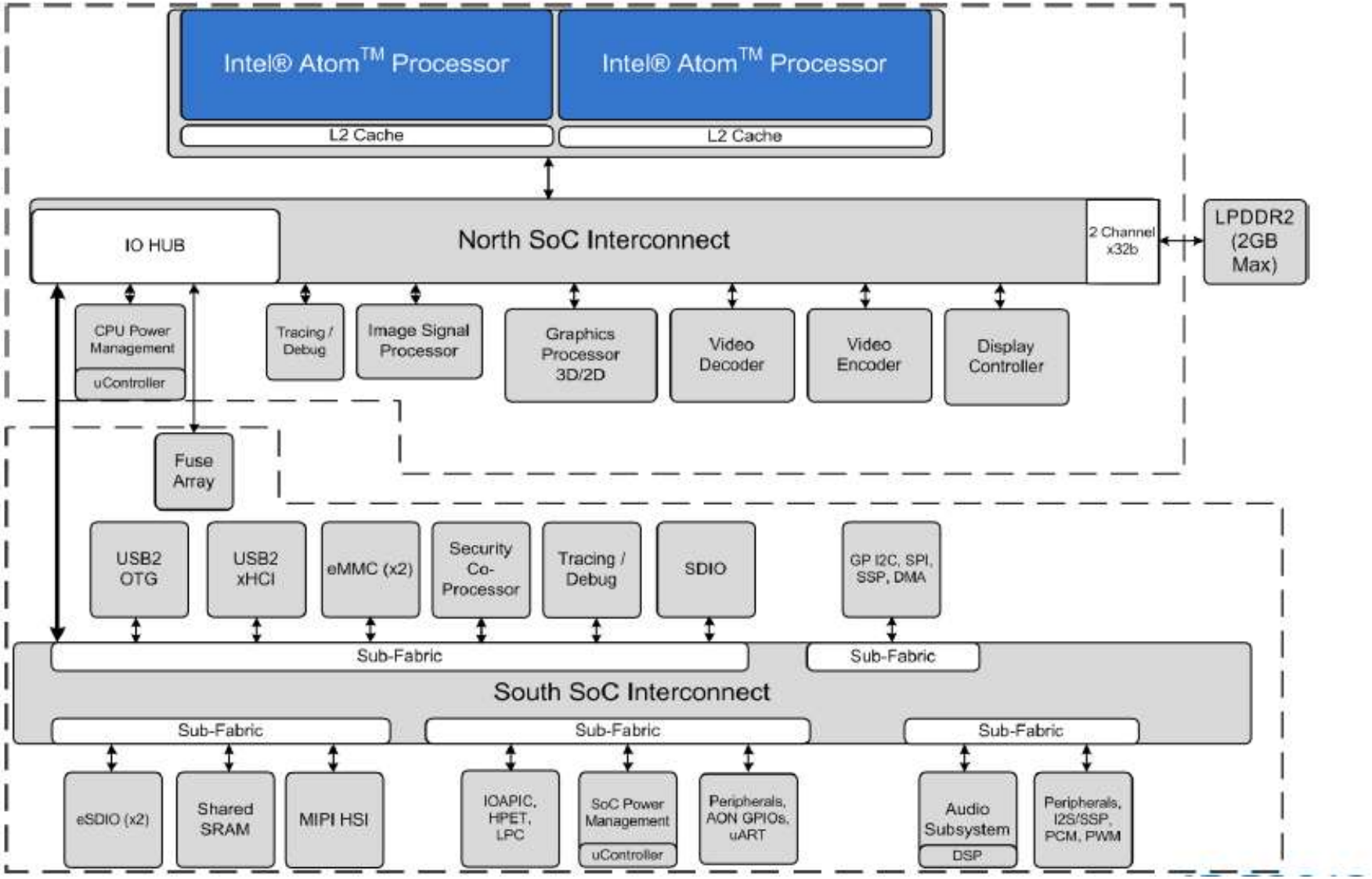
Block diagram of the Cloverview processor, as revealed by Intel at their IDF 2012 [96]





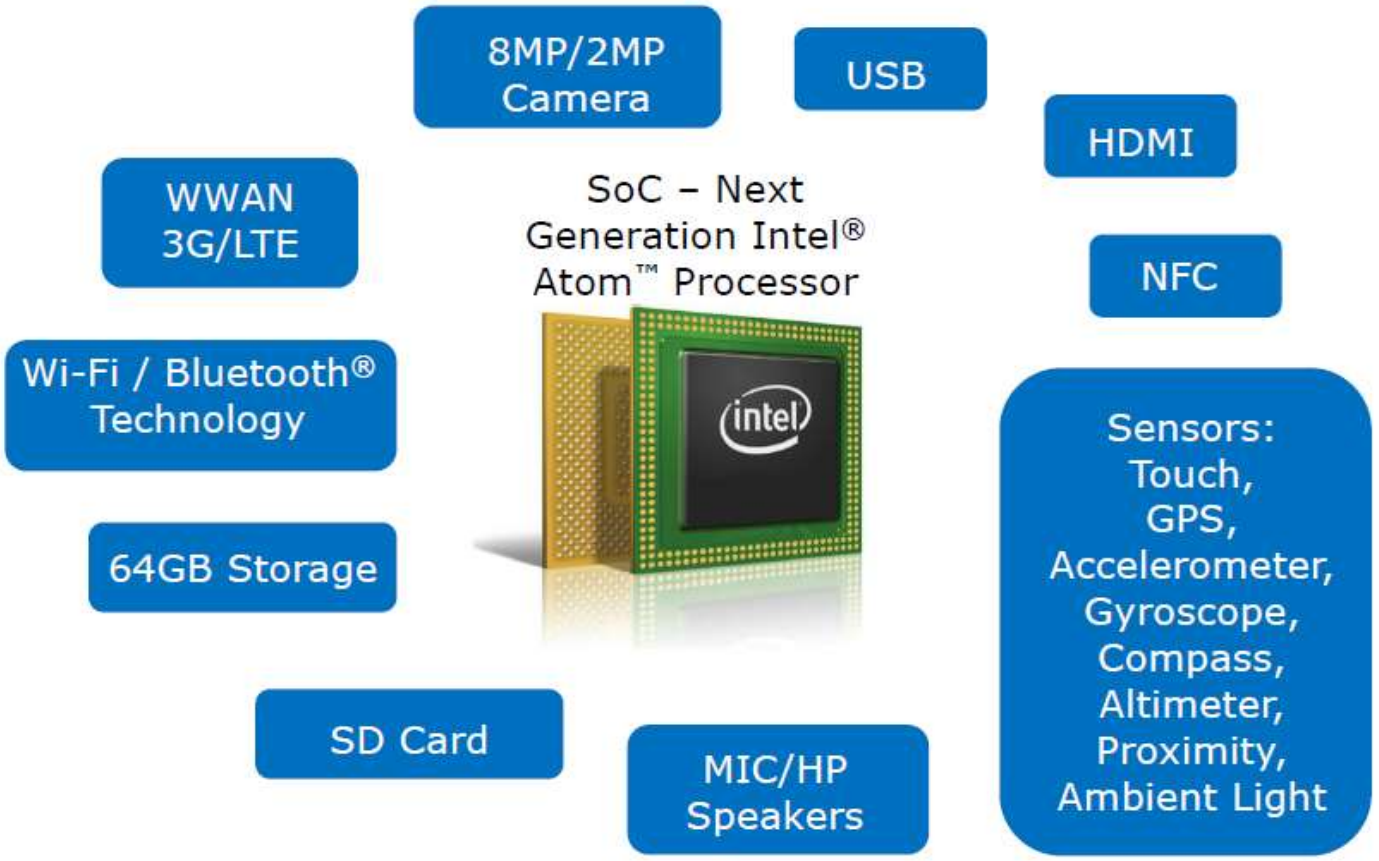
4.4 The Clover Trail platform (11)

More detailed block diagram of the Clover Trail SOC [96]



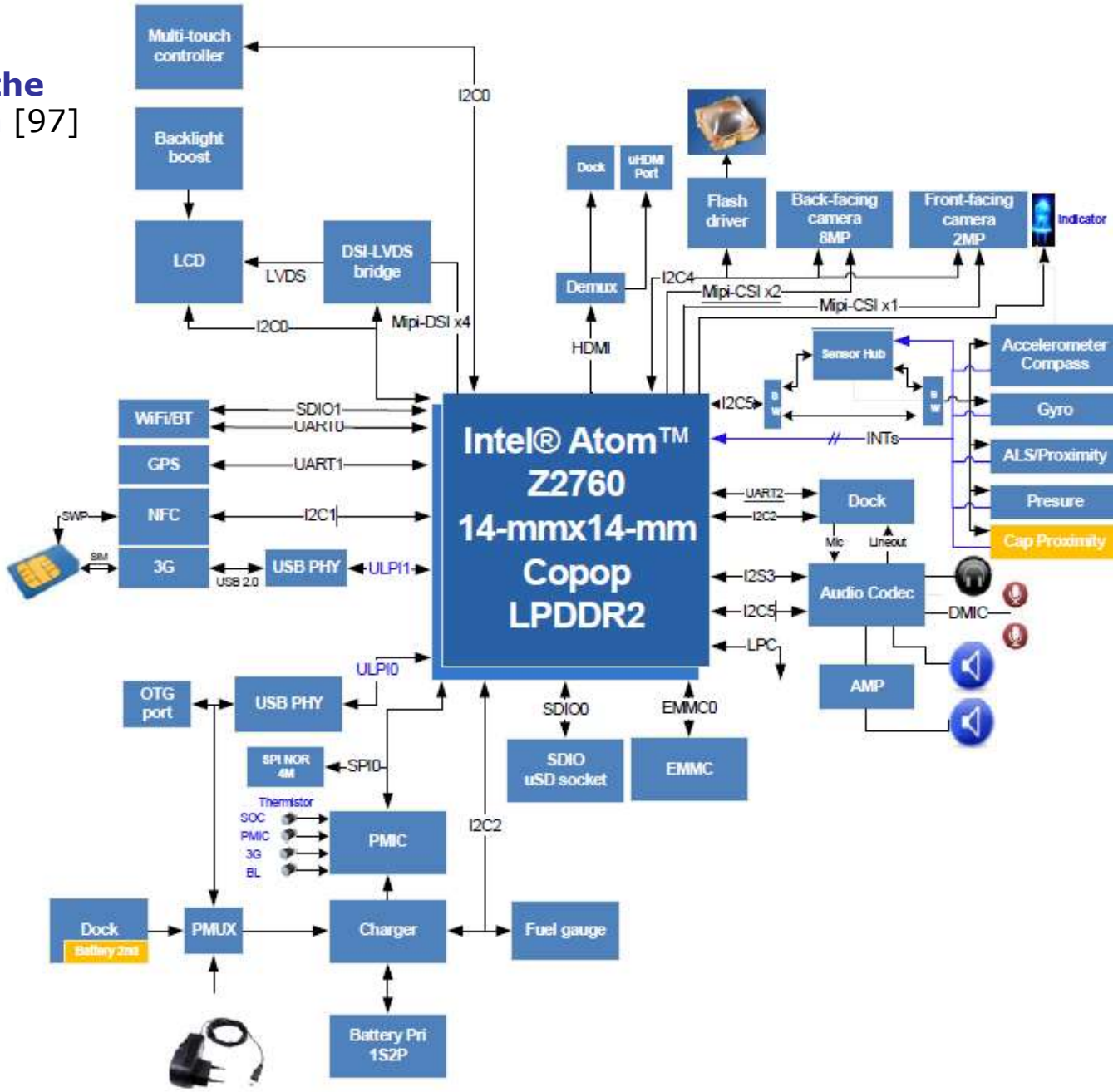
4.4 The Clover Trail platform (12)

Main components of the I/O-systems of the Clover Trail platform [96]



4.4 The Clover Trail platform (13)

Example system block diagram with the Clover Trail platform [97]



4.4 The Clover Trail platform (14)

Main features of the Clover Trail tablet platform

	Menlow	Oak Trail	Clover Trail	Clover Trail+	Bay Trail -T
Available	04/2008	04/2011	12/2012	02/2013	Q9/2013
Focus	MIDs	Tablets	Tablets	Smartphones/tablets	Tablets
Processor	Silverthorne	Lincroft	Cloverview	Cloverview	Valleyview -T
Models	Z5xx	Z650/Z670	Z2760	Z2520-Z2580	Z36xx, Z37xx(D)
Technology	45nm	45nm	32nm	32nm	22nm
Die size	26 mm^2	65 mm2	64 mm2		
No. of trans.	47 mtrs	140 mtrs	432 mtrs		
Micro-arch.	Bonnell	Bonnell	Saltwell	Saltwell	Silvermont
32/64-bit	32-bit	32-bit	32-bit	32-bit	64-bit
1C/2C	1C	1C	2C	2C	2C/4C
HT	HT	HT	HT	HT	no HT
fc [GHz]	0.8-2.13	1.20/1.25	1.50 (1.80 Turbo)	Up to 1.2-2.0 (Turbo)	Up to 1.83-2.41 (Turbo)
L2	512 kB	512 kB	2x512 kB	2x512 kB	2x1 MB
No. of mem.ch.	Single channel MC on SCH	Single channel MC on proc. die (32-bit)	Dual channels MC on proc. die (32-bit)	Dual mem. ch. MC on proc. die (32-bit)	Single/dual mem. channels MC on proc. die (64-bit)
Memory	DDR2-533/400	DDR2-800	LPDDR2-800 (POP)	LPDDR2-1066 (POP)	LPDDR3-1066
GPU	GMA 500 (SGX 535) in PCH (US15W)	GMA 600 (SGX 535) on the proc.	Power VR SGX 545 on the proc	Power VR SGX 544 MP2 on the proc.	Gen 7 DX11 on the proc.
DX	DX 9.0c	DX 9.0c	DX 9.0c	DX 9.x	DX 11
Camera res.	—	—	8 Mpixel	16 Mpixel	
ISP	—	—	ISP 2300	ISP	ISP
Display output	LVDS, SDVO on U515W	LVDS or MIPI-DSI on proc. HDMI 1.3a on SM35	HDMI 1.3a, MIPI-CSI,-2 MIPI-DSI, MIPI-HSI	HDMI 1.3a, MIPI-CSI,-2 MIPI-DSI, MIPI.HSI	HDMI 1.4a, DP 1.2, eDP1.3, MIPI_CSI, MIPI-DSI
GPU clock	400/533 Mb/s	400 MHz	533 MHz	300-533 MHz	
Proc. TDP	0.65-2.5 W	3.0 W	1.7W	2.0-3.0 W	2.0-2.4 W (SDP)
FSB	400/533 MT/s	400 MT/s per dir. cDMI (8-bit)	—	—	—
Socket	PBGA441	BGA 518	FC-MB4760	BGA 760	UTFCBGA1380
Chipset	U515W (Poulsbo)	SM 35 (Whitney Point)	no, SOC	no, SOC	no, SOC
OS	Windows XP/Vista/7 Moblin 1	Windows 7 Home Premium MeeGo, Android	Windows 8 Pro Windows 8	Android 4.2	Windows 8.1 CS (32-bit) Android 4.2.2
Examples	Beng S6 Compal KAX15 Lenovo ideapad U8	Fujitsu Q550 Intel Studybook prototype Motion Computing's CL900 tablet	Acer Iconia W3/W510 Asus VivoTab Dell Latitude 10 HP Envy x2/ElitePad 900 Lenovo Thinkpad Tablet 2 Samsung Series 5 Slate	Asus MeMO Pad FHD 10 / Fonepad Note / Transformer Book Trio Samsung Galaxy Tab3	Acer W3-810 Asus Transformer Book Trio T100 Dell Venue/ Midland Lenovo Miix 8/ Miix 2 Toshiba Encore

4.4 The Clover Trail platform (15)

Key innovations of the Clover Trail platform over the Oak Trail platform

a) Increasing performance through introducing Burst Technology,
b) lowering idle power through introducing the S0i1 and S0i3 system states and
c) implementing POP memory.

4.4 The Clover Trail platform (16)

a) Increasing performance through introducing Burst Technology [111], [112]

The Burst technology of the Clover Trail platform provides about the same benefits as Intel's Turbo Boost technology found in x86-based processors as introduced in the Nehalem family.

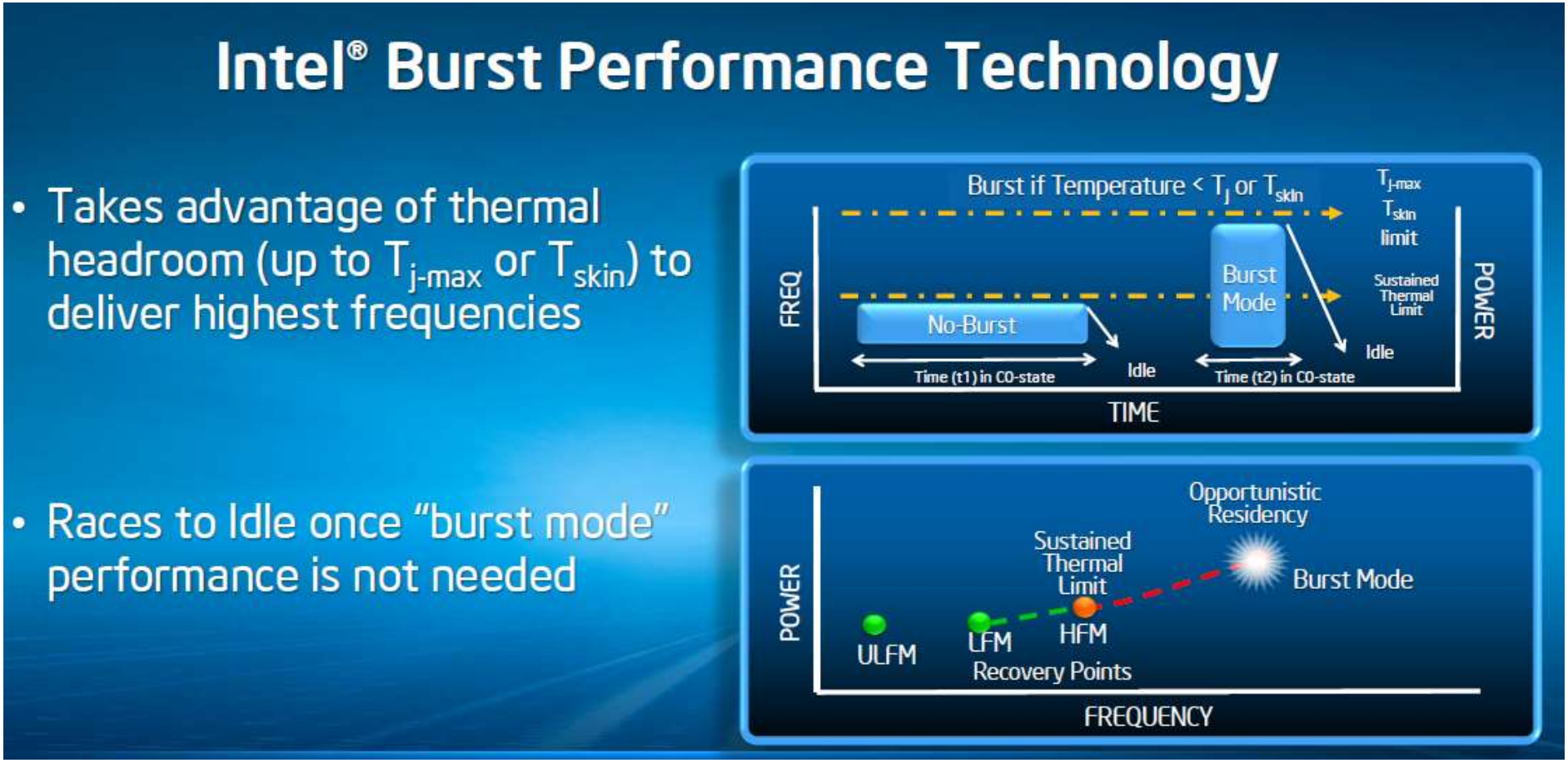
It allows the CPU cores to run at higher clock speed than limited by the TDP (Thermal Design Power) of the chip for short periods of time if

- there is a thermal headroom,
- the OS requests higher performance and
- specified temperature limits (Tjmax (junction temperature) and Tskin (the temperature of the case, like the case of a tablet)

will not be exceeded.

The intended operating mode is to allow the processor to wake up from an idle state, perform the work to be done and return to the idle state as quickly as possible, as indicated in the next Figure.

Principle of the Burst Technology [98]



4.4 The Clover Trail platform (18)

Remark

1) The Burst Technology is not detailed in the associated datasheet.

2) The Skin temperature t_{skin} is the temperature of the case, like the case of a tablet.

If the case becomes hotter than a given temperature it can be unpleasant for the user and thus it should be avoided.

4.4 The Clover Trail platform (19)

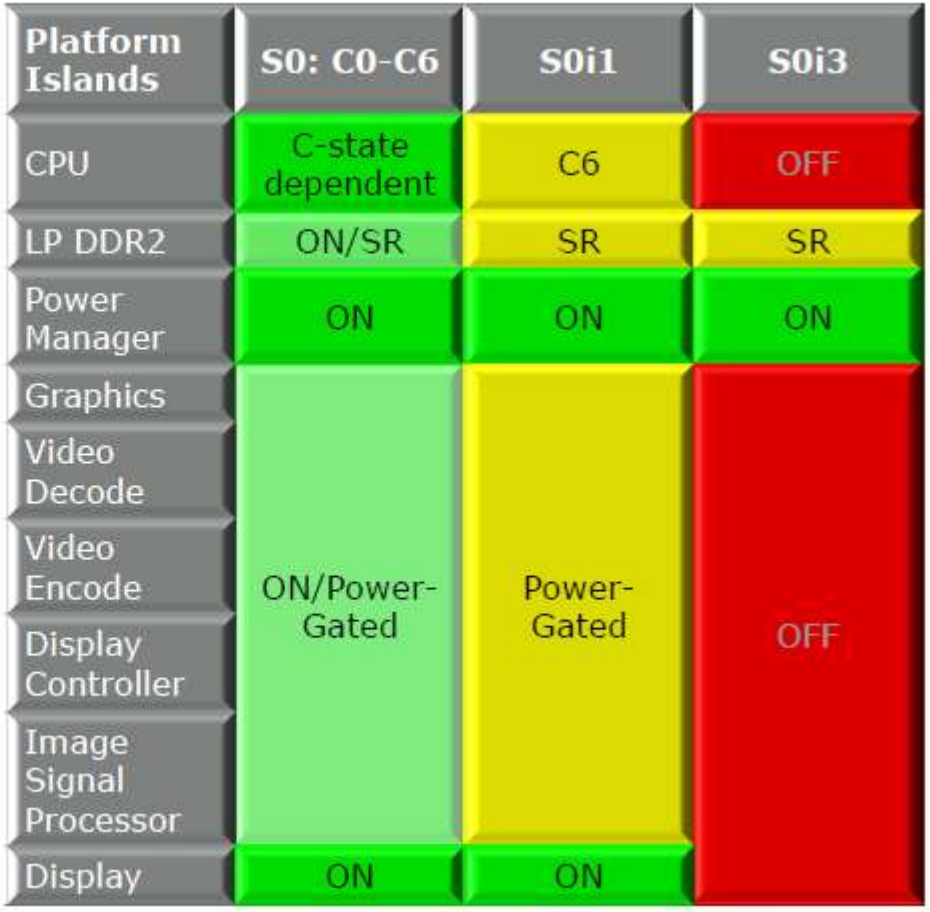
b) Lowering idle power by introducing the S0i1 and S0i3 system states [96]

S0i1

- Used during idle (e.g. home screen, web browsing)
- SoC power: mW
- Entry-Exit Latency: μs

S0i3 (connected standby)

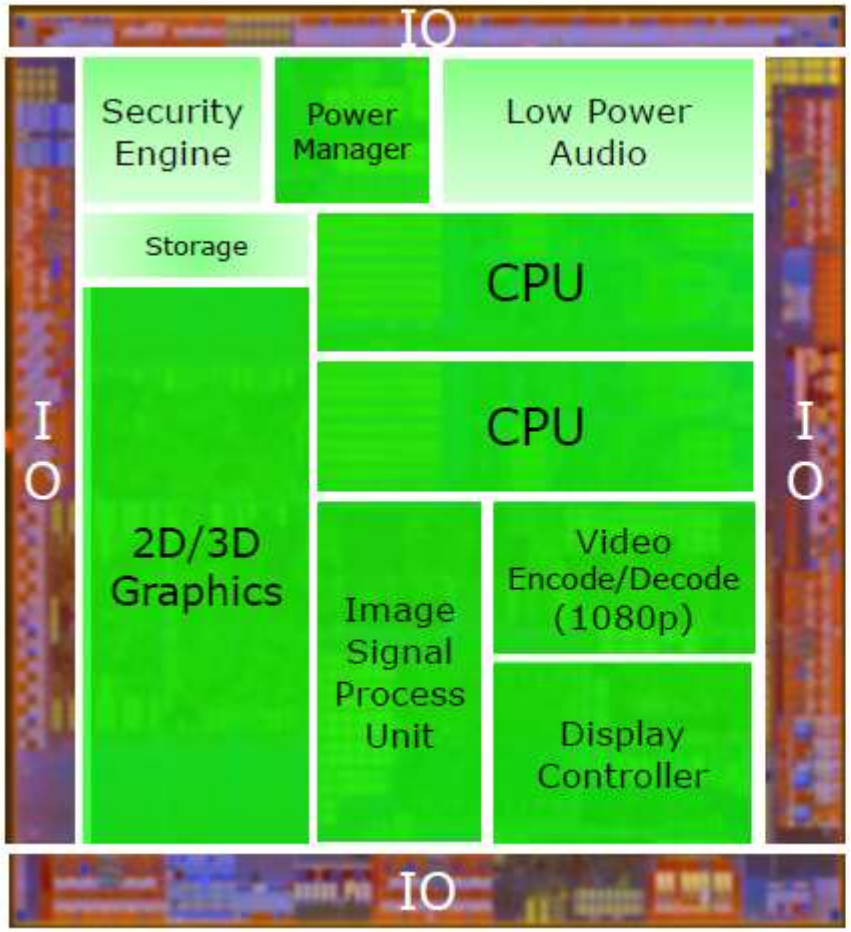
- Used when NOT interacting with the device (e.g., standby mode)
- SoC power: μW
- Entry-Exit Latency: ms

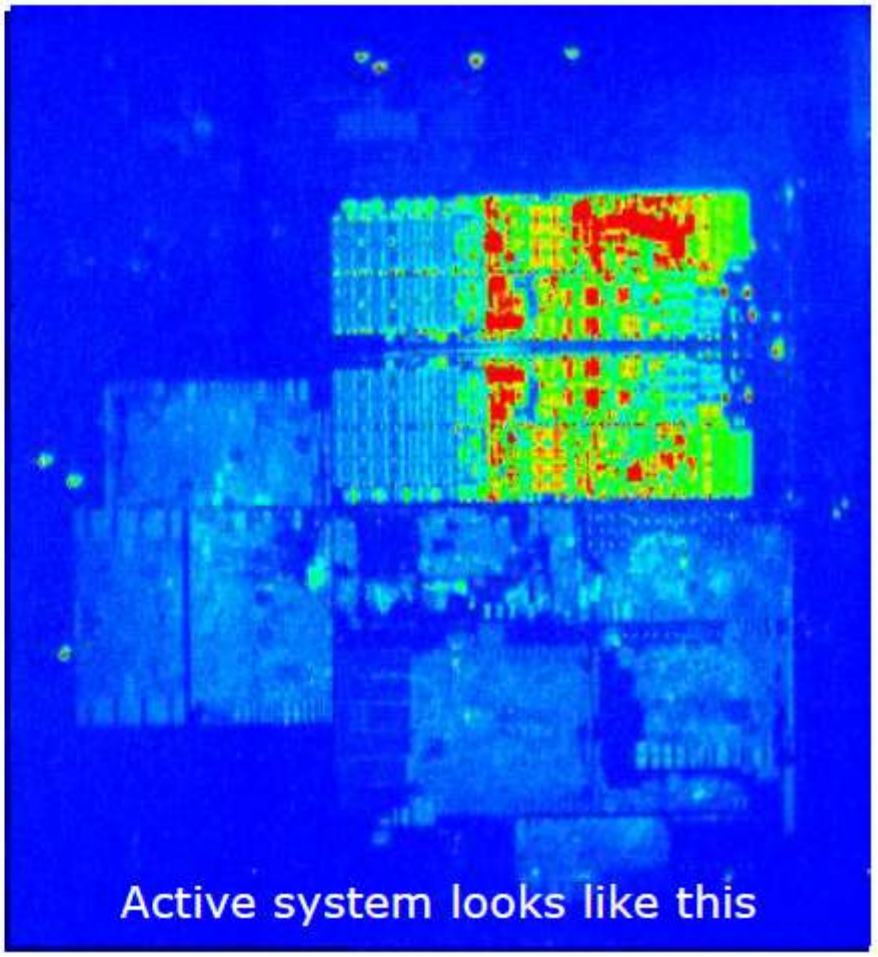


SR: Memory is in Self Refresh state

4.4 The Clover Trail platform (20)

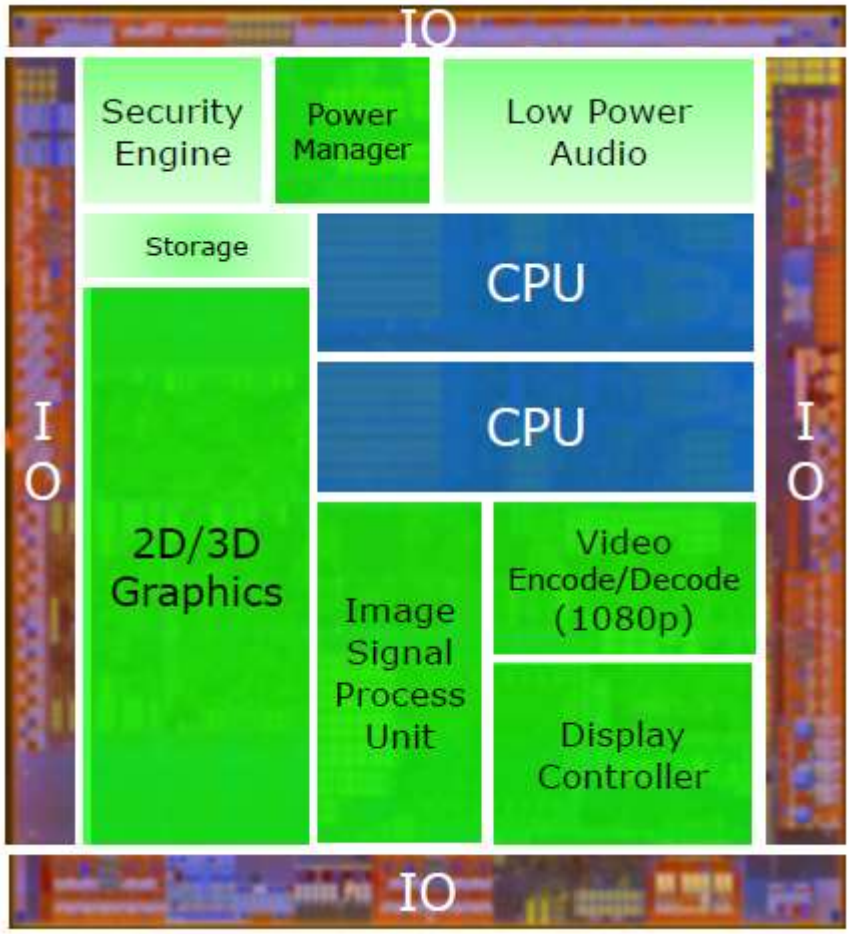
Infrared emission (IREM) image of the Cloverview die when the CPU is active [96]

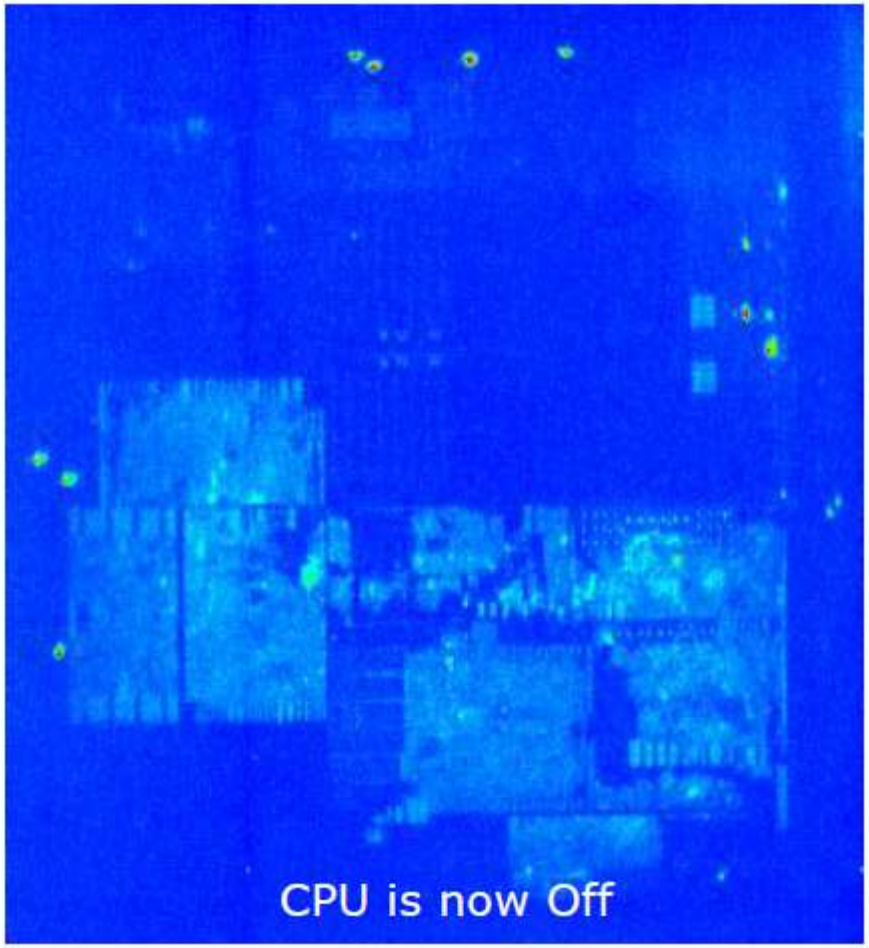




4.4 The Clover Trail platform (21)

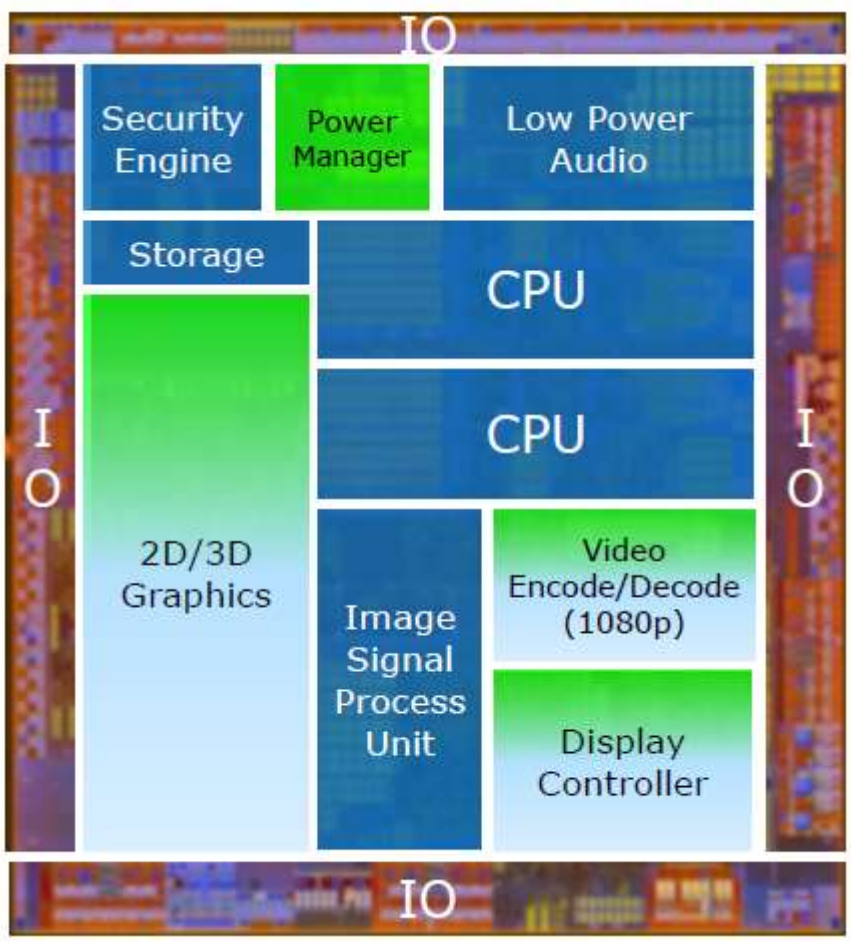
Infrared emission (IREM) image of the Cloverview die when the CPU is off [96]

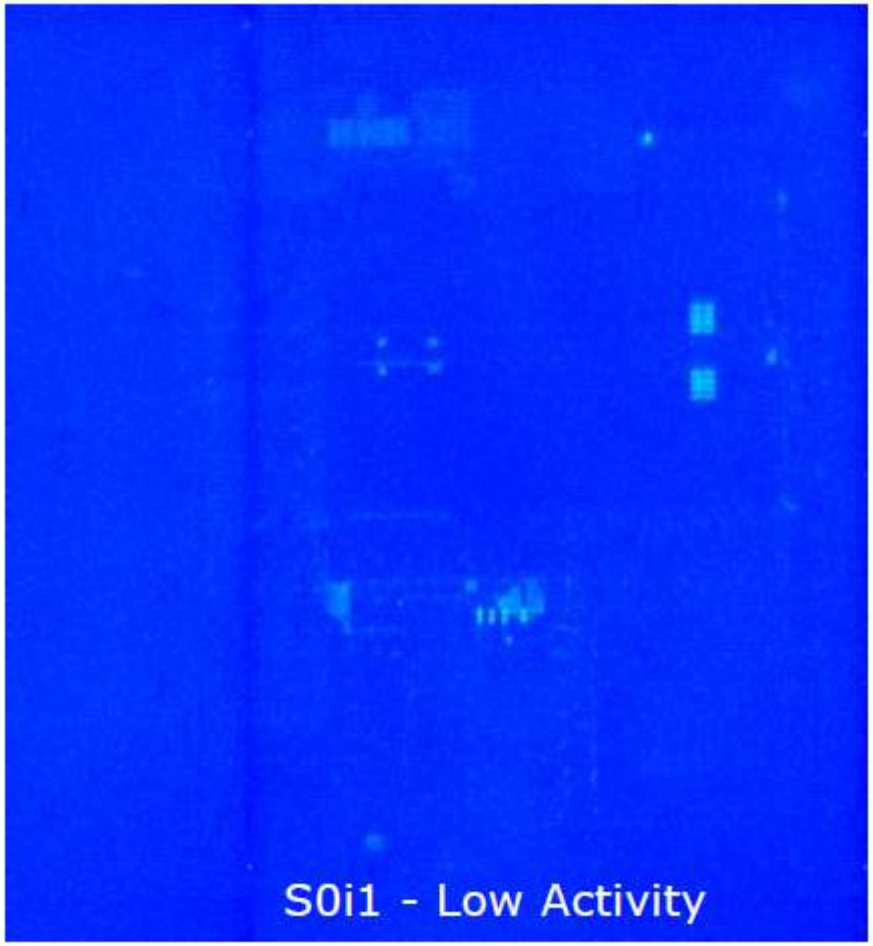




4.4 The Clover Trail platform (22)

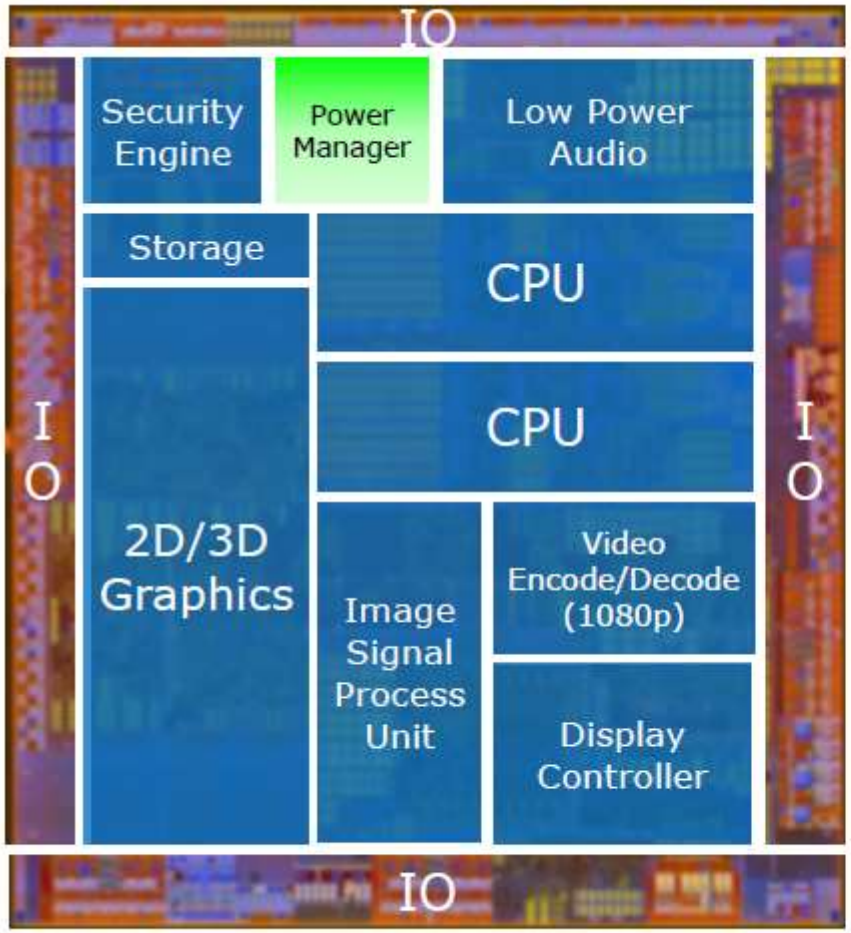
Infrared emission (IREM) image of the Cloverview die in the S0i1 system state [96]

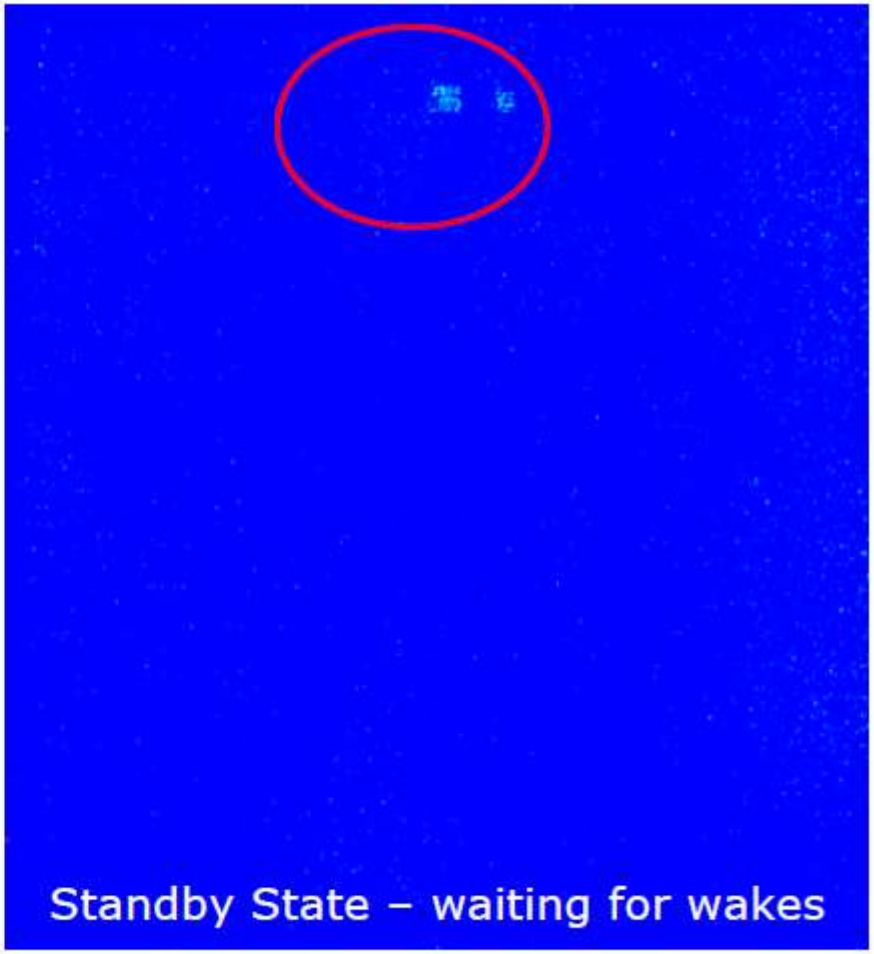




4.4 The Clover Trail platform (23)

Infrared emission (IREM) image of the Cloverview die in the S0i3 system state [96]





Specks are due to detector noise with scaling increase

4.4 The Clover Trail platform (24)

c) Implementing PoP memory [56]

LPDDR2 memory is implemented as Package-on-Package (PoP) design that stacks the LPDDR2 memory chip on top of the SOC die, as shown in the Figure below.

The memory chips are placed on top of the SoC that is soldered on a shared package substrate.

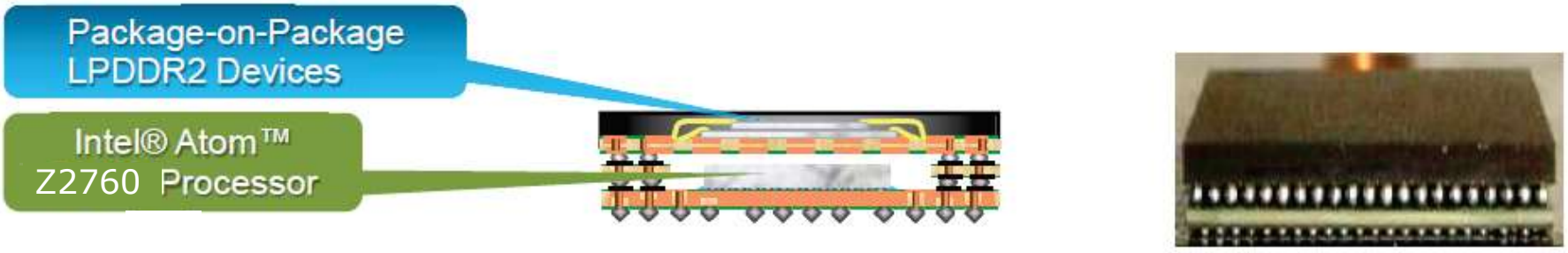


Figure: Package-on-Package memory stacking (based on [56])

Main features of the PoP memory subsystem

- The design allows to implement up to 2 GB stacked memory.
- There are dual 32-bit memory channels available with 800 MT/s LPDDR2 memory, providing a total peak memory bandwidth of 6.4 GB/s.
- The whole PoP stack has a high of 1.4 mm.

Market reception of the Clover Trail platform

There are much more tablet designs based on the Clover Trail platform than on the previous Oak Trail platform.

Nevertheless, as market analysts estimate the ratio of Windows-based tablets is in Q1/2013 as low as about 7 % and this figure is expected to rise only to about 10 % for 2016, so Windows 8-based tablets seems not be able to conquer the tablet market [37], [36].

4.5 The Clover Trail+ platform as used for tablets

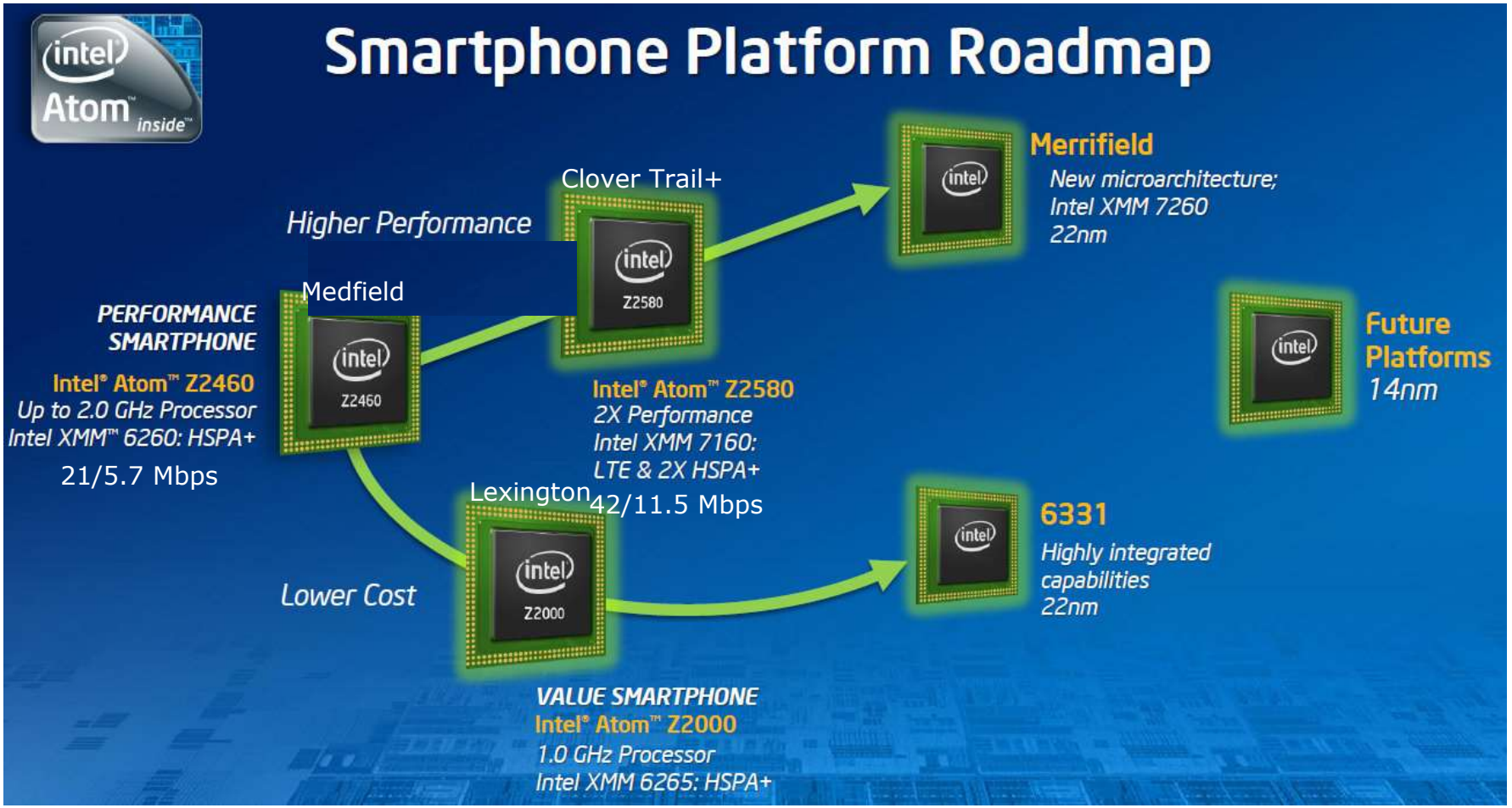
4.5 The Clover Trail+ platform as used for tablets

Introduction

- Disclosed already in Intel's smartphone roadmap from 5/2012 (see next slide).
- Introduced in 2/2013 at the Mobile World Congress (MWC) primarily for Android smartphones, but used also for Android tablets.

4.5 The Clover Trail+ platform as used for tablets (2)

Intel's smartphone roadmap from 5/2012 [176]



4.5 The Clover Trail+ platform as used for tablets (3)

The Clover Trail platform

The Clover Trail+ platform was originally intended for Android-based smart phones whereas the Clover Trail platform for Windows 8-based tablets, as indicated in a roadmap from 11/2012 (see next slide).

4.5 The Clover Trail+ platform as used for tablets (4)

Intel's tablet and smartphone roadmap from 11/2012 [114]

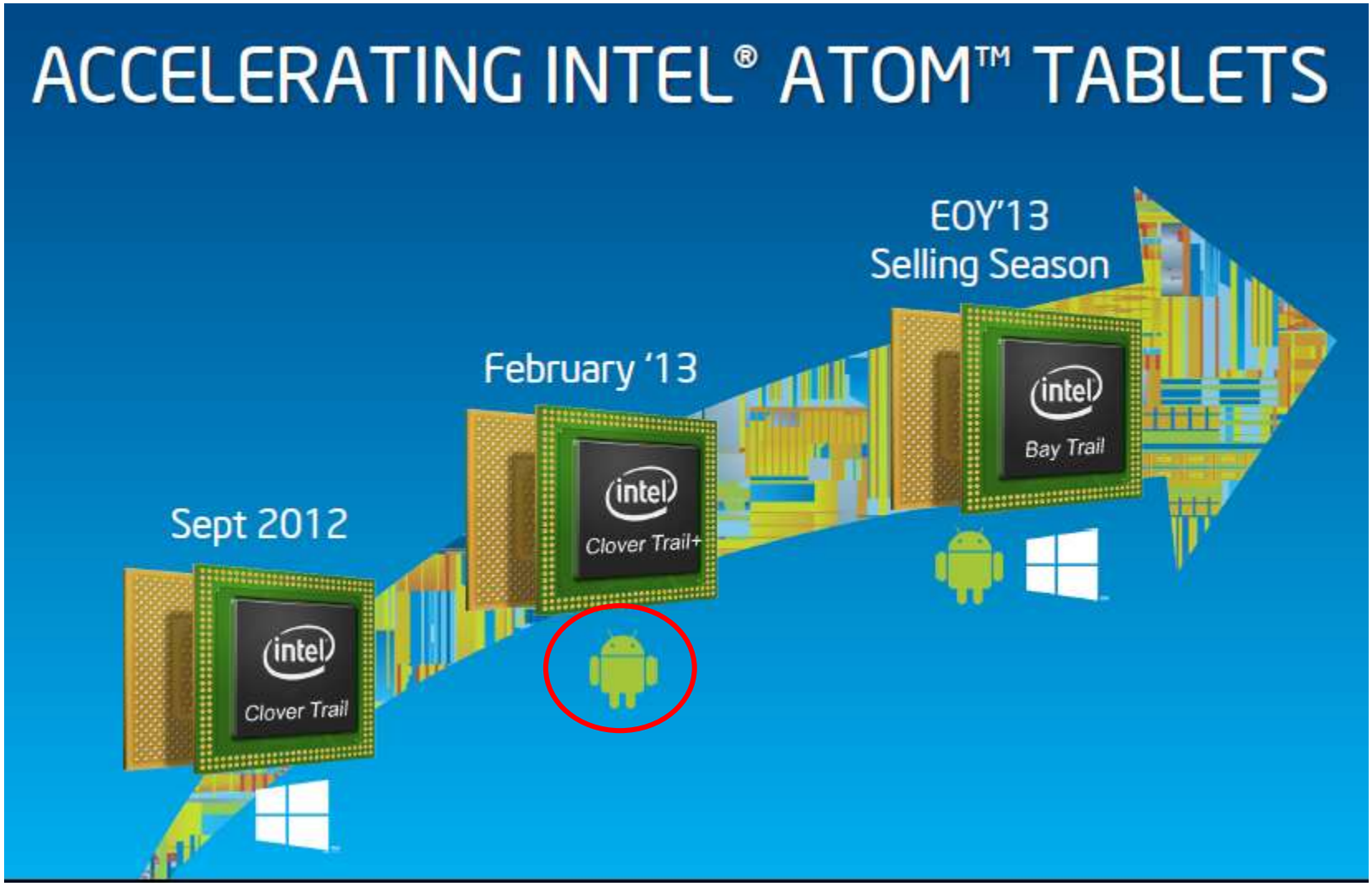
4.5 The Clover Trail+ platform as used for tablets (5)

Use of the Clover Trail+ platform for tablets as well

In 6/2013 (at their Shareholders meeting) Intel disclosed plans to make use of the Clover Trail+ platform as a basis for Android tablets as well, as seen below.

4.5 The Clover Trail+ platform as used for tablets (6)

Intel's plan to make use of the Clover Trail+ platform for introducing Android tablets into the market [115]



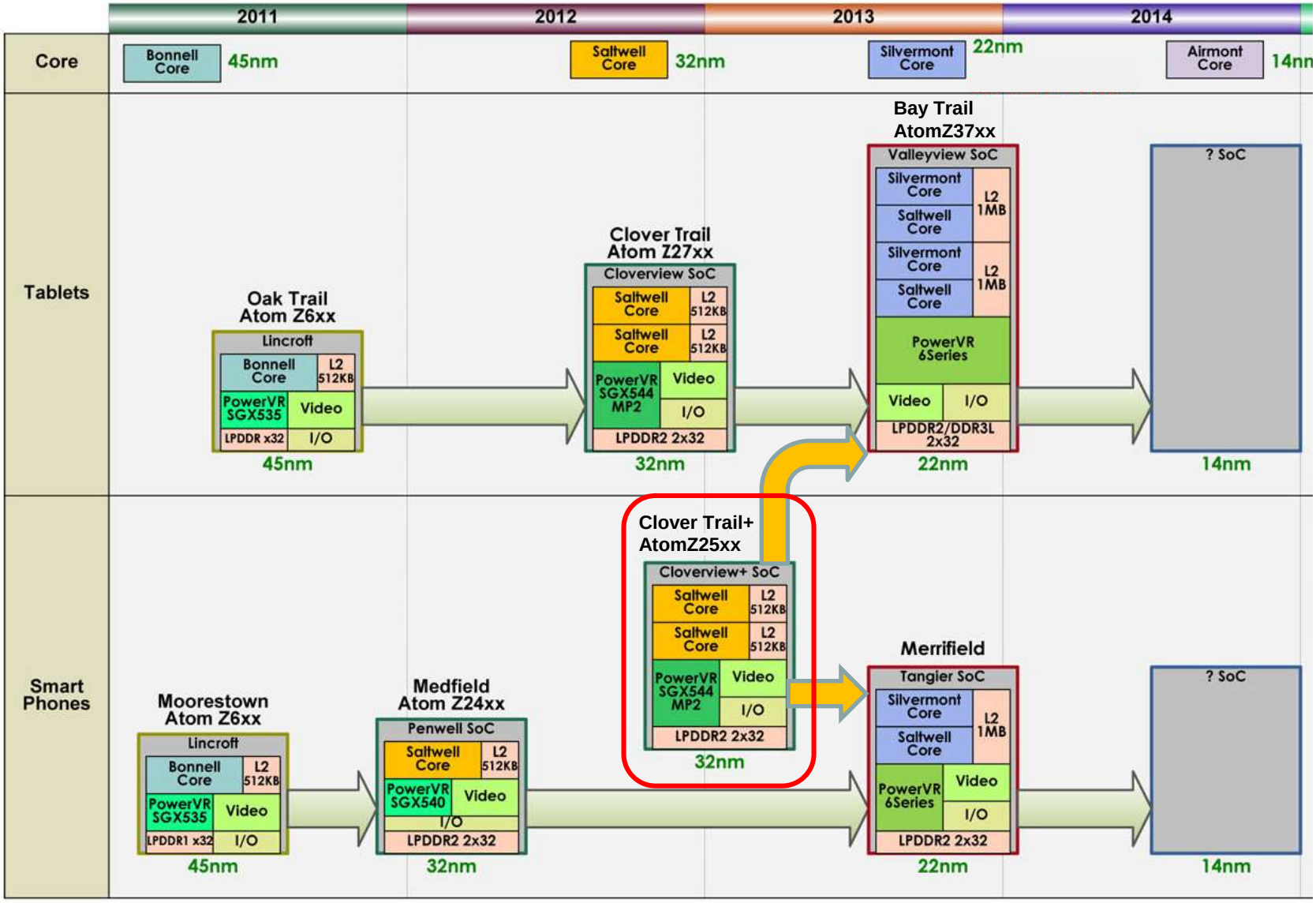
4.5 The Clover Trail+ platform as used for tablets (7)

Note

Although the Clover Trail+ platform was disclosed first for Android smartphones (5/2012), it is used now for both Android-based tablets and smartphones.

4.5 The Clover Trail+ platform as used for tablets (8)

Positioning the Clover Trail+ platform in Intel's tablet and smart phone platforms [110]



4.5 The Clover Trail+ platform as used for tablets (9)

Differences between the Clover Trail and the Clover Trail+ platforms

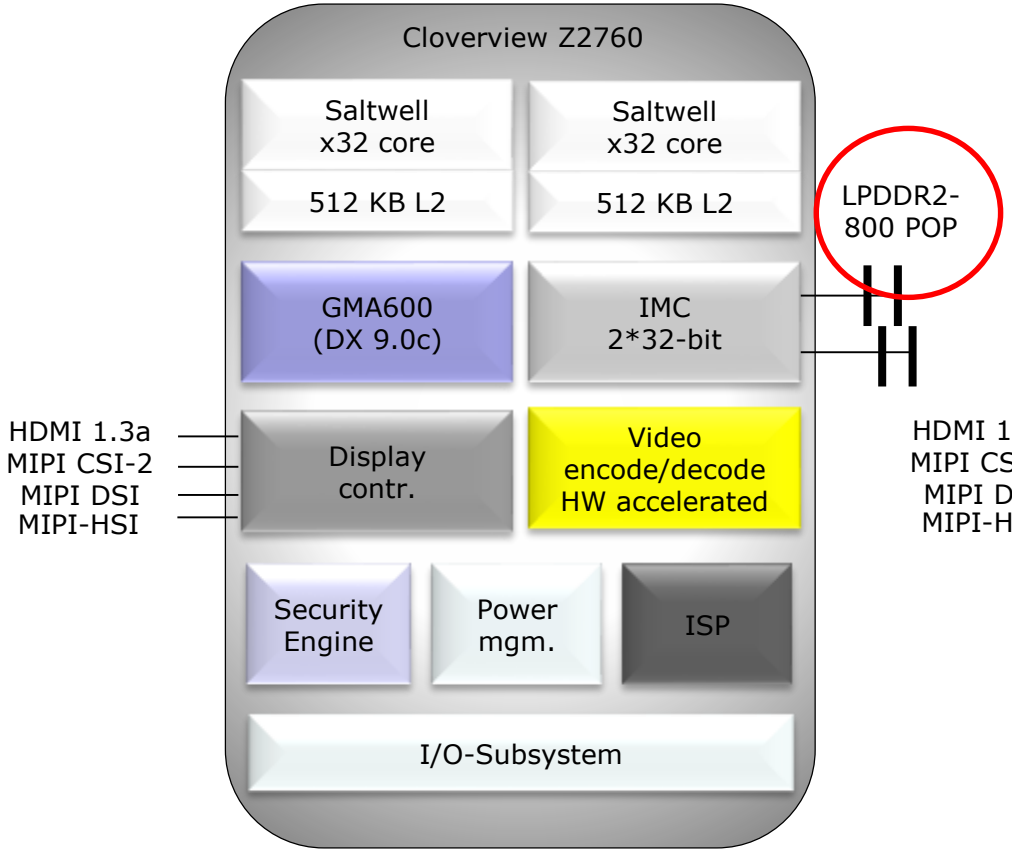


Figure: The Cloverview processor

Optimized for Windows 8

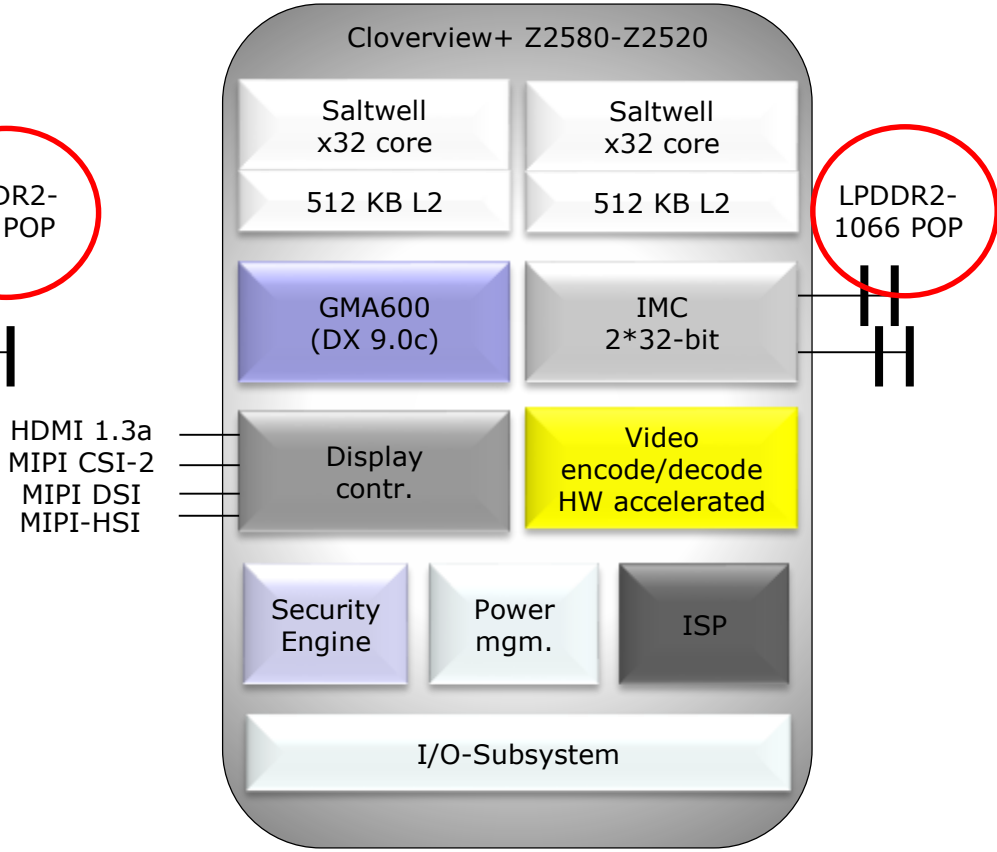


Figure: The Cloverview+ processor

Optimized for Android 4.2

4.5 The Clover Trail+ platform as used for tablets (10)

Note

The main difference of the Clover Trail+ and the Clover Trail platforms is that the former is optimized for Android and the latter for Windows 8.1.

4.5 The Clover Trail+ platform as used for tablets (11)

Main features of the Clover Trail+ models introduced [116]

	Z2580	Z2560	Z2520
CPU Frequency	Up to 2.0Ghz	Up to 1.6Ghz	Up to 1.2Ghz
Process Tech	32nm		
CPU performance	Dual Core with HT (4 Threads)		
Memory	LPDDR2 2x32-bit 1066MTS		
Video Dec/Enc	1080p30 /1080p30		
Enhanced Video codecs	MPEG-4,H.264,DivX,VC-1,WMV-9,VP6		
Enhanced Audio codecs	AMR-NB AMR-WB AAC , MP3 MIDI, WMA		
Display support	WUXGA (1920x1200)		
Graphics	SGX 544MP2 533 MHz Boost	SGX 544MP2 400 MHz	SGX 544MP2 300 MHz
Camera	Primary: 16MP; Secondary: 2MP		
Advanced imaging features	Continuous shooting, continuous viewfinder, mobile HDR, 2-axis DVS		
Modem	XMM™ 6360		

Remark

For comparison, the Clover Trail based Z2460 has a clock frequency of 1.5 GHz.

4.5 The Clover Trail+ platform as used for tablets (12)

Main features of the Clover Trail+ platform while used for tablets

	Menlow	Oak Trail	Clover Trail	Clover Trail+	Bay Trail -T
Available	04/2008	04/2011	12/2012	02/2013	Q9/2013
Focus	MIDs	Tablets	Tablets	Smartphones/tablets	Tablets
Processor	Silverthorne	Lincroft	Cloverview	Cloverview	Valleyview -T
Models	Z5xx	Z650/Z670	Z2760	Z2520-Z2580	Z36xx, Z37xx(D)
Technology	45nm	45nm	32nm	32nm	22nm
Die size	26 mm^2	65 mm2	64 mm2		
No. of trans.	47 mtrs	140 mtrs	432 mtrs		
Micro-arch.	Bonnell	Bonnell	Saltwell	Saltwell	Silvermont
32/64-bit	32-bit	32-bit	32-bit	32-bit	64-bit
1C/2C	1C	1C	2C	2C	2C/4C
HT	HT	HT	HT	HT	no HT
fc [GHz]	0.8-2.13	1.20/1.25	1.50 (1.80 Turbo)	Up to 1.2-2.0 (Turbo)	Up to 1.83-2.41 (Turbo)
L2	512 kB	512 kB	2x512 kB	2x512 kB	2x1 MB
No. of mem.ch.	Single channel MC on SCH	Single channel MC on proc. die (32-bit)	Dual channels MC on proc. die (32-bit)	Dual mem. ch. MC on proc. die (32-bit)	Single/dual mem. channels MC on proc. die (64-bit)
Memory	DDR2-533/400	DDR2-800	LPDDR2-800 (POP)	LPDDR2-1066 (POP)	LPDDR3-1066
GPU	GMA 500 (SGX 535) in PCH (US15W)	GMA 600 (SGX 535) on the proc.	Power VR SGX 545 on the proc	Power VR SGX 544 MP2 on the proc.	Gen 7 DX11 on the proc.
DX	DX 9.0c	DX 9.0c	DX 9.0c	DX 9.x	DX 11
Camera res.	–	–	8 Mpixel	16 Mpixel	
ISP	–	–	ISP 2300	ISP	ISP
Display output	LVDS, SDVO on U515W	LVDS or MIPI-DSI on proc. HDMI 1.3a on SM35	HDMI 1.3a, MIPI-CSI,-2 MIPI-DSI, MIPI-HSI	HDMI 1.3a, MIPI-CSI,-2 MIPI-DSI, MIPI.HSI	HDMI 1.4a, DP 1.2, eDP1.3, MIPI_CSI, MIPI-DSI
GPU clock	400/533 Mb/s	400 MHz	533 MHz	300-533 MHz	
Proc. TDP	0.65-2.5 W	3.0 W	1.7W	2.0-3.0 W	2.0-2.4 W (SDP)
FSB	400/533 MT/s	400 MT/s per dir. cDMI (8-bit)	–	–	–
Socket	PBGA441	BGA 518	FC-MB4760	BGA 760	UTFCBGA1380
Chipset	U515W (Poulsbo)	SM 35 (Whitney Point)	no, SOC	no, SOC	no, SOC
OS	Windows XP/Vista/7 Moblin 1	Windows 7 Home Premium MeeGo, Android	Windows 8 Pro Windows 8	Android 4.2	Windows 8.1 CS (32-bit) Android 4.2.2
Examples	Beng S6 Compal KAX15 Lenovo ideapad U8	Fujitsu Q550 Intel Studybook prototype Motion Computing's CL900 tablet	Acer Iconia W3/W510 Asus VivoTab Dell Latitude 10 HP Envy x2/ElitePad 900 Lenovo Thinkpad Tablet 2 Samsung Series 5 Slate	Asus MeMO Pad FHD 10 / Fonepad Note / Transformer Book Trio Samsung Galaxy Tab3	Acer W3-810 Asus Transformer Book Trio T100 Dell Venue/ Midland Lenovo Miix 8/ Miix 2 Toshiba Encore

4.5 The Clover Trail+ platform as used for tablets (13)

Market acceptance of the Clover Trail+ platform for Android tablets

There are only a few Android tablets that are based on specific models of Intel's Clover Trail+ family, such as the

- Samsung's GALAXY Tab 3 10.1
- ASUS MeMO Pad FHD 10
- ASUS's 6-inch Fonepad Note
- ASUS's 11.6-inch Transformer Book Trio

All in all, with the Clover Trail+ platform Intel could not yet achieve a noteworthy market share in the tablet space.

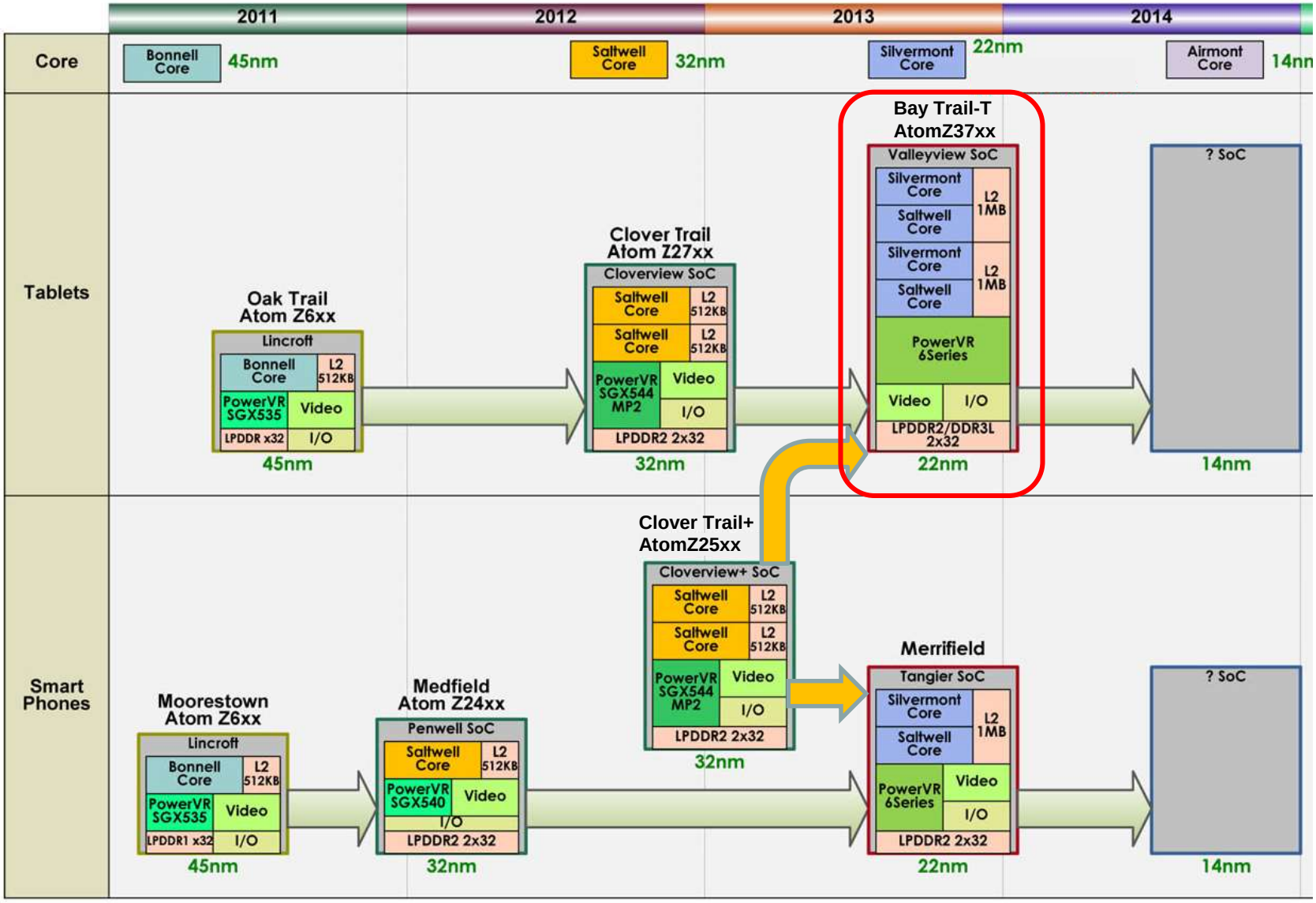
4.6 The Bay Trail-T platform

4.6 The Bay Trail-T platform

- Announced: 5/2013
- Launched: 9/2013
- Tablets built upon the Bay Trail-T platform are expected in Q4/2013
- Based on the 22 nm Silvermont CPU, it is Intel's next generation SOC platform for tablets and convertibles, as indicated in the Figure.

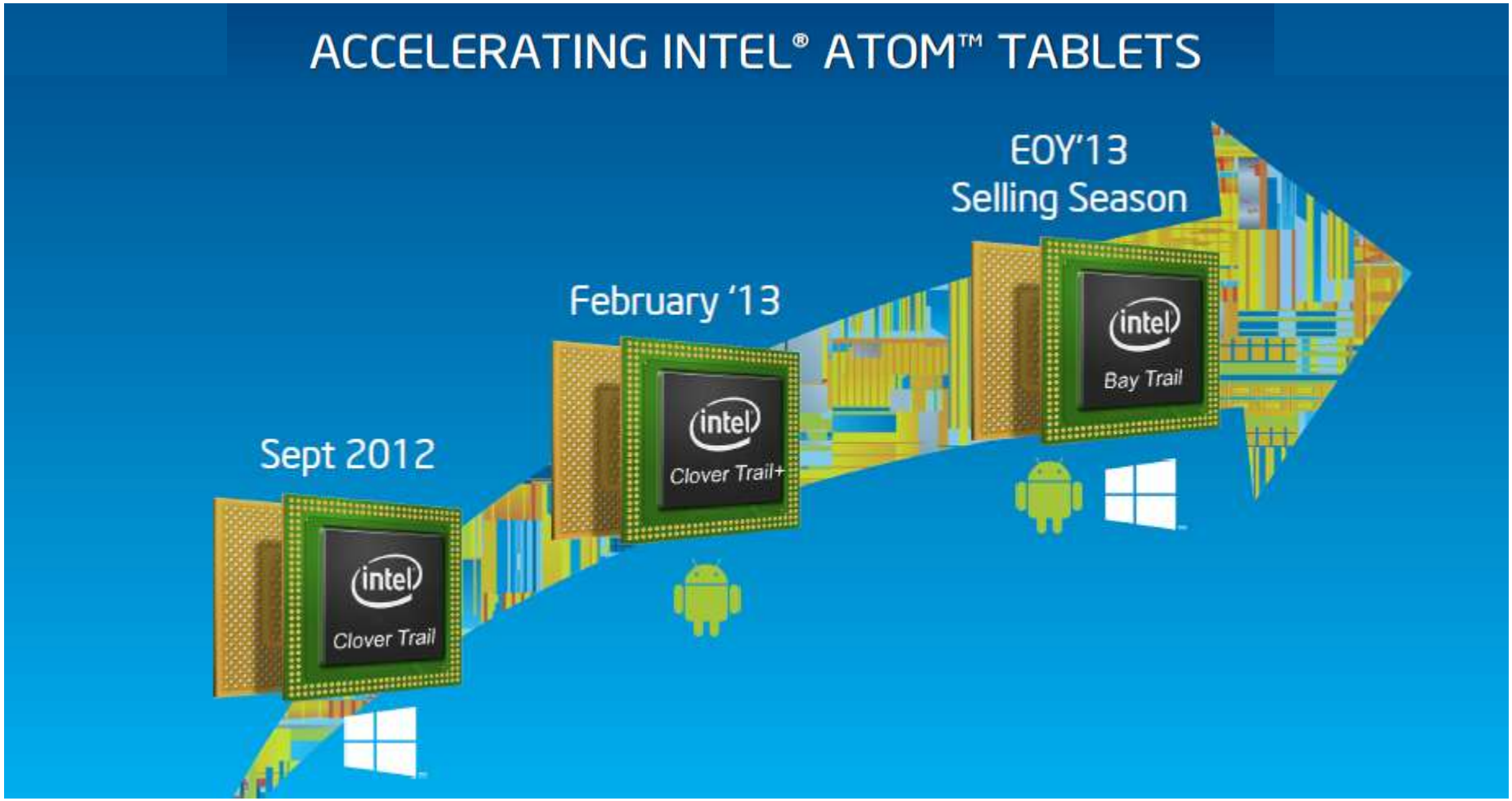
4.6 The Bay Trail-T platform (2)

Positioning the Bay Trail-T platform in Intel's tablet and smart phone platforms [110]



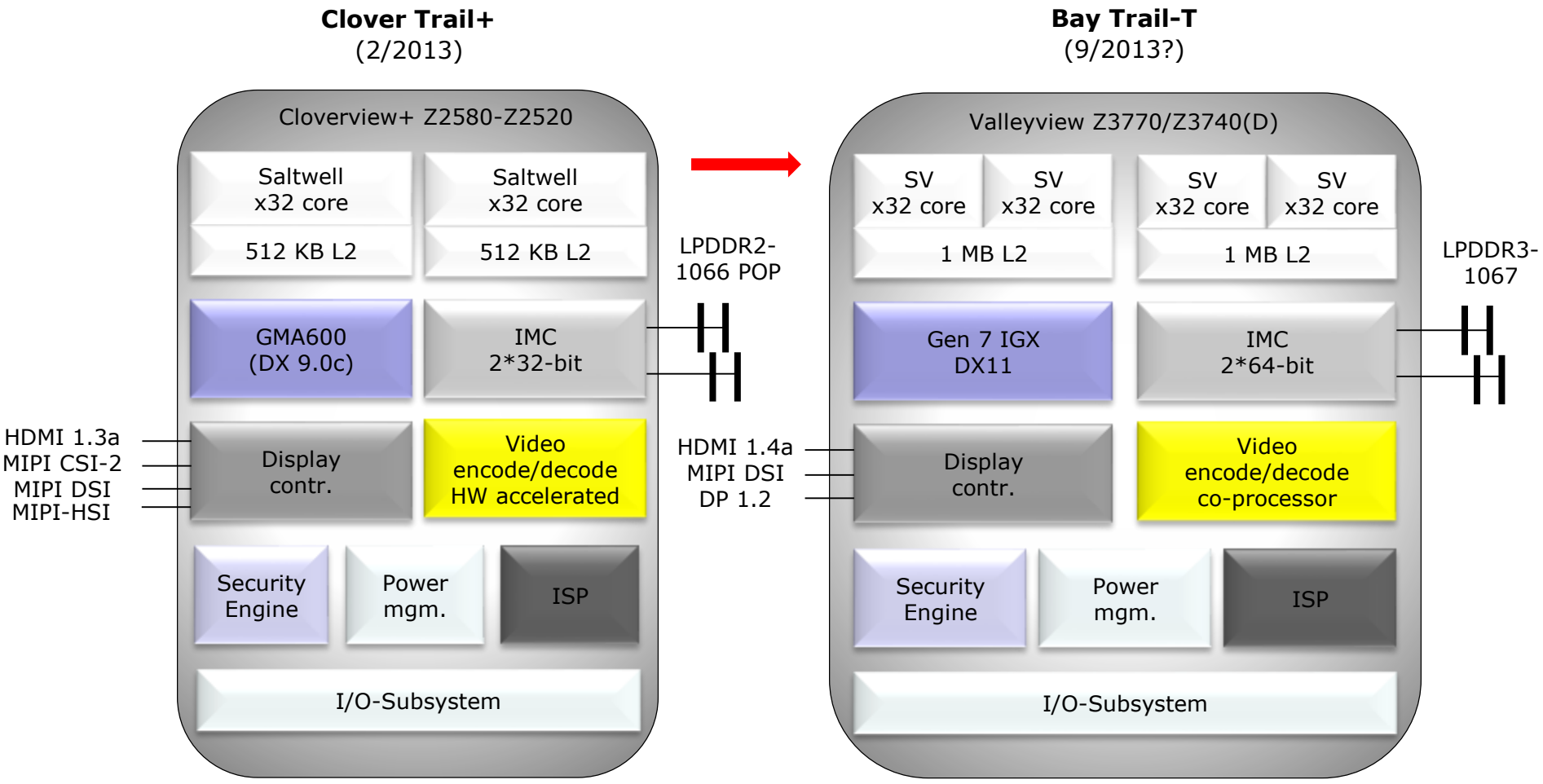
4.6 The Bay Trail-T platform (3)

Evolution of Intel's more recent tablet platforms [115]



4.6 The Bay Trail-T platform (4)

Contrasting the Clover Trail+ and the Bay Trail-T platforms



Optimized for Android 4.2

Optimized for Windows 8.1 and Android 4.2.2

4.6 The Bay Trail-T platform (5)

Remark [117]

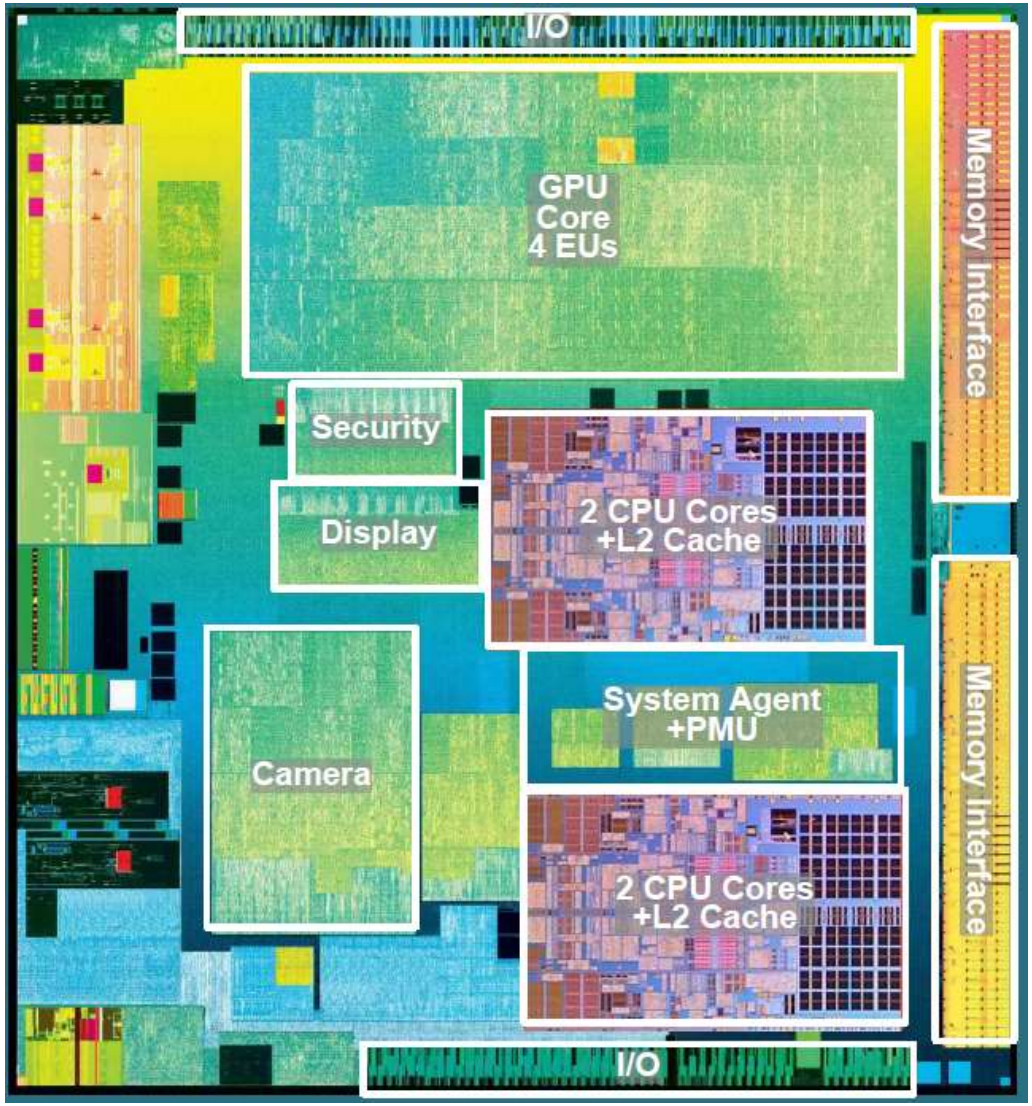
Although the Silvermont-based Bay Trail-T processor is a 64-bit design, 64-bit software support won't be present in devices launched first.

This is not a problem in low end devices targeting the 32-bit only Android OS, but Windows 8.1 devices may miss 64-bit support.

Intel did not revealed yet when 64-bit support will hit the market.

4.6 The Bay Trail-T platform (6)

Die plot and floor plan of the Z37xx processors [141]



4.6 The Bay Trail-T platform (7)

Major enhancements of the Bay Trail-T line vs. the Clover Trail+ line [118]

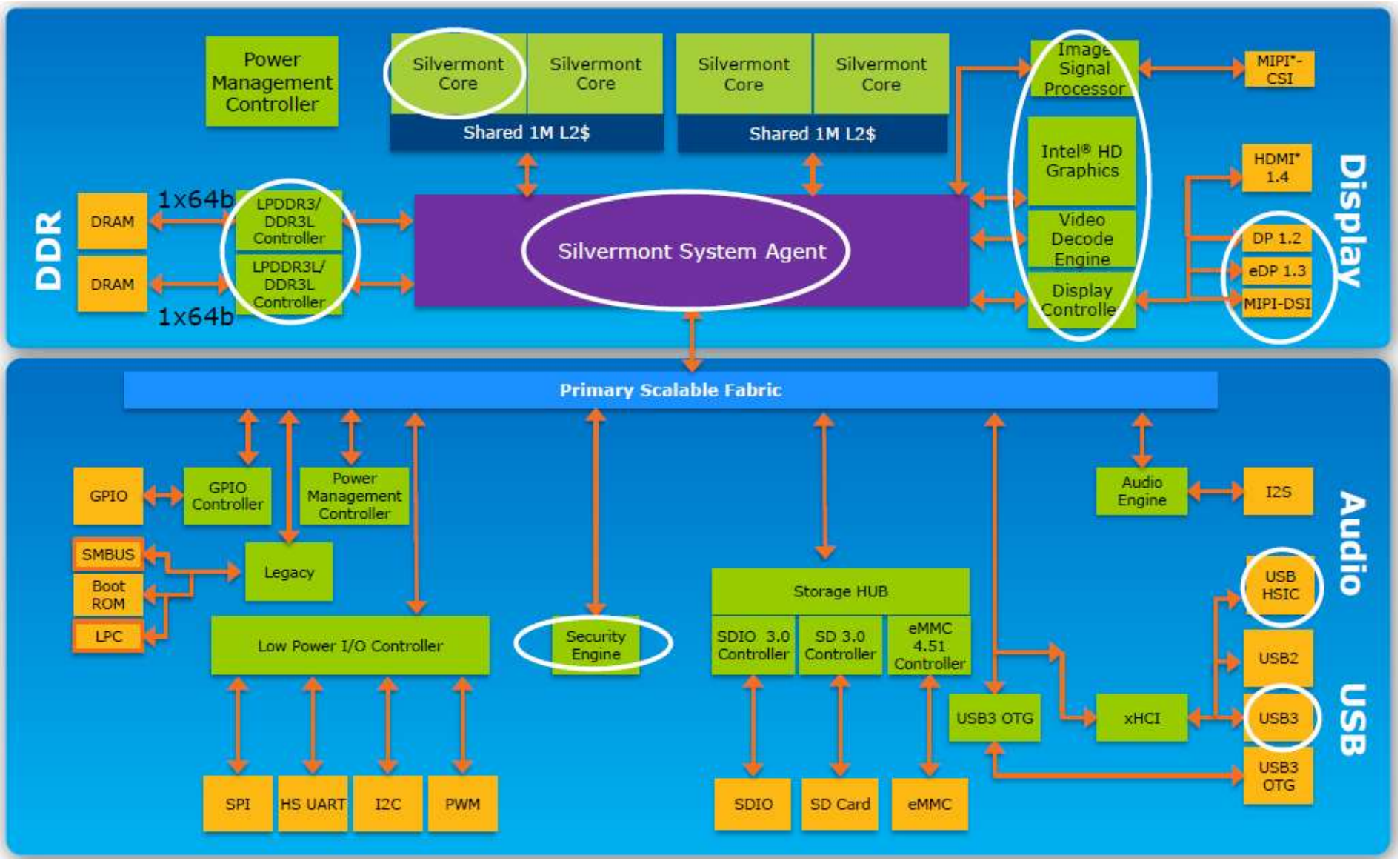
	Clover Trail+	Bay Trail-T
Process	32nm	22nm
Package	14x14	17x17
OS	Android*	Android & Windows*
CPU	Intel® Atom™ 2 cores 4 threads 2GHz	Intel Silvermont Quad Core 2.4GHz, 2M L2
Graphics	SGX 544MP2 @ 400-533MHz	Intel® HD Graphics Gen 7 >= 667MHZ
Display	4 MIPI* DSI 1Gbps/lane, Intel® DPST 3.0, DSR	8 MIPI DSI 1Gbps/lane. 4 lanes eDP 1.3, Intel DPST 6.0, PSR/DSR, DRRS
Internal Display	Up to 19x12	Up to 25x16
External Display	1080p30	1080p60
Memory	LPDDR2 (COPoP) 2x32bit, up to 2GB	LPDDR3 (BGA) 2x64 bit, up to 4GB DDR3L-RS (BGA) 1x64 bit, up to 2GB
Memory BW	8.5GB/s	17GB/s
I/O & Storage	USB 2.0 eMMC 4.41	USB 3.0, USB HSIC eMMC 4.5, SD 3.0
Intel Modem	Intel® XXM™ 7160	Intel XXM 7160

Comparing features of the Bay Trail-T/M/D platforms [82]

	Bay Trail-T	Bay Trail-M	Bay Trail-D
CPU naming	Valleyview - T	Valleyview - M	Valleyview - D
Die Process	22nm	22nm	22nm
Package Size	17x17mm	27x25mm	27x25mm
Max C-state	C7 (S0ix)	C7	C0, C1
Memory	LPDDR3 -1066 up to 4GB	DDR3L & DDR3L RS-1066 up to 8GB	DDR3L -1333 up to 8GB
Graphics	Gen7 DX11, OGL 3.2 Gfx with Burst Technology[1]	Gen7 DX11, OGL 3.2 Gfx with Burst Technology[1]	Gen7 DX11, OGL 3.2 Gfx with Burst Technology[1]
Display	MIPI-DSI (2560x1600), eDP (2560x1600), HDMI rev1.4	HDMI 1.4a, eDP, DP 1.2 2500x1600 @ 60Hz max res	HDMI 1.4a, eDP, DP 1.2 2500x1600 @ 60Hz max res
Video Encode/ Decode	Full HW acceleration for encode of H.264, H.263 MPEG2, MVC Up to 1080p decode. VXD392, MVC, VP8 & JPEG/MJPEG, MPEG2, h.264, VC-1/WMV9	Full HW acceleration for encode of H.264, MPEG2, MVC Up to 1080p decode. VXD392, MVC, VP8 & JPEG/MJPEG, MPEG2, h.264, VC-1/WMV9	Full HW acceleration for encode of H.264, MPEG2, MVC Up to 1080p decode. VXD392, MVC, VP8 & JPEG/MJPEG, MPEG2, h.264, VC-1/WMV9
I/O	MIPI_CSI, ISP 2.0 up to 16-24MP, Stereoscopic video 1080p60, USB 2.0 & USB3.0, USB3.0 OTG, USB HSIC, MIPI HIS, ULPI, eMMC 4.5, SDIO 3.0, HSUART, I2S, I2C, SPI, LPE	PCIe 2.0, SATA 2.0, USB 2.0 & USB3.0, GbE, eMMC 4.5, SDIO 3.0, HSUART, I2S, I2C, SPI, HD Audio	PCIe 2.0, SATA 2.0, USB 2.0 & USB3.0, GbE, eMMC 4.5, SDIO 3.0, HSUART, I2S, I2C, SPI, HD Audio
Security	Secure Boot, Anti theft, virus & Malware Protection baseline, One time Password, WYSIWY, PP-DRNG, Isolation SMEP, B-Crypt, AES-NI, fTPM, NfFC, PAVP 2.0	Secure Boot, virus & Malware Protection baseline, PP-DRNG, SMEP, B-Crypt, AES-NI, fTPM, PAVP 2.0	Secure Boot, virus & Malware Protection baseline, PP-DRNG, SMEP, B-Crypt, fTPM, PAVP 2.0
TDP Targets SOC	Valleyview-T: ≤3W	Valleyview-M: ≤4-6.5W	Valleyview-D: ≤12W
OS	WIN 8 CS (32 bits)	WIN 8 non CS (32 & 64 bits), Win8 CS (32bit)**, Win 7**, Chrome**	WIN 8 non CS (32 & 64 bits)**, Win 7**, Linux**

4.6 The Bay Trail-T platform (9)

Intel's Bay Trail-T tablet platform [118]



4.6 The Bay Trail-T platform (10)

Main features of the Bay Trail tablet platform

	Menlow	Oak Trail	Clover Trail	Clover Trail+	Bay Trail -T
Available	04/2008	04/2011	12/2012	02/2013	Q9/2013
Focus	MIDs	Tablets	Tablets	Smartphones/tablets	Tablets
Processor	Silverthorne	Lincroft	Cloverview	Cloverview	Valleyview -T
Models	Z5xx	Z650/Z670	Z2760	Z2520-Z2580	Z36xx, Z37xx(D)
Technology	45nm	45nm	32nm	32nm	22nm
Die size	26 mm^2	65 mm2	64 mm2		
No. of trans.	47 mtrs	140 mtrs	432 mtrs		
Micro-arch.	Bonnell	Bonnell	Saltwell	Saltwell	Silvermont
32/64-bit	32-bit	32-bit	32-bit	32-bit	64-bit
1C/2C	1C	1C	2C	2C	2C/4C
HT	HT	HT	HT	HT	no HT
fc [GHz]	0.8-2.13	1.20/1.25	1.50 (1.80 Turbo)	Up to 1.2-2.0 (Turbo)	Up to 1.83-2.41 (Turbo)
L2	512 kB	512 kB	2x512 kB	2x512 kB	2x1 MB
No. of mem.ch.	Single channel MC on SCH	Single channel MC on proc. die (32-bit)	Dual channels MC on proc. die (32-bit)	Dual mem. ch. MC on proc. die (32-bit)	Single/dual mem. channels MC on proc. die (64-bit)
Memory	DDR2-533/400	DDR2-800	LPDDR2-800 (POP)	LPDDR2-1066 (POP)	LPDDR3-1066
GPU	GMA 500 (SGX 535) in PCH (US15W)	GMA 600 (SGX 535) on the proc.	Power VR SGX 545 on the proc	Power VR SGX 544 MP2 on the proc.	Gen 7 DX11 on the proc.
DX	DX 9.0c	DX 9.0c	DX 9.0c	DX 9.x	DX 11
Camera res.	—	—	8 Mpixel	16 Mpixel	
ISP	—	—	ISP 2300	ISP	ISP
Display output	LVDS, SDVO on U515W	LVDS or MIPI-DSI on proc. HDMI 1.3a on SM35	HDMI 1.3a, MIPI-CSI,-2 MIPI-DSI, MIPI-HSI	HDMI 1.3a, MIPI-CSI,-2 MIPI-DSI, MIPI.HSI	HDMI 1.4a, DP 1.2, eDP1.3, MIPI_CSI, MIPI-DSI
GPU clock	400/533 Mb/s	400 MHz	533 MHz	300-533 MHz	
Proc. TDP	0.65-2.5 W	3.0 W	1.7W	2.0-3.0 W	2.0-2.4 W (SDP)
FSB	400/533 MT/s	400 MT/s per dir. cDMI (8-bit)	—	—	—
Socket	PBGA441	BGA 518	FC-MB4760	BGA 760	UTFCBGA1380
Chipset	U515W (Poulsbo)	SM 35 (Whitney Point)	no, SOC	no, SOC	no, SOC
OS	Windows XP/Vista/7 Moblin 1	Windows 7 Home Premium MeeGo, Android	Windows 8 Pro Windows 8	Android 4.2	Windows 8.1 CS (32-bit) Android 4.2.2
Examples	Beng S6 Compal KAX15 Lenovo ideapad U8	Fujitsu Q550 Intel Studybook prototype Motion Computing's CL900 tablet	Acer Iconia W3/W510 Asus VivoTab Dell Latitude 10 HP Envy x2/ElitePad 900 Lenovo Thinkpad Tablet 2 Samsung Series 5 Slate	Asus MeMO Pad FHD 10 / Fonepad Note / Transformer Book Trio Samsung Galaxy Tab3	Acer W3-810 Asus Transformer Book Trio T100 Dell Venue/ Midland Lenovo Miix 8/ Miix 2 Toshiba Encore

4.6 The Bay Trail-T platform (11)

Main features of the models of the Bay Trail-T based Z37xx line [119]

Processor	Cores	L2	Max. freq.	RAM	B/W	Max. RAM	Max. Res.	Process
Atom Z3770	4	2 MB	2,4 GHz	LPDDR3-1066 (dual channel)	17,1 GB/s	4 GB	2560x1600	22 nm
Atom Z3770D	4	2 MB	2,4 GHz	DDR3L-RS-1333 (single channel)	10,6 GB/s	2 GB	1920x1200	22 nm
Atom Z3740	4	2 MB	1,8 GHz	LPDDR3-1066 (dual channel)	17,1 GB/s	4 GB	2560x1600	22 nm
Atom Z3740D	4	2 MB	1,8 GHz	DDR3L-RS-1333 (single channel)	10,6 GB/s	2 GB	1920x1200	22 nm
Atom Z3680	2	1 MB	2,0 GHz	LPDDR3-1066 (single channel)	8,5 GB/s	1 GB	1280x800	22 nm
Atom Z3680D	2	1 MB	2,0 GHz	DDR3L-RS-1333 (single channel)	10,6 GB/s	2 GB	1920x1200	22 nm

4.6 The Bay Trail-T platform (12)

Max. turbo and base clock frequencies of the models of the Bay Trail-T based Z37xx line [120]

Bay Trail Turbo Speeds						
	Z3770	Z3770D	Z3740	Z3740D	Z3680	Z3680D
Max turbo frequency	2.39GHz	2.41GHz	1.86GHz	1.83GHz	2.0GHz	2.0GHz
Max non-turbo Frequency	1.46GHz	1.5GHz	1.33GHz	1.33GHz	1.33GHz	1.33GHz

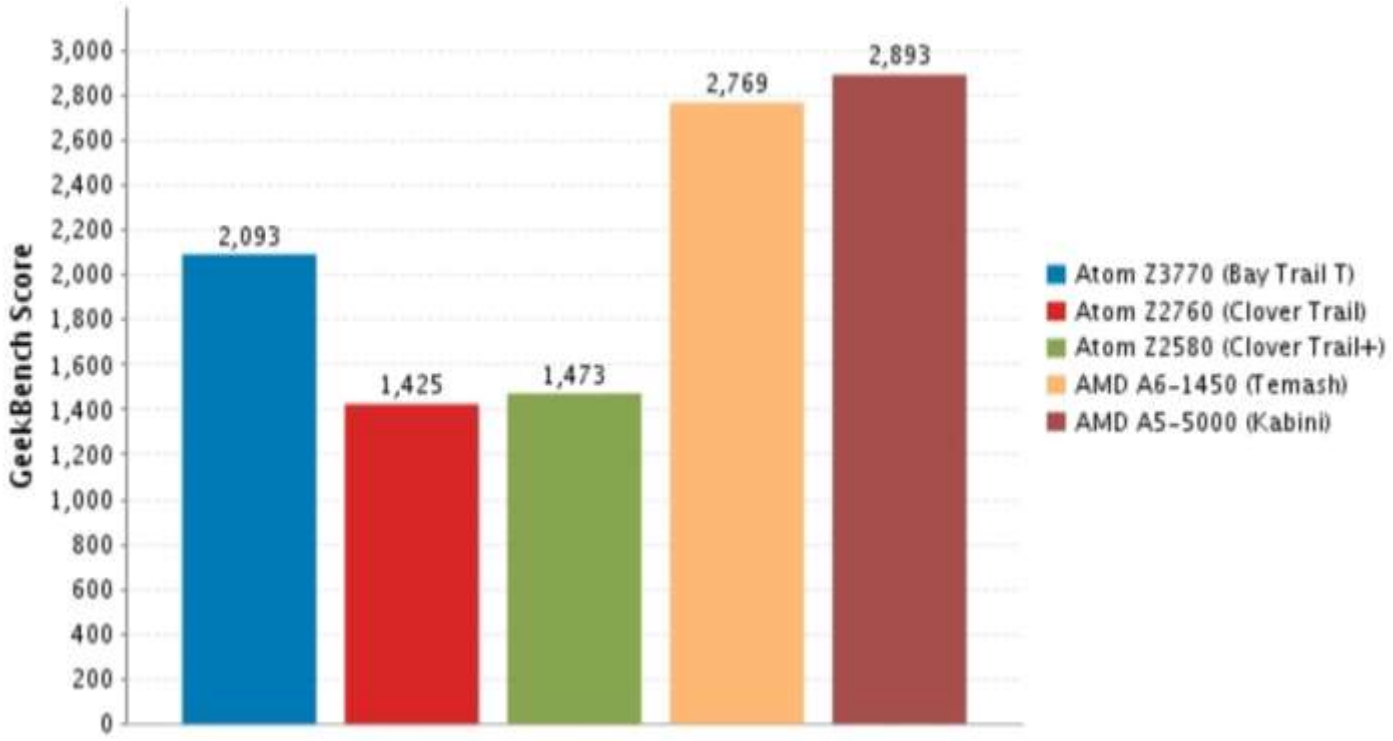
4.6 The Bay Trail-T platform (13)

Remark

Intel considers their 2. generation Turbo technology as a viable alternative to ARM's big/little architecture concept when only a "little" core operates if there is no need for higher performance [120].

4.6 The Bay Trail-T platform (14)

Performance comparison of the Z3770 with Intel's previous tablet platforms and AMD's low power platforms-1 [105]



4.6 The Bay Trail-T platform (15)

Performance comparison of the Z3770 with Intel's previous tablet platforms and AMD's low power platforms-2 [105]

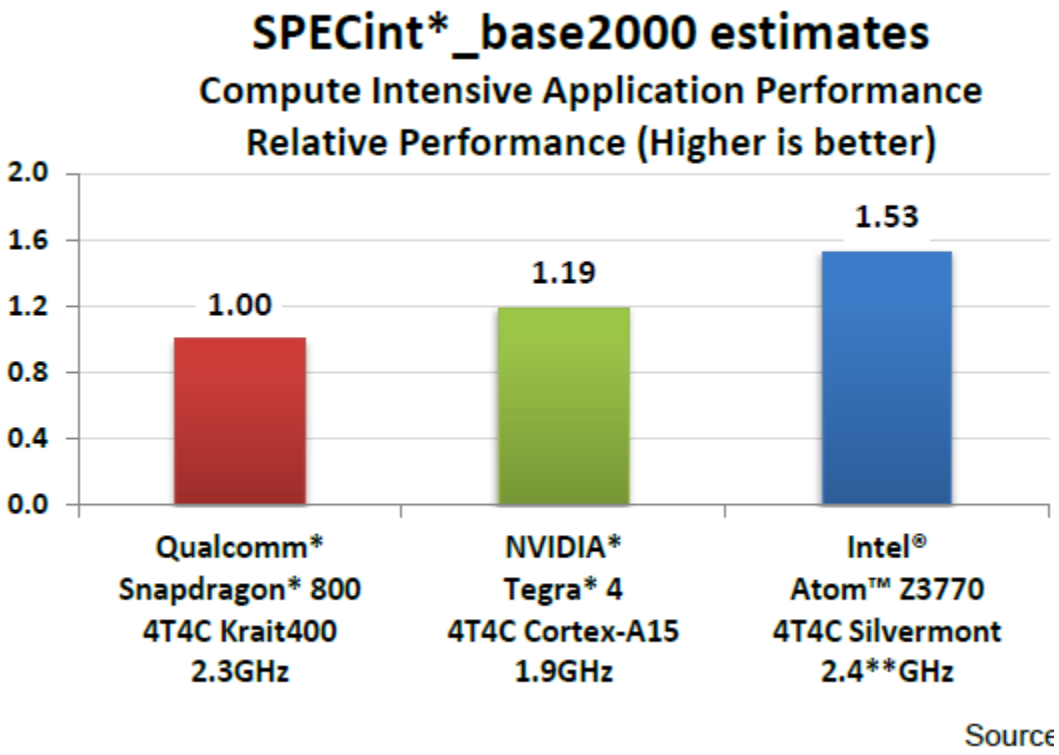
As the Figure indicates, at least for the benchmark used the Z3770 processor

- provides about 50 % more performance than Intel's previous Clover Trail and Clover Trail+ tablet platforms, but
- AMD's recent low power chips outperform it by about 30 – 40 %.

Nevertheless, both AMD quad-core chips consume more power (the Temash chip has a TDP of 8 W whereas the Kabini chip 15 W vs. the 2 W SDP consumption of the Z3770 (equaling about 3-3.5 W TDP).

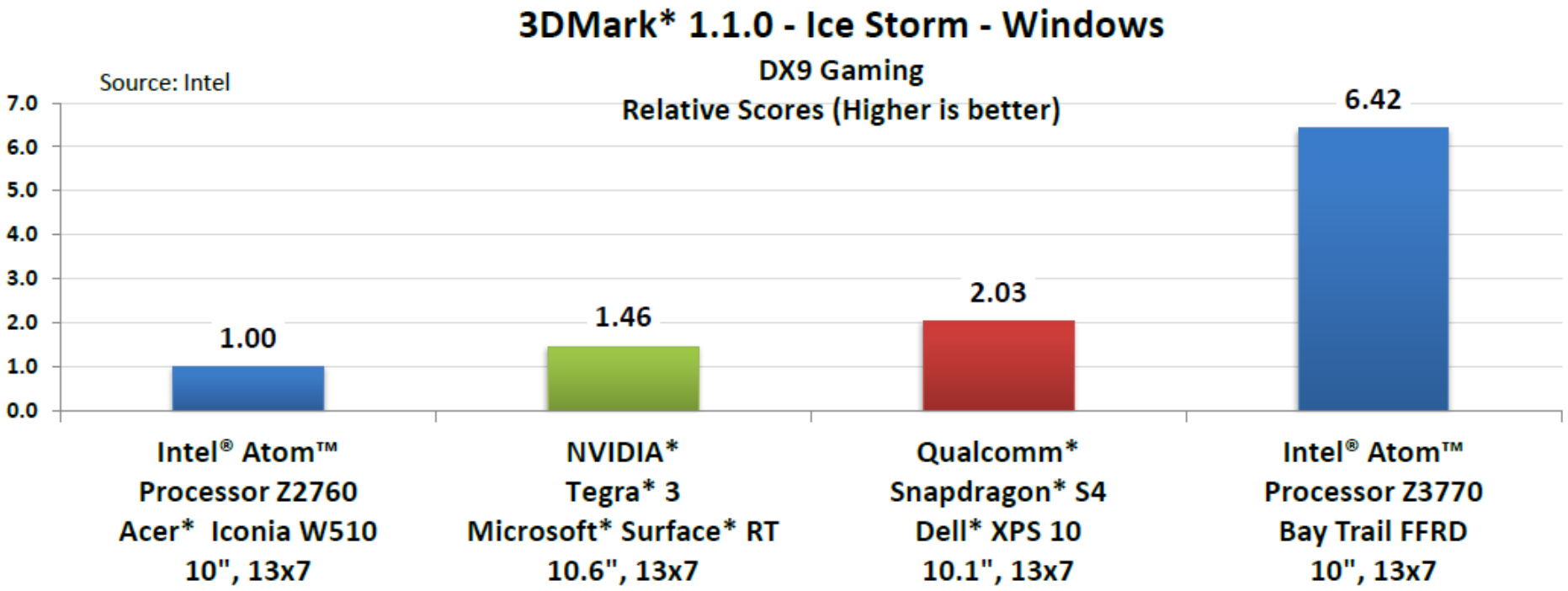
4.6 The Bay Trail-T platform (16)

Performance comparison of the Z3770 with Qualcomm's and Nvidia's recent 4-core tablets while running the SPECint_base 2000 benchmark [118]



4.6 The Bay Trail-T platform (17)

Performance comparison of the Z3770 with Qualcomm's and Nvidia's recent 4-core tablets as well as Intel's previous line while running the 3DMark 1.1.0 benchmark [118]

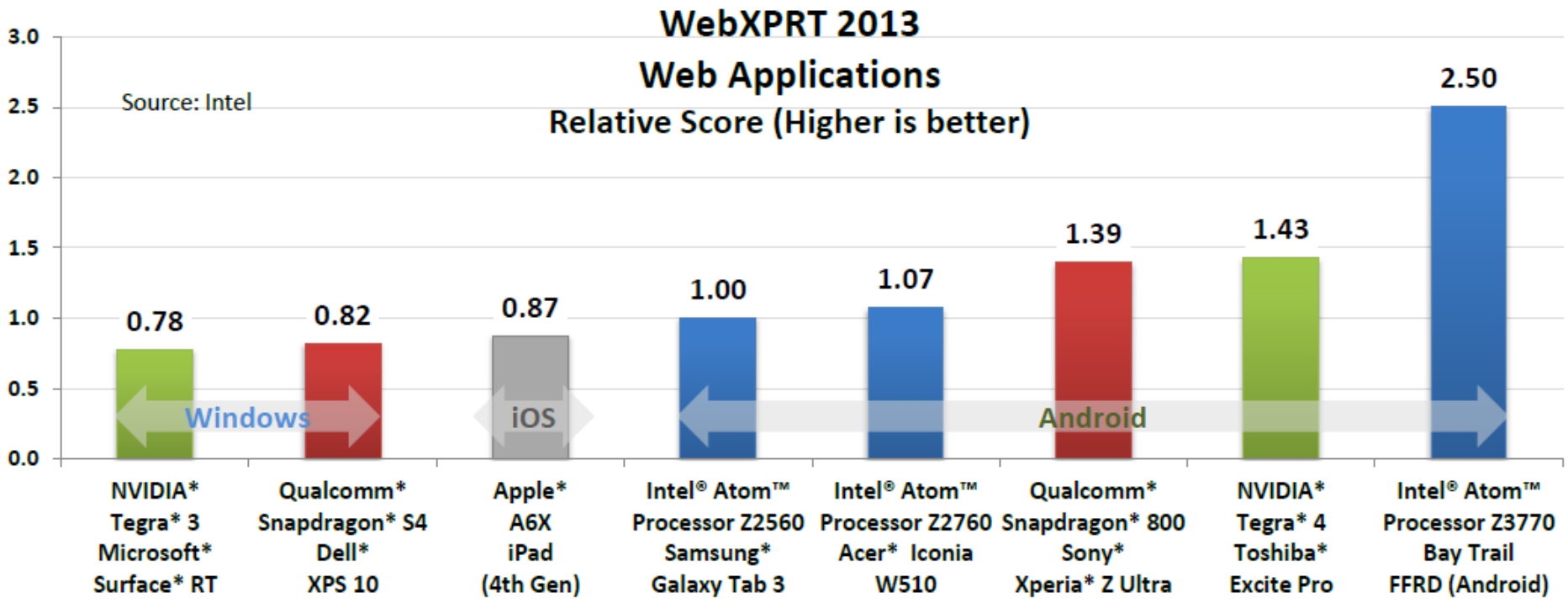


Intel® Atom™ Z3770 (Bay Trail) offers up to 6.4X 3D gaming performance over Intel® Atom™ Z2760 (Clover Trail)

4.6 The Bay Trail-T platform (18)

Cross OS performance results while running the WebXPRT 2013 benchmark [118]

It measures the JavaSript and HTML5 performance of a device on real-world usage



Intel® Atom™ Z3770 (Bay Trail) offers up to 2.5X higher performance over Intel® Atom™ Z2560 (Clover Trail+) on browser-based usages

4.6 The Bay Trail-T platform (19)

Market reception of Intel's Bay Trail-T tablet platform

There are high expectation for all Silvermont-based devices both for the tablet and the smartphone space, as indicated e.g. in [118]

4.6 The Bay Trail-T platform (20)

Remark

Recently, Intel introduced a few new notions related to power consumption, like cTDP, SDP or ACP. Subsequently, we give a brief overview of these notions.

Interpretation of the power consumption related notions TDP, cTDP, SDP and ACP

TDP (Thermal Design Point)

Historically, Intel specifies the thermal dissipation of their processors as the TDP value.

TDP is the max. power a device consumes when running power intensive applications at given clock speed and ambient temperature [101].

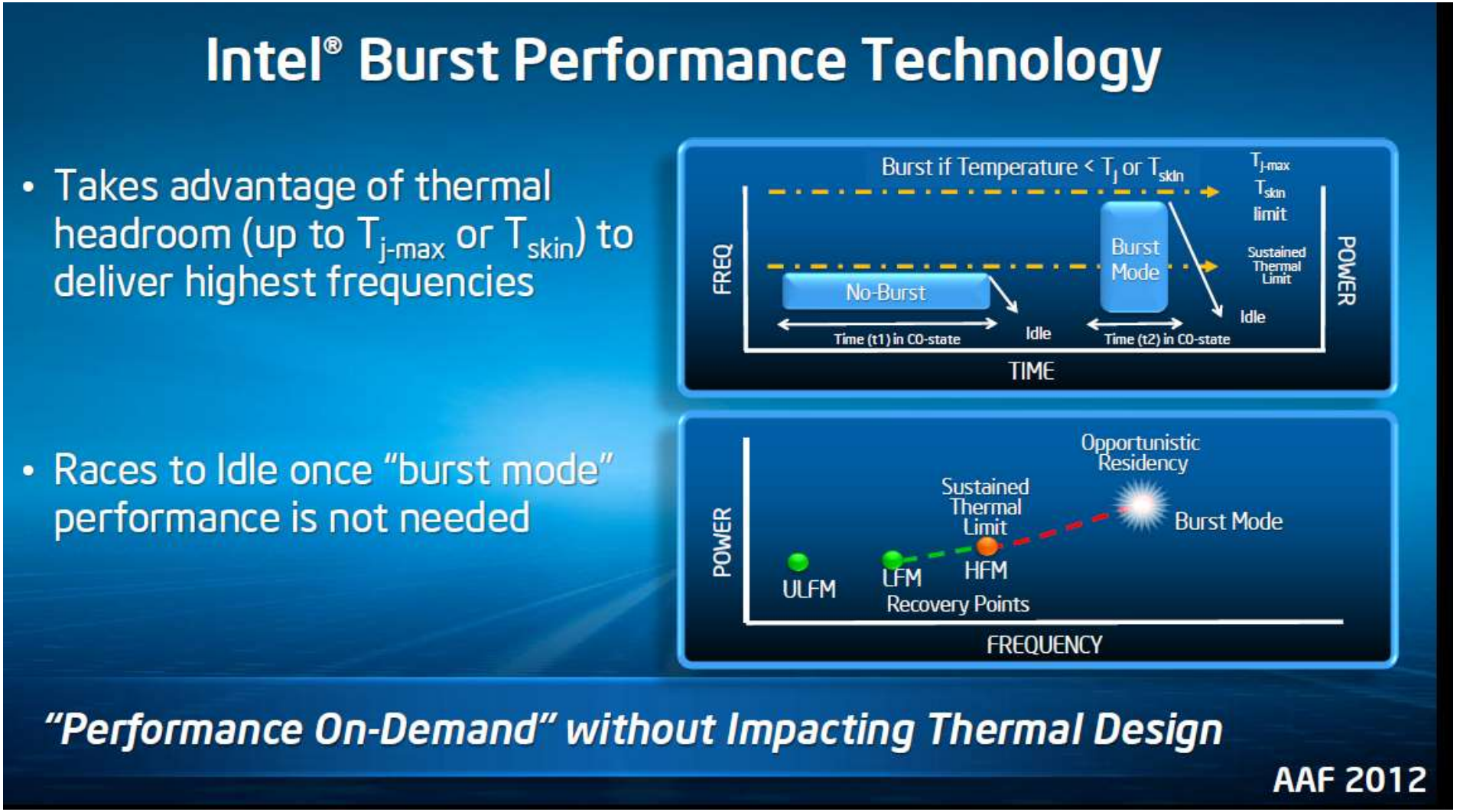
TDP is not the max. dissipation, an application that runs e.g. "power viruses, like the Furemark power benchmark, can consume 20 – 30 % more power than specified by the TDP.

The TDP is determined such that running power intensive applications Tj (junction temperature) and Tskin (skin temperature), i.e. case temperature remain below specified values if the cooling system is designed to cope with a sustained TDP value.

So TDP is the basic input parameter for designing the cooling system.

Note that in Turbo mode (designated also as Burst mode) when there is a power headroom (e.g. due to a light workload or a previous sleep state when the device was cooled down) TDP can be exceeded for a short time to boost performance, as indicated in the next slide.

The concept of Turbo mode (Burst mode) [98]



4.6 The Bay Trail-T platform (23)

cTDP (configurable TDP) [102]

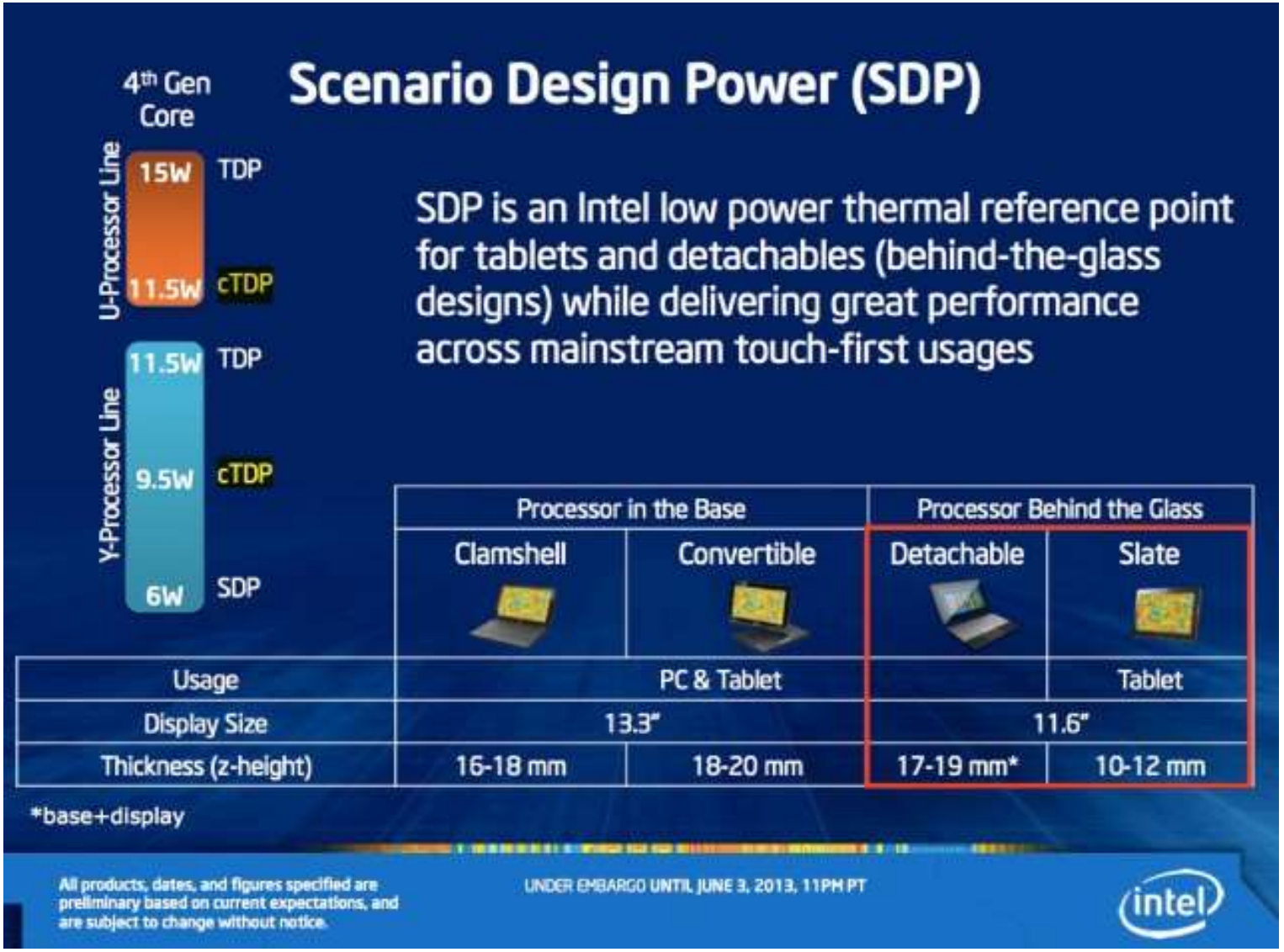
- New forms of implementation of notebooks and tablets, such as convertibles with a docking station, let Intel rethink their power strategy.
- With the traditional TDP interpretation, when a fanless tablet is docked on the base station, the docked tablet will run at the same maximal clock speed as before despite the fact that the docking station could provide an effective cooling system.
- To amend this problem at Computex 2011 (9/2011) Intel introduced the concept of the configurable TDP such that a processor can have two or even three power ratings.
- As an example, when a tablet processor has a TDP of 15 W and runs at 1.5 GHz base frequency in tablet mode, after docking and assuming an appropriate cooling it can behave like a processor with e.g. 22.5 W TDP and running at 2.0 GHz.
- In other words, with configurable TDP a processor can run in two (or even in three) different user scenarios with different cooling conditions and associated clock frequencies.

4.6 The Bay Trail-T platform (24)

SPD (Scenario Design Point) [121]

- In the beginning of 2013, Intel introduced a new concept for specifying power consumption called Scenario Design Point (SDP).
- SPD is a usage-based design specification, and provides an additional reference point for designing power constrained platforms.
- SDP is a specified under a specific workload, junction temperature (Tj = 80 C^0, and frequency, and reflects the average dissipation when running the specified workload.
- SPD is typically 50-70 % of the TDP figure.
- As an example, Haswell-based mobile Y-line processors have an SDP value of 6W but a TDP of 11.5W, as indicated in the subsequent slide [104].
- While SPD is specified at Tj = 80 C^0, the functional limit for the processor remains Tjmax (E.g. 100 C^0 for the mobile Haswell lines).
- Obviously, it is also possible to lay out a platform for TDP power consumption in order to run the processor at a higher clock frequency and thus to provide more performance, but in this case both the cooling capability of the platform and the thermal control mechanism used needs to be fitted.
- The notion of SPD introduced for mobile devices by Intel is considered by some market analysts as a marketing trick to indicate a low dissipation figure compared to competing products [122].

Example figures for TDP, cTDP and SDP for mobile Haswell processors [104]



4.6 The Bay Trail-T platform (26)

ACP (Average CPU Power)

- ACP is a similar notion as AMD's SDP, that was introduced along with their K10 Barcelona family of server processors in 2007 in the first line for data center applications.
- ACP characterizes the averages power consumption while the processor runs a given set of benchmark applications.
- The reasoning for introducing ACP was the consideration that in "scenarios" when a large number of CPU's is used, the sum of the average power consumption of the CPUs (i.e. the sum of their ACP values) is a more reasonable design parameter for designing the power supply and the cooling system than the sum of the max. power consumption of the CPUs (i.e. the sum of their TDP values).

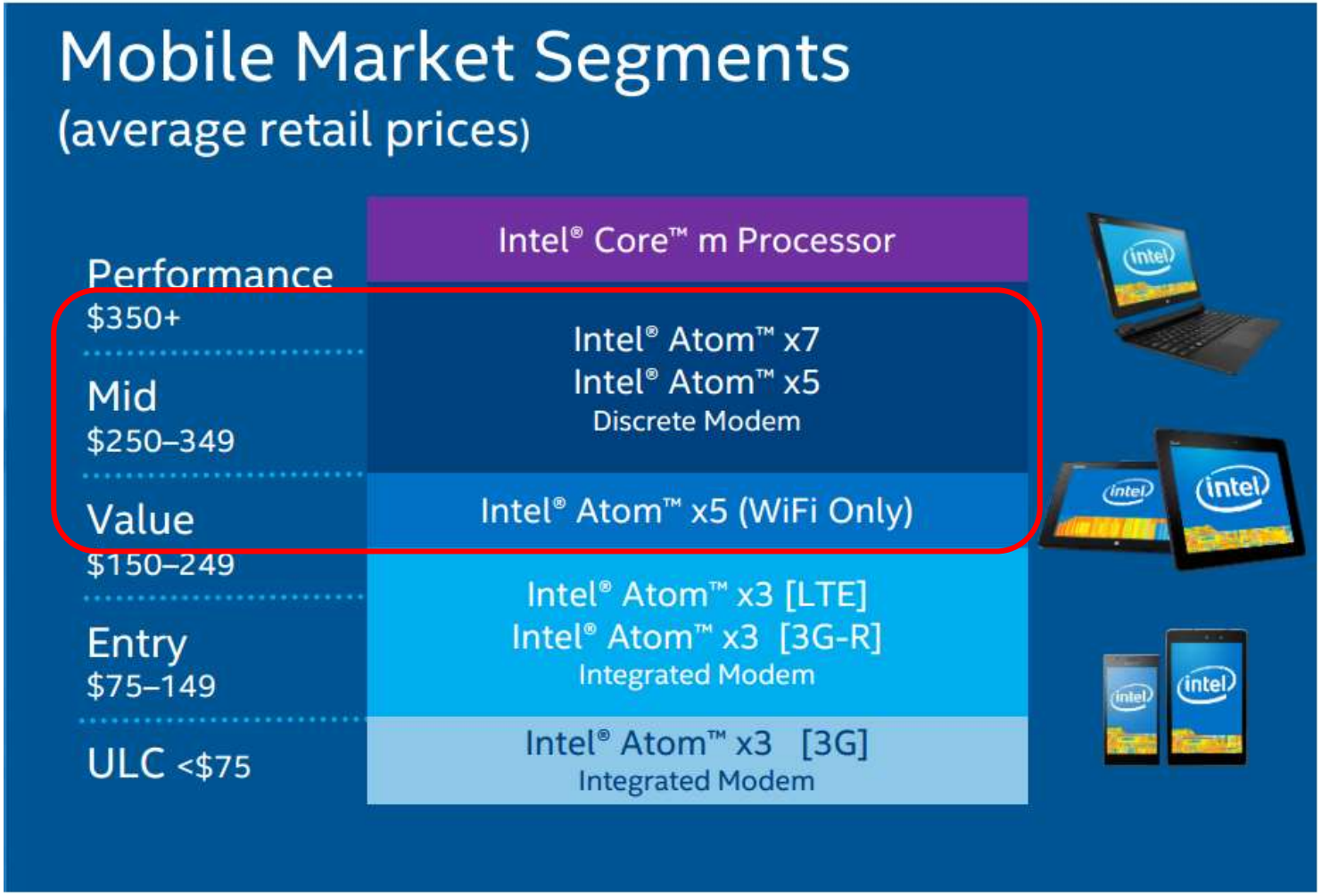
4.7 The Cherry Trail platform

4.7 The Cherry Trail platform

- It was announced at Intel's Annual Investor Day in 11/2013 and launched with some delay in 03/2015.
- It is based on the 14 nm Airmont CPU.
- The related application processor is termed Valleyview-T and the models dubbed as x5-Z83xx/Z85xx and x7-Z87xx, as indicated in the next Figure.
- The Cherry Trail platform does not yet include an integrated baseband modem but needs an external companion chip (XMM 7260).

4.7 The Cherry Trail platform (2)

Positioning Intel's Cherry Trail processors in the mobile market segment [169]



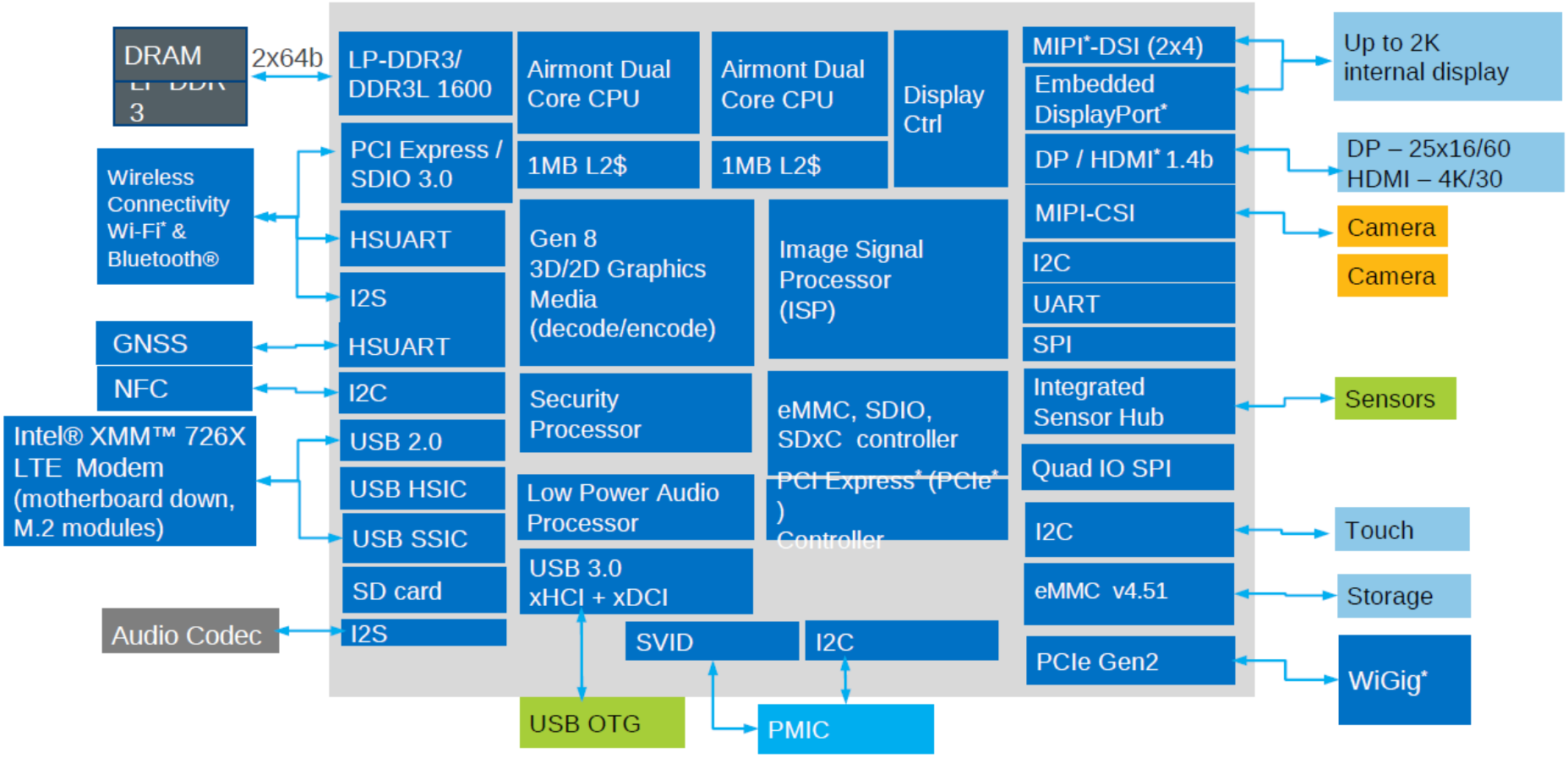
4.7 The Cherry Trail platform (3)

Main features of the Cherry Trail tablet platform

	Cherry Trail
Available	Q3/2015
Focus	Tablets
Processor	Valleyview -T
Models	X5-Z83xx/Z85xx, x7-Z87xx
Technology	14 nm
Die size	
No. of trans.	
Micro-arch.	Airmont
32/64-bit	64-bit
Core count	4C
HT	no HT
fc [GHz]	Up to 1.6 GHz
L2	1 MB/2 cores
No. of mem.ch.	Up to dual channels on proc. die (64-bit)
Memory	LPDDR3-1600
GPU	Gen 8-LP on the proc.
DX	DX 11.1
Camera res.	
ISP	ISP
Display output	HDMI 1.4b, DP 1.1a, eDP1.3, MIPI-DSI 1.01
GPU clock	200 MHz
Proc. TDP	2.0-2.4 W (SDP)
FSB	—
Socket	UTFCBGA1380
Chipset	no, SOC
OS	Windows 7/8/8.1/10 Android 5.1
Examples	HP ElitePad Microsoft Surface 3

4.7 The Cherry Trail platform (4)

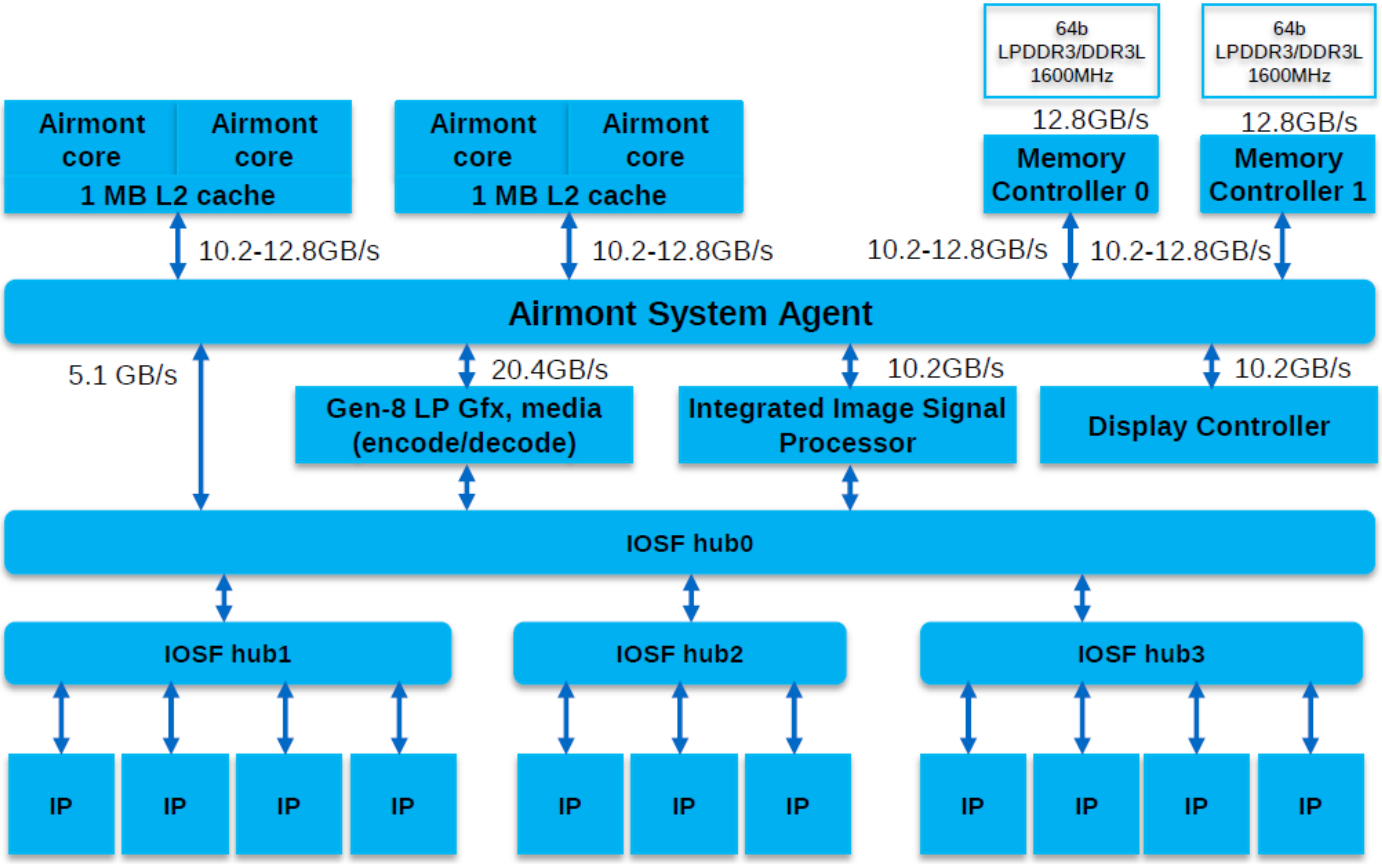
Block diagram of the Cherry Trail platform [170]



4.7 The Cherry Trail platform (5)

System architecture of Cherry Trail processors [170]

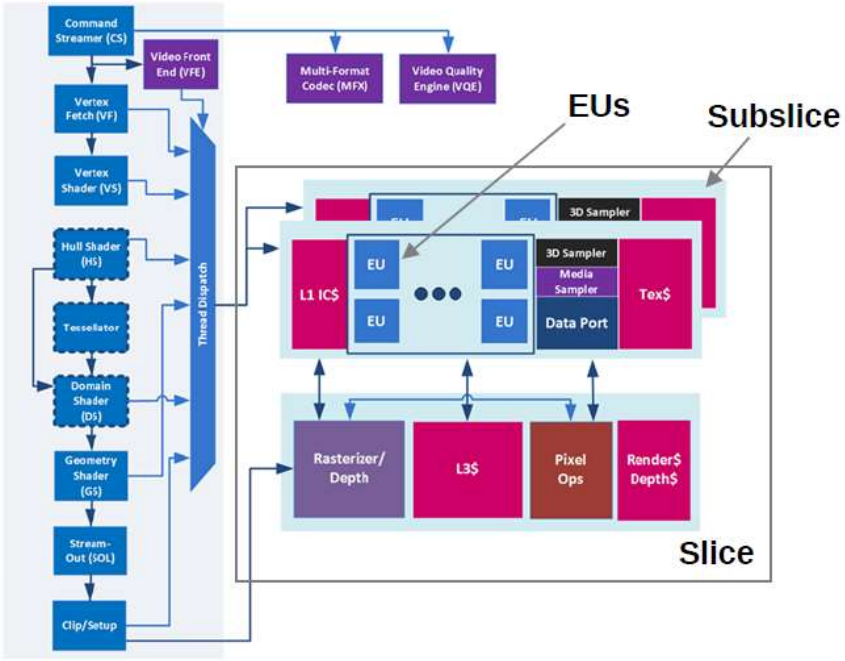
- Single/Dual x32/x64 ch LPDDR3/DDR3L 1600MHz
- Asynchronous link between System Agent to Memory Controller
- Multiple flexible System Agent arbitration to ensure isochronous traffic and allow maximizing DDR self-refresh time for power management
- Two dual-core AMT module with 1MBL2 each
- GEN8LP direct System Agent connection, max possible memory bandwidth
- Direct imaging and display controller connection to System Agent



4.7 The Cherry Trail platform (6)

The Gen8LP graphics [170]

- Leading features
  - **Support DirectX11, OpenGL ES3.0, OpenCL1.2, OpenGL4.3, RS Compute**
  - Supports higher precision computes and OpenCL 1.2, natively supports latest texture compression formats like ETC and ASTC-LDR
- Performance & Power
  - **>2x performance per watt improvement**
  - **4x compute and pixel throughput, 2x texture throughput**
  - Power wells for 3D and Media, sub-slice and EU power gating
  - Native 16 bit computes with 2x performance at ISO power
  - Power optimized for UI high ppi workloads

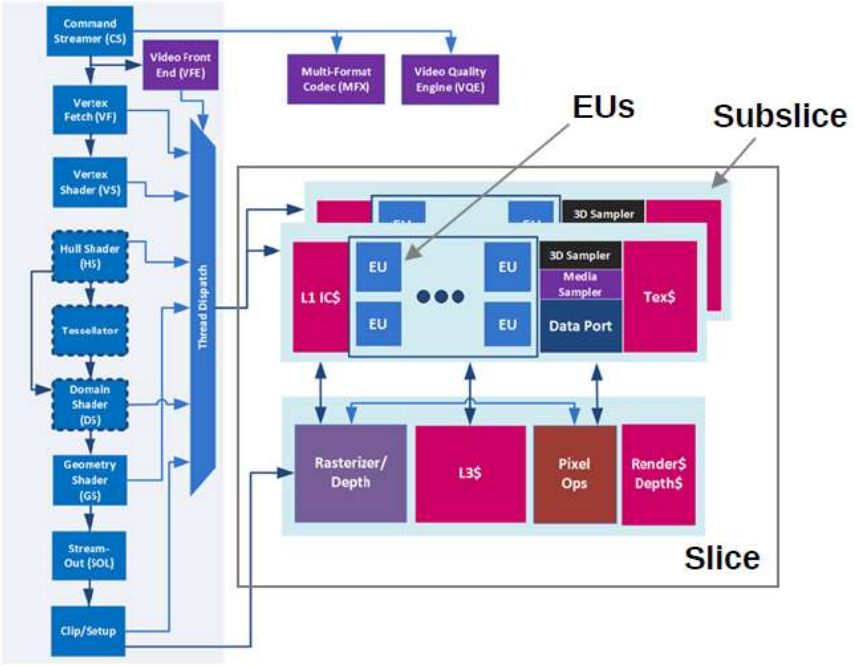


Delivered on Intel leading14nm low-leakage process

4.7 The Cherry Trail platform (7)

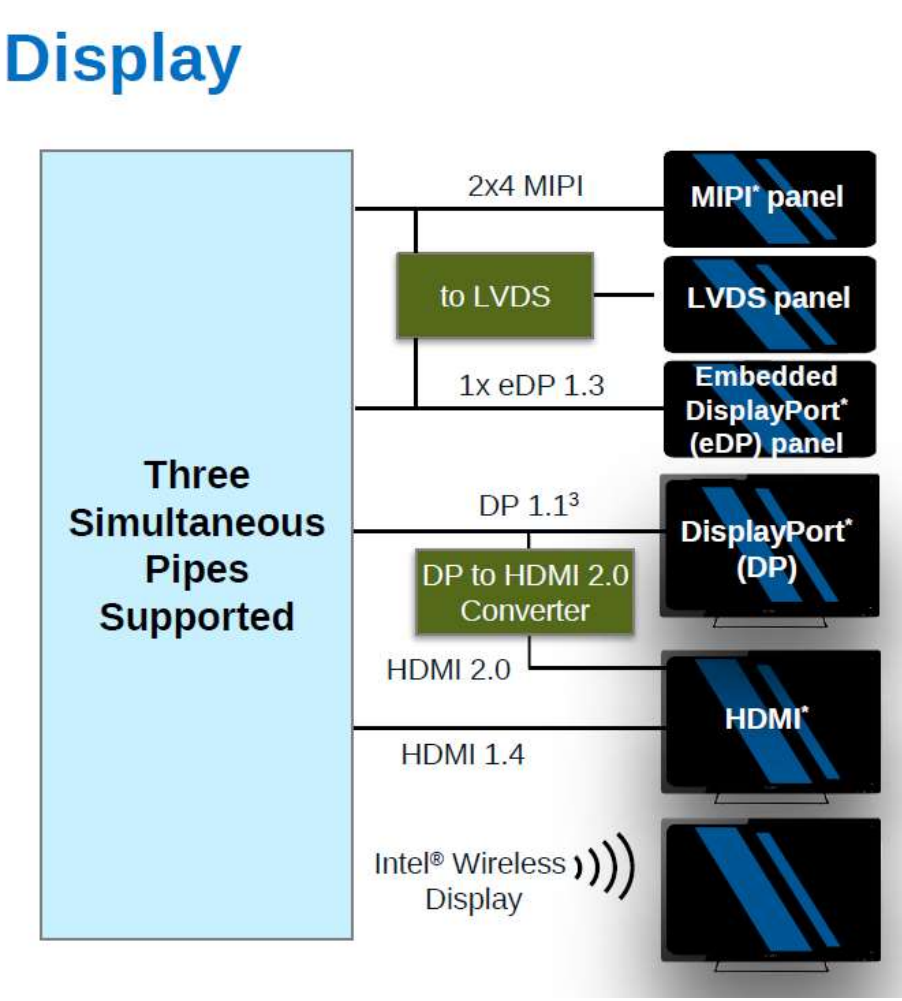
Architecture of the Gen8LP graphics [170]

- EU (Execution Unit)
  - 7 HW threads per EU, 128 “GRF” registers per thread, 32 bytes per “GRF” register
  - Arch register, SMT Instruction Dispatcher
  - 2 floating point units, Branch and messaging unit
- Sub-slice
  - 8 EUs, thread dispatcher, instruction cache, texture/image sampler unit
  - 64 bytes/cycle read bandwidth
- Slice
  - 2 Sub-slices x 8 = 16 EUs.
  - 2x8x7=112 hardware threads
  - L3 data cache, 384KB/slice, 64 byte cachelines,
  - Shared local memory 64KB/Subslice



4.7 The Cherry Trail platform (8)

Display properties of Cherry Trail processors [170]



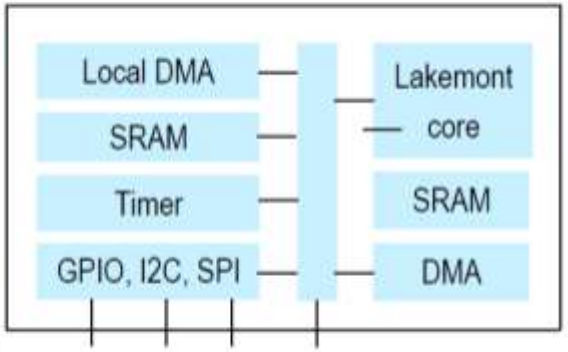
Intel® Atom™ x5-8300	Intel Atom x5-8500	Intel Atom x7-8700
2 Displays	3 Displays[3]	3 Displays[3]
1900x1200@60Hz (1x4)	2560x1600@60Hz	2560x1600@60Hz
1900x1200@60Hz	1900x1200@60Hz	1900x1200@60Hz
1900x1200@60Hz	2560x1600@60Hz	2560x1600@60Hz 3840x2160@60Hz[1]
2560x1600@60Hz	2560x1600@60Hz	2560x1600@60Hz
1920x1080@60Hz 3820x2160@30Hz	1920x1080@60Hz 3840x2160@30Hz	1920x1080@60Hz 3840x2160@30Hz 3840x2160@60Hz[2, 1]
1080p@60Hz 2560x1440@30Hz 2560x1600@30Hz	**1080p@60Hz** 2560x1440@30Hz 2560x1600@30Hz	**1080p@60Hz** 2560x1440@30Hz 2560x1600@30Hz

4.7 The Cherry Trail platform (9)

The integrated sensor hub [170]

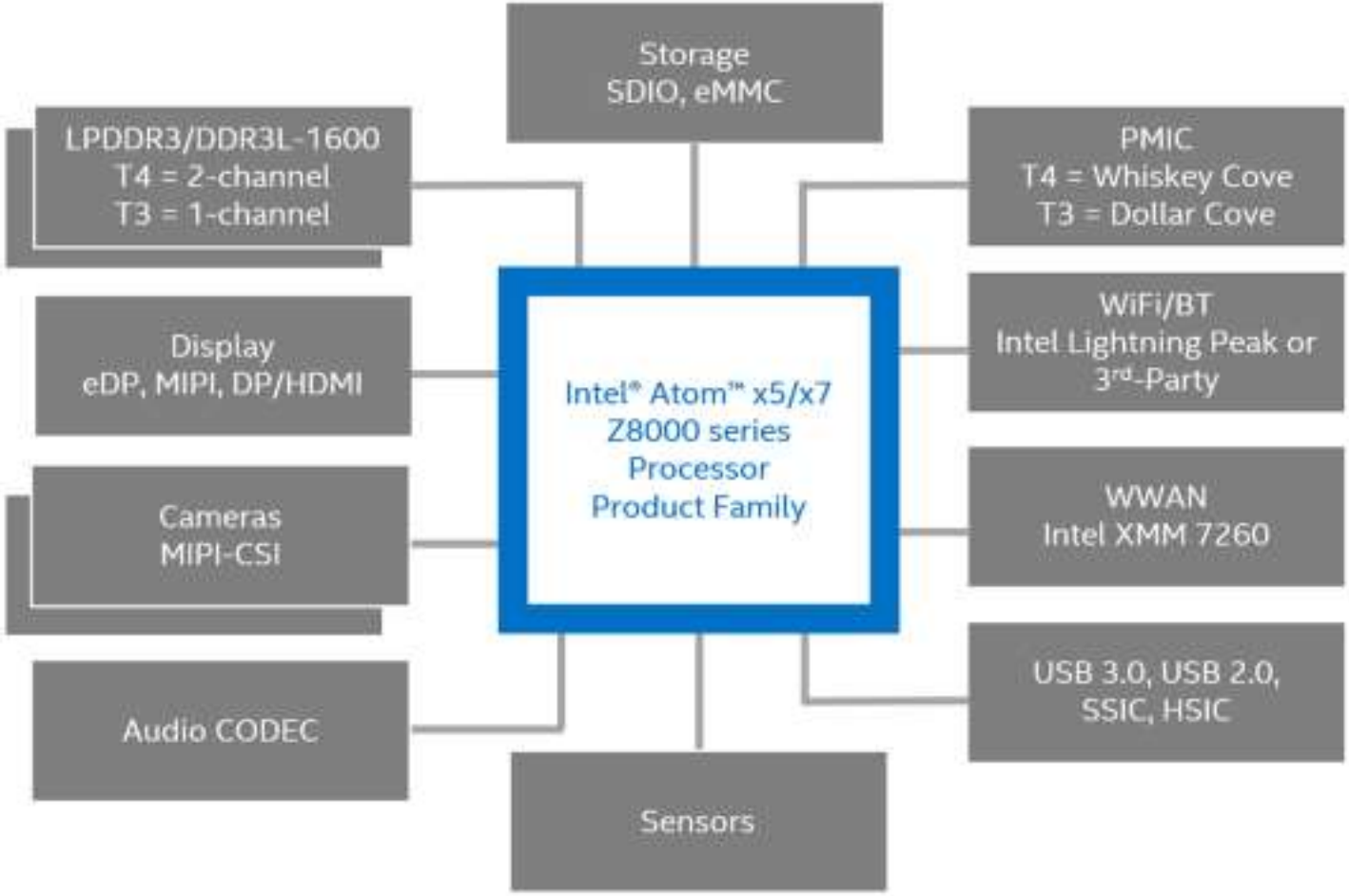
"Always On, Always Sensing" and it provides the following functions to support this goal:

- Acquisition / sampling of sensor data
- The ability to combine data from individual sensors to create a more complex Virtual sensor that can be directly used by the firmware/OS.
- Low power operation through clock gating and power gating of parts of the ISH together with the ability to turn sensors off.
- The ability to operate independently when the host platform is shut off



4.7 The Cherry Trail platform (10)

The Cherry Trail platform [171]



4.7 The Cherry Trail platform (11)

Launched Cherry Trail models

SKU	Status	Launch Date	# of Cores	Processor Base Frequency
x7-Z8750	Launched	Q1'16	4	1.60 GHz
x7-Z8700	Launched	Q1'15	4	1.60 GHz
x5-Z8550	Launched	Q1'16	4	1.44 GHz
x5-Z8500	Launched	Q1'15	4	1.44 GHz
x5-Z8350	Launched	Q1'16	4	1.44 GHz
x5-Z8330	Launched	Q1'16	4	1.44 GHz
x5-Z8300	Launched	Q2'15	4	1.44 GHz

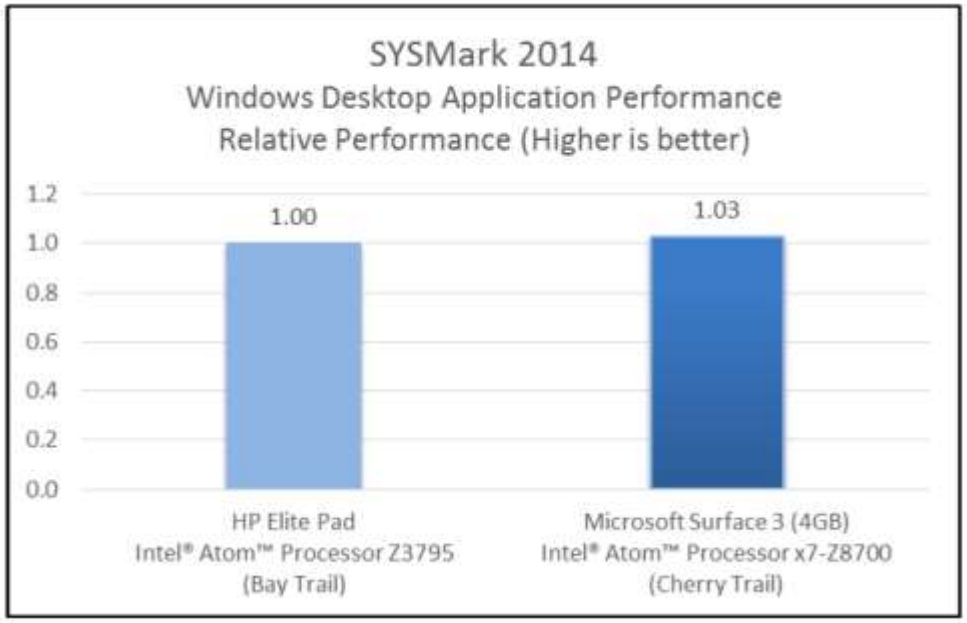
4.7 The Cherry Trail platform (12)

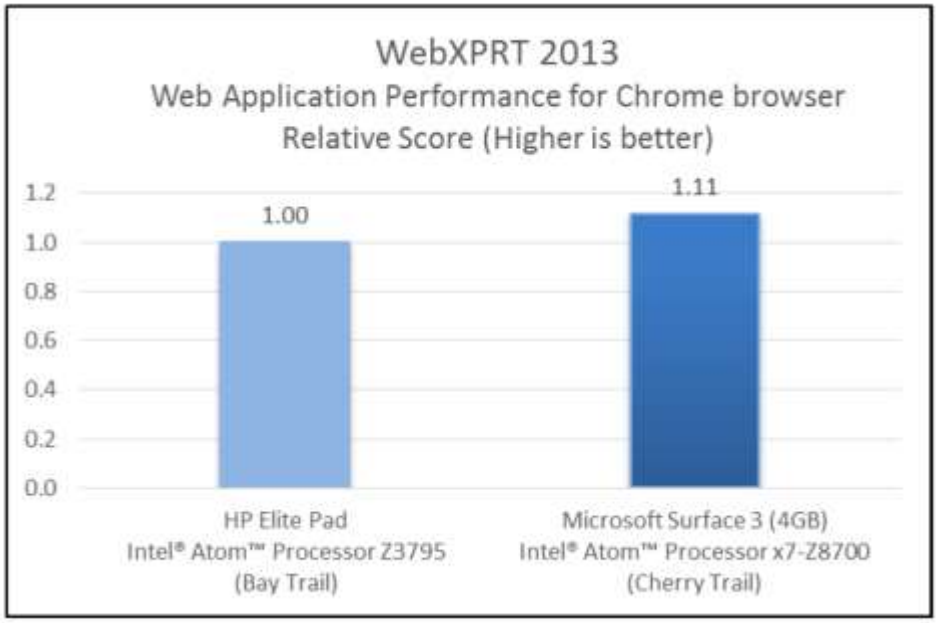
Main features of the first launched Cherry Trail models [170]

Specifications	Intel® Atom™ x5-8300	Intel Atom x5-8500	Intel Atom x7-8700
Scenario Design Power	2 watts	2 watts	2 watts
Form Factor	7" to 11.6" tablet, and small screen 2 in 1s	7" to 11.6" tablet, and small screen 2 in 1s	7" to 11.6" tablet, and small screen 2 in 1s
CPU	Quad core 64-bit Atom x5 Up to 1.84 GHz[1]	Quad core 64-bit Atom x5 Up to 2.24 GHz	Quad core 64-bit Atom x7 Up to 2.4 GHz
Process	14nm	14nm	14nm
Graphics (GPU)	Gen8 12EU, up to 500MHz DirectX* 11.1, OpenGL* ES 3.1, OpenCL* 1.2, OpenGL 4.3, RS Compute	Gen8 12EU, up to 600 MHz DirectX 11.1, OpenGL ES 3.1, OpenCL 1.2, OpenGL 4.3, RS Compute	Gen8 16EU, up to 600 MHz DirectX 11.1, OpenGL ES 3.1, OpenCL 1.2, OpenGL 4.3, RS Compute
Media (Encode/Decode)	HEVC (decode), H.264, VP8	HEVC (decode), H.264, VP8	HEVC (decode), H.264, VP8
Memory	1x32, 1x64 DDR3L-RS[2] 1600, 1-2GB	2x64 LPDDR3 1600, 2-8GB	2x64 LPDDR3 1600, 2-8GB
Display Resolution	INTERNAL: 1920x1200 (MIPI*-DSI or LVDS) EXTERNAL: 1920x1080 (HDMI*)	INTERNAL: up to 25x16 (MIPI-DSI or Embedded DisplayPort* (eDP)) EXTERNAL: up to 4k2k (HDMI)	INTERNAL: up to 25x16 (MIPI-DSI or eDP) EXTERNAL: up to 4k2k (HDMI)
Modem (Discrete)	Intel® XMM™ 7260/62 LTE Cat-6 (up to 300Mbps DL) M.2 only for x5 8300	Intel XMM 7260/62 LTE Cat-6 (up to 300Mbps DL, 50Mbps UL for modem-down)	Intel XMM 7260/62 LTE Cat-6 (up to 300Mbps DL, 50Mbps UL for modem-down)
Connectivity	Intel® WLAN, Intel® WWAN (M.2 modules), Intel® NFC	Intel WLAN, Intel WWAN (Intel XMM 726x), Intel NFC	Intel WLAN, Intel WWAN (Intel XMM 726x), Intel® WiGig*, Intel NFC
Input Output	6xI2C[4], 2xHSUART, 1xSDIO, 3xI2S, SPI[5], PCI Express* (PCIe*) 2.0 x1, 1xI2C(ISH), 1xI2C (NFC)	7xI2C[4], 2xHSUART, 1xSDIO, 3xI2S, 1xLPC, 1xSPI[5], PCIe 2.0 x2, 1x I²C[4] (ISH), 1xI2C (NFC)	7xI2C[4], 2xHSUART, 1xSDIO, 3xI2S, 1xLPC,1x SPI[5] , PCIe 2.0 x2, 1x I²C[4] (ISH), I2C[4](NFC)
USB	1xUSB3 OTG, 2xHSIC, 3xUSB2	1xUSB3 OTG, 3xUSB3[6] 2xSSIC, 2xHSIC	1xUSB3 OTG, 3xUSB3[6] 2xSSIC, 2xHSIC
Storage	eMMC 4.51[7]	eMMC 4.51[7]	eMMC 4.51[7]
ISP / Camera (rear/front)	Up to 8MP Intel® RealSense™ Snapshot	Up to 13MP Intel® RealSense™ 3DCamera	Up to 13MP Intel RealSense 3DCamera

4.7 The Cherry Trail platform (13)

Application performance [170]





5. Atom-based platforms targeting smartphones

- 5.1 Introduction and overview of Intel's Atom-based platforms targeting smartphones
- 5.2 Performance oriented smartphone platforms
- 5.3 Low-cost oriented smartphone platforms

5.1 Introduction and overview of Intel's Atom-based platforms targeting smartphones

5.1 Introduction and overview of Intel's Atom-based platforms targeting smartphones

A t o m b a s e d p r o d u c t s e r i e s

Entry-level desktops	Notebooks (Subnotebooks)	Convertibles	Tablets	Smartphones	Embedded	Microservers
D/J-Series *(First D, then J)*	***N-Series***		***Z-Series*** *Zx6xx/x7xx*	***Z-Series*** *Zx4xx/x5xx*	***E/CE-Series***	***S-Series***
	Section 3		*Section 4*	*Section 5*	*Not discussed*	*Not discussed*

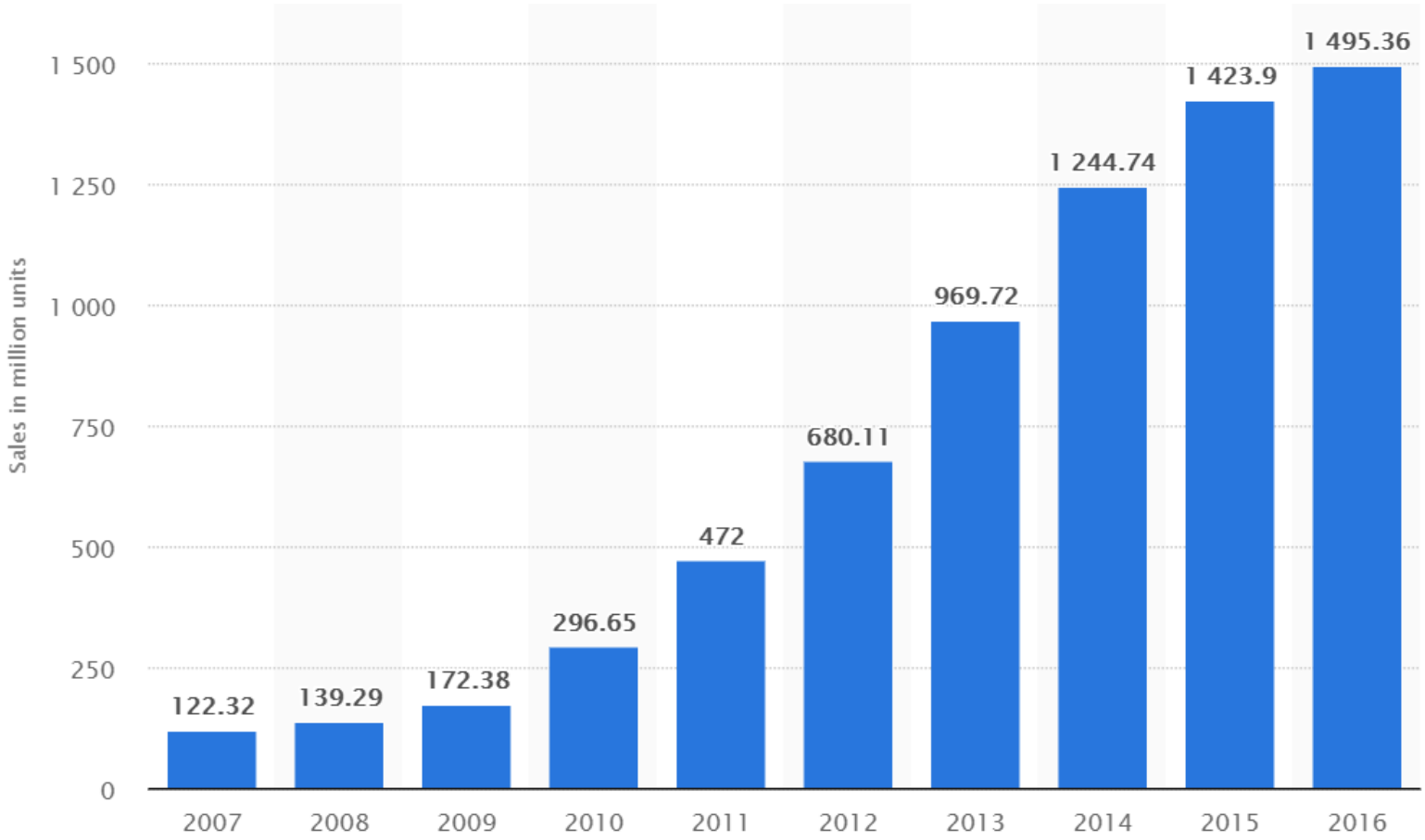
5.1 Introduction to Atom-based platforms targeting smartphones (2)

The birth of smartphones

- Smartphones emerged in 2006 with the Blackberry Pearl 8100 design from the Canadian firm RIM (Research in Motion) [38].
- In 2007 Apple's iPhone gave a strong momentum for rapid spreading of smartphones.
- Google's Android was unveiled also in 2007 with first Android-powered phones sold in 10/2008 [39].

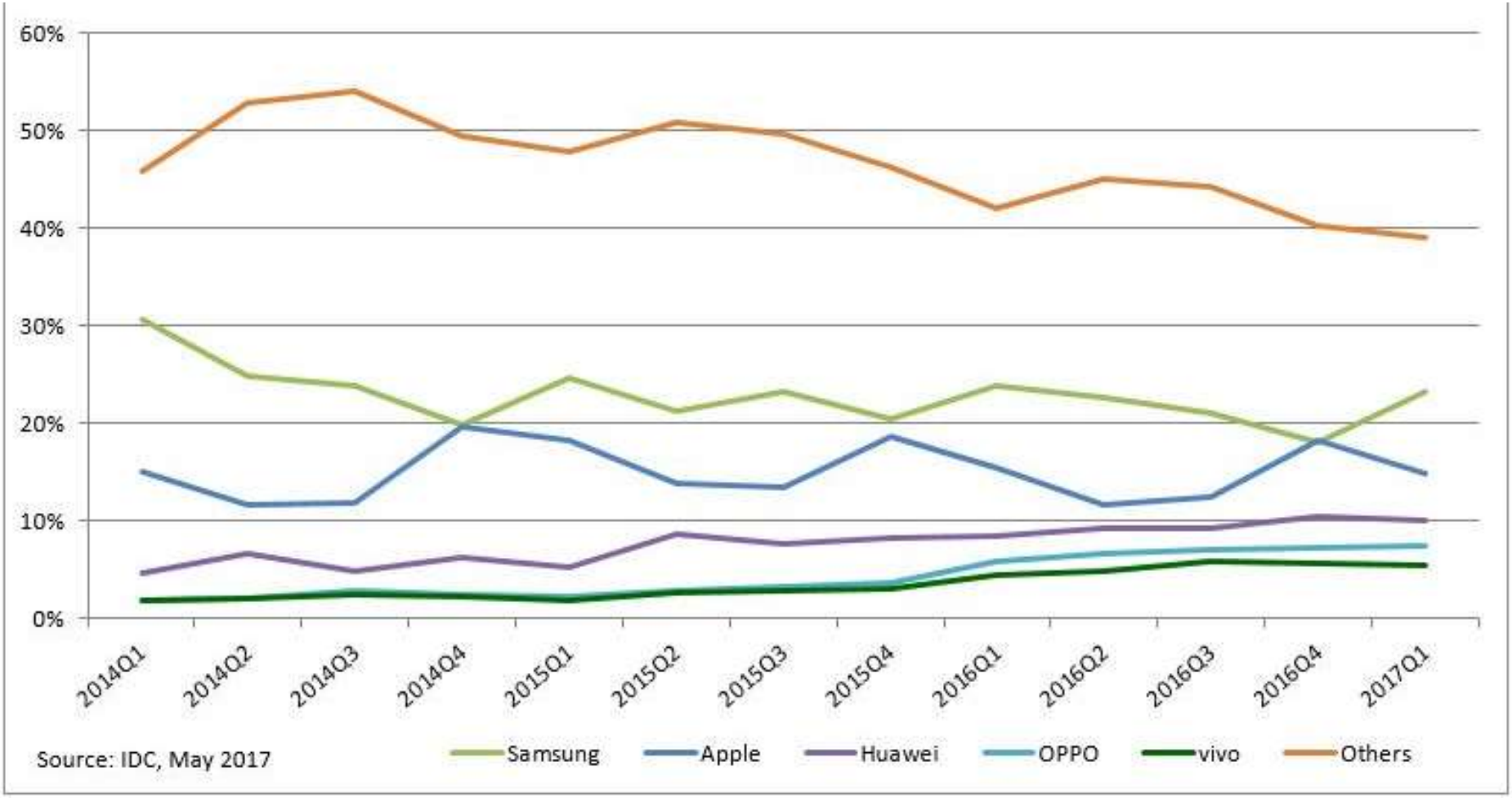
5.1 Introduction to Atom-based platforms targeting smartphones (3)

Worldwide unit shipments of smartphones 2007-2016 [172]



5.1 Introduction to Atom-based platforms targeting smartphones (4)

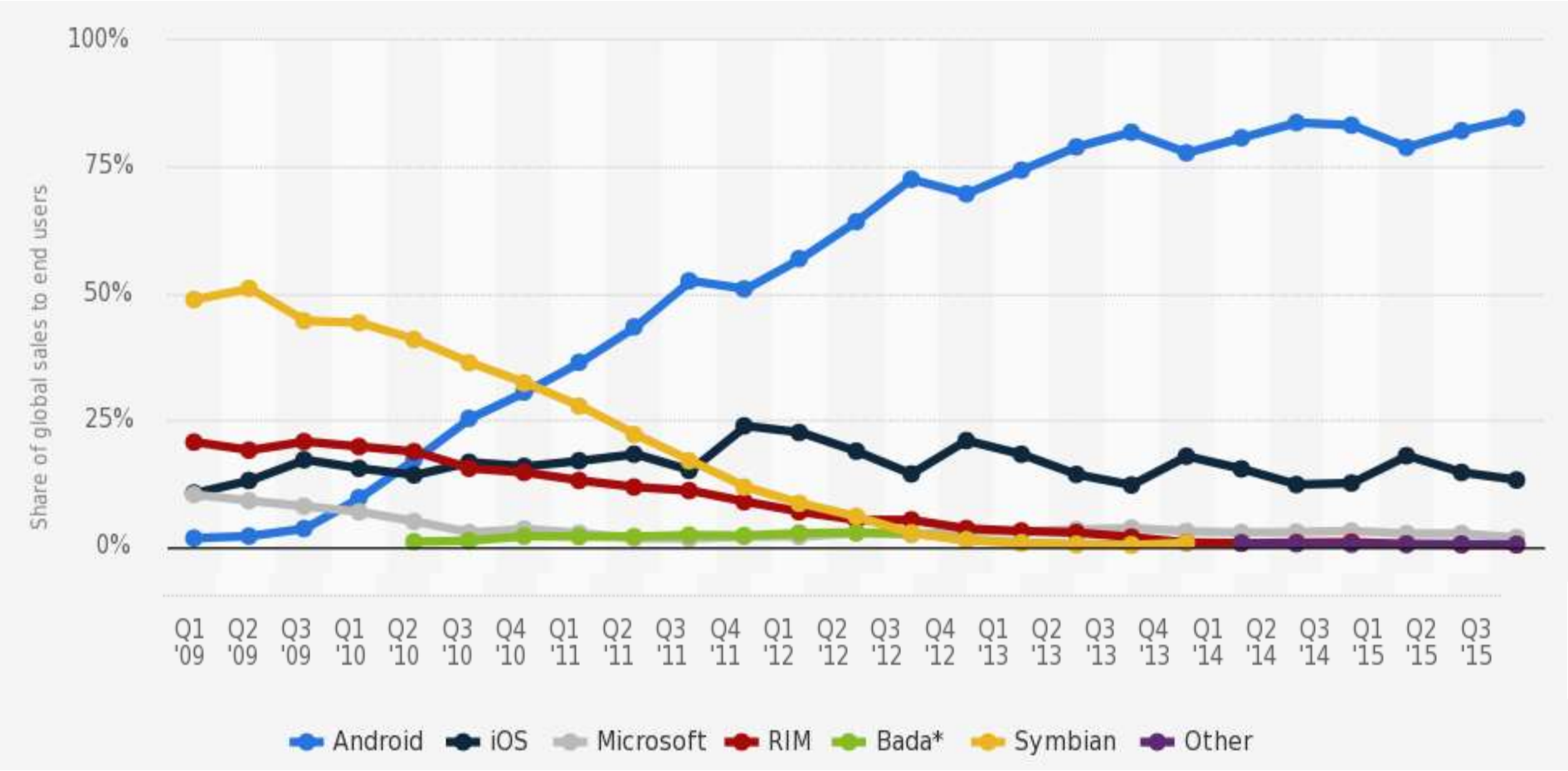
Worldwide smartphone market share in 2014-2017 (in unit shipments) [173]



Huawei: Chinese Oppo: Chinese Vivo: Chinese

5.1 Introduction to Atom-based platforms targeting smartphones (5)

Worldwide market share of smartphone OSs in 2009-2015 [174]



*

5.1 Introduction to Atom-based platforms targeting smartphones (6)

Worldwide market share of application processors in 1H 2017 used in smartphones (based on revenue) [175]

Vendor	Market share	Processor lines (examples)	ISA
Qualcomm (USA)	42 %	Snapdragon line 200-805 Snapdragoon 808-845	ARMv7 ARMv8
Apple (USA)	18 %	Apple A4-A6X Apple A7-A11	ARMv7 ARMv8
MediaTek (Taiwan)	18 %	Helio x10 Helio X20	ARMv7 ARMv8
Samsung (S. Korea)		Exynos 5 line Exynos 7/8/9	ARMv7 ARMv8

[Source: Strategy Analytics]

ARMv7: 32-bit
ARMv8: 64-bit

*

5.1 Introduction to Atom-based platforms targeting smartphones (7)

Intel's differentiation between high performance and low cost smartphone processors -1

At their Annual Investor Day on the 10. of May 2012 Intel differentiated two smartphone platform classes depending on their price – performance orientation, as indicated below

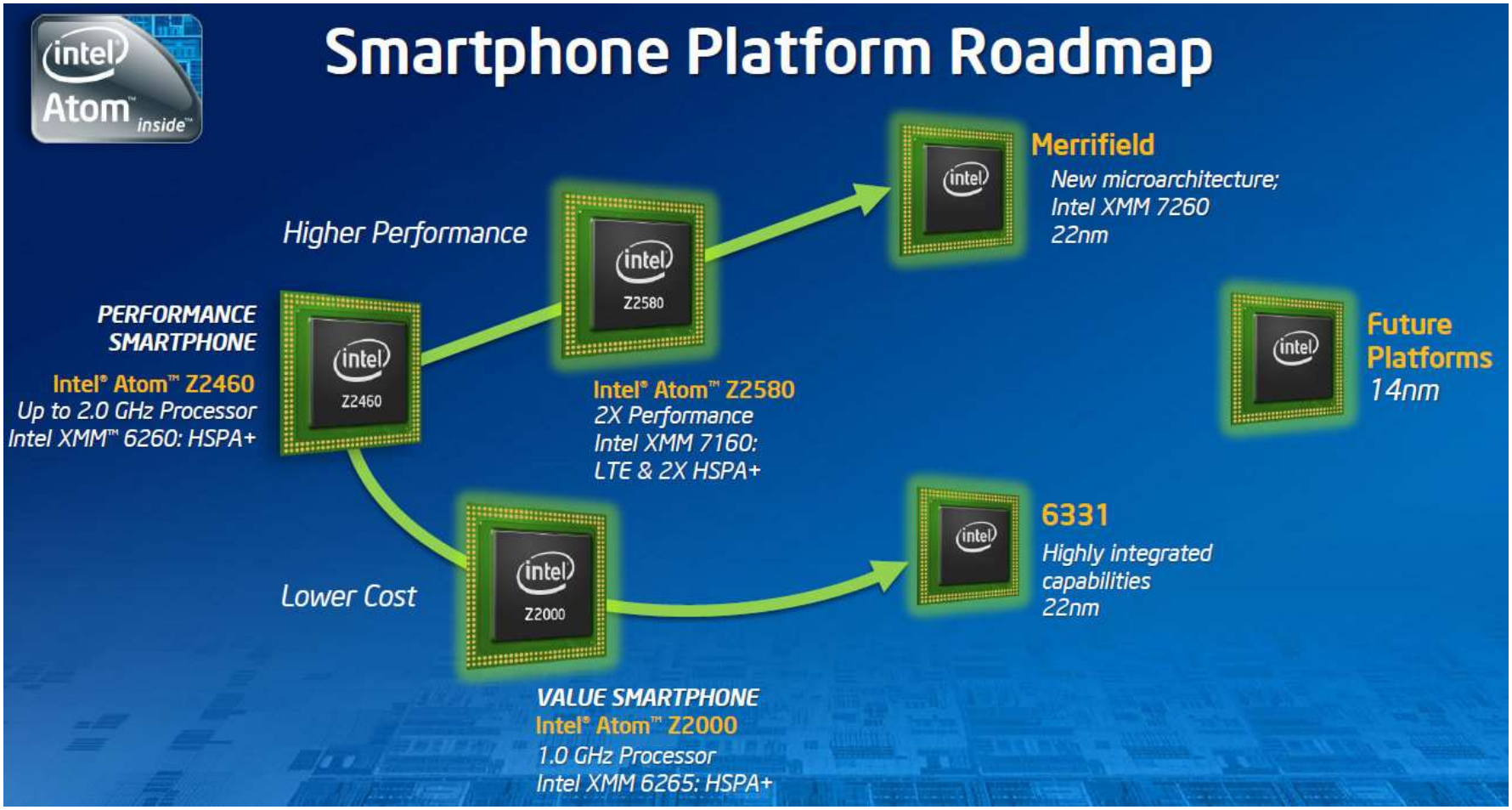


Figure: Intel's differentiation between high performance and low cost smartphone processors from 5/2012 [176]

5.1 Introduction to Atom-based platforms targeting smartphones (8)

Remarks to Intel's 05/2012 smartphone processor roadmap

- A subsequent announcement from 01/2013 disclosed that the low-cost model dubbed as the Z2000 is the Lexington processor.
- On the other hand, an internal roadmap from Q2/2013 [145]) revealed that the other "highly integrated" low-cost processor, designated as the 22 nm 6331 was changed into two models: into the Silverton CPU-based 22 nm Slayton with an integrated 3G modem and the Airmont CPU-based 14 nm Riverton with an integrated 4G (LTE) modem [145].
- Finally, in 11/2013 Intel announced the SoFIA series as a replacement of both the planned Slayton and Riverton processor models.

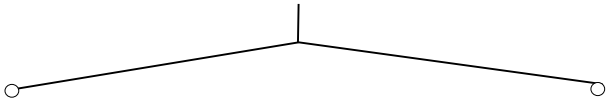
  The SoFIA series was stated to include Silverton-based models with integrated 3G (HSPA+) or 4G (LTE) modems, to be developed in partnership with the Chinese semiconductor firm Rockchip and to be fabricated externally by TSMC on a 28 nm process.

- At last the SoFIA series was launched in 03/2015 but cancelled in 04/2016.

Intel's differentiation between high performance and low cost smartphone processors -2

Accordingly, Intel's smartphone application processors can be subdivided into two groups when considering their price - performance orientation, i.e. into performance oriented and low-cost oriented smartphone platforms, as shown below.

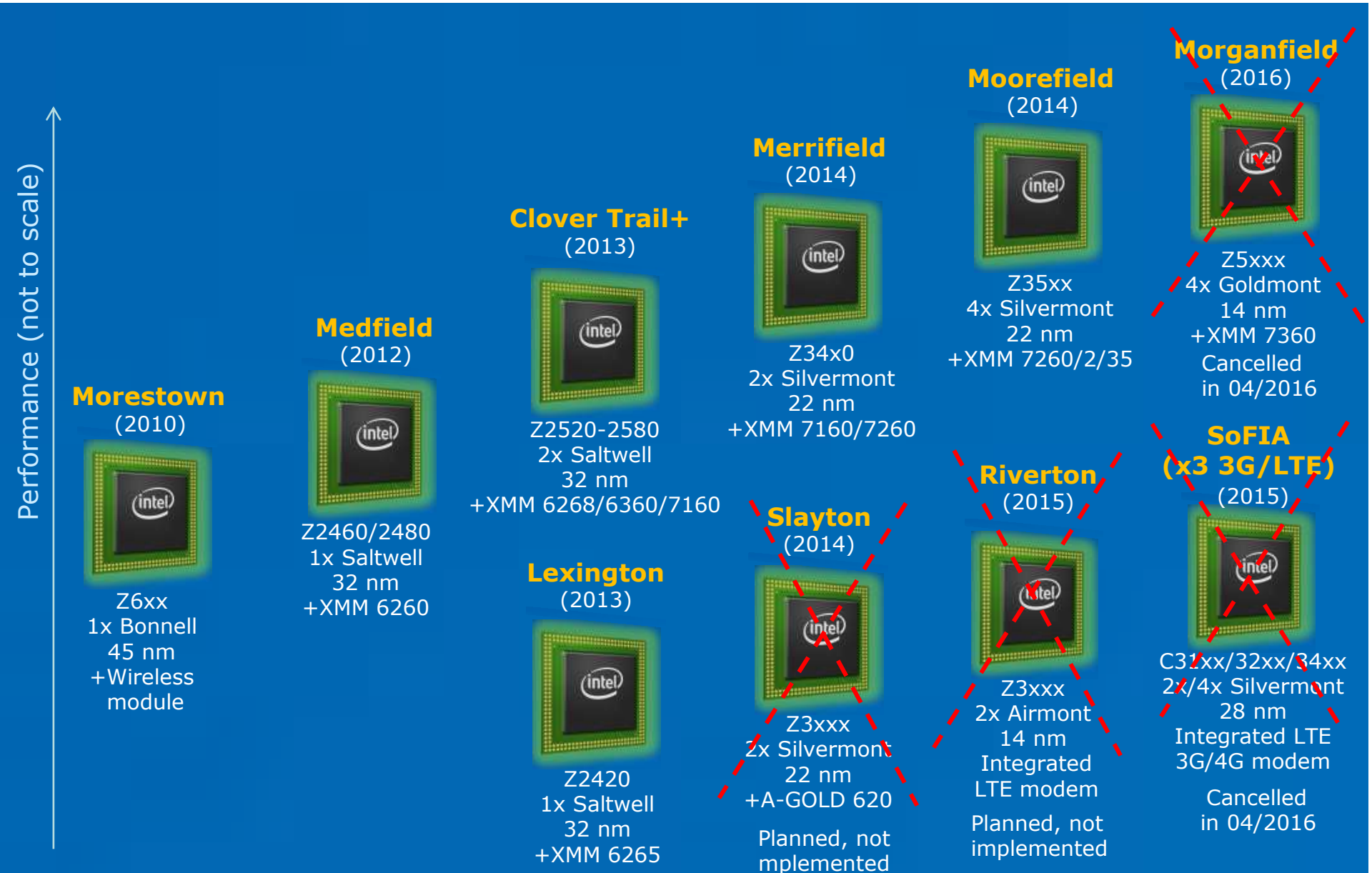
Intel's smartphone platforms classified according to their price - performance orientation (Only the implemented platforms are indicated)



Performance oriented smartphone platforms	**Low-cost oriented smartphone platforms**
Moorestown (2010)	*Lexington (2013)*
Medfield (2012)	*SoFIA (2015)*
Clover Trail+ (2013)	
Merrifield (2014)	
Moorefield (2014)	

5.1 Introduction to Atom-based platforms targeting smartphones (10)

Intel's Atom-based smartphone platforms (based on [43])



5.1 Introduction to Atom-based platforms targeting smartphones (11)

Intel's market share in the worldwide smartphone market

Intel entered the smartphone market in 1/2010 at the CES while announcing their Moorestown platform running under given versions of Moblin (Intel's Linux alternative), MeeGo (Intel's and Nokia's Linux-based OS) or Android.

Although Intel quoted a few reference designs, actually no signs of shipping Moorestown-based smartphones could be found on the internet.

Subsequently, Intel introduced a number of more and more enhanced platforms, such as

- the Medfield platform (01/2012)
- the Lexington platform (01/2013) and
- the Clover Trail+ platform (02/2013) and
- the Merrifield platform (06/2013)
- the Moorefield platform (06/2014) and
- the SoFIA (x3) platform (03/2015)

No one of these platforms brought Intel the expected success, e.g. according to industry sources in 2014 Intel achieved only less than 1 % share in smartphone application processors revenue [177], so finally Intel quoted both the smartphone and tablet market segments in 04/2016, as detailed in Section 6.

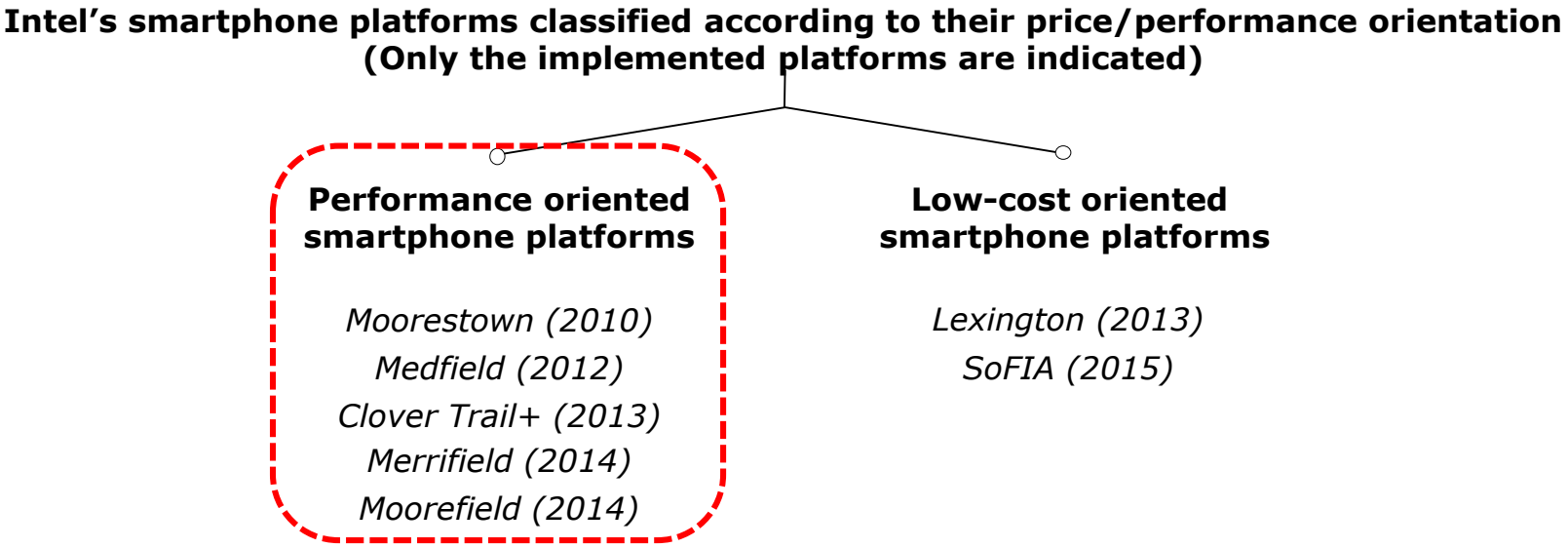
5.2 Performance oriented smartphone platforms

- 5.2.1 Overview of Intel's performance oriented smartphone platforms
- 5.2.2 The Moorestown platform
- 5.2.3 The Medfield platform
- 5.2.4 The Clover Trail+ platform as a smartphone platform
- 5.2.5 The Merrifield platform
- 5.2.6 The Moorefield platform
- 5.2.7 The Morganfield platform

5.2.1 Overview of Intel’s performance oriented smartphone platforms

5.2.1 Overview of Intel's performance oriented smartphone platforms

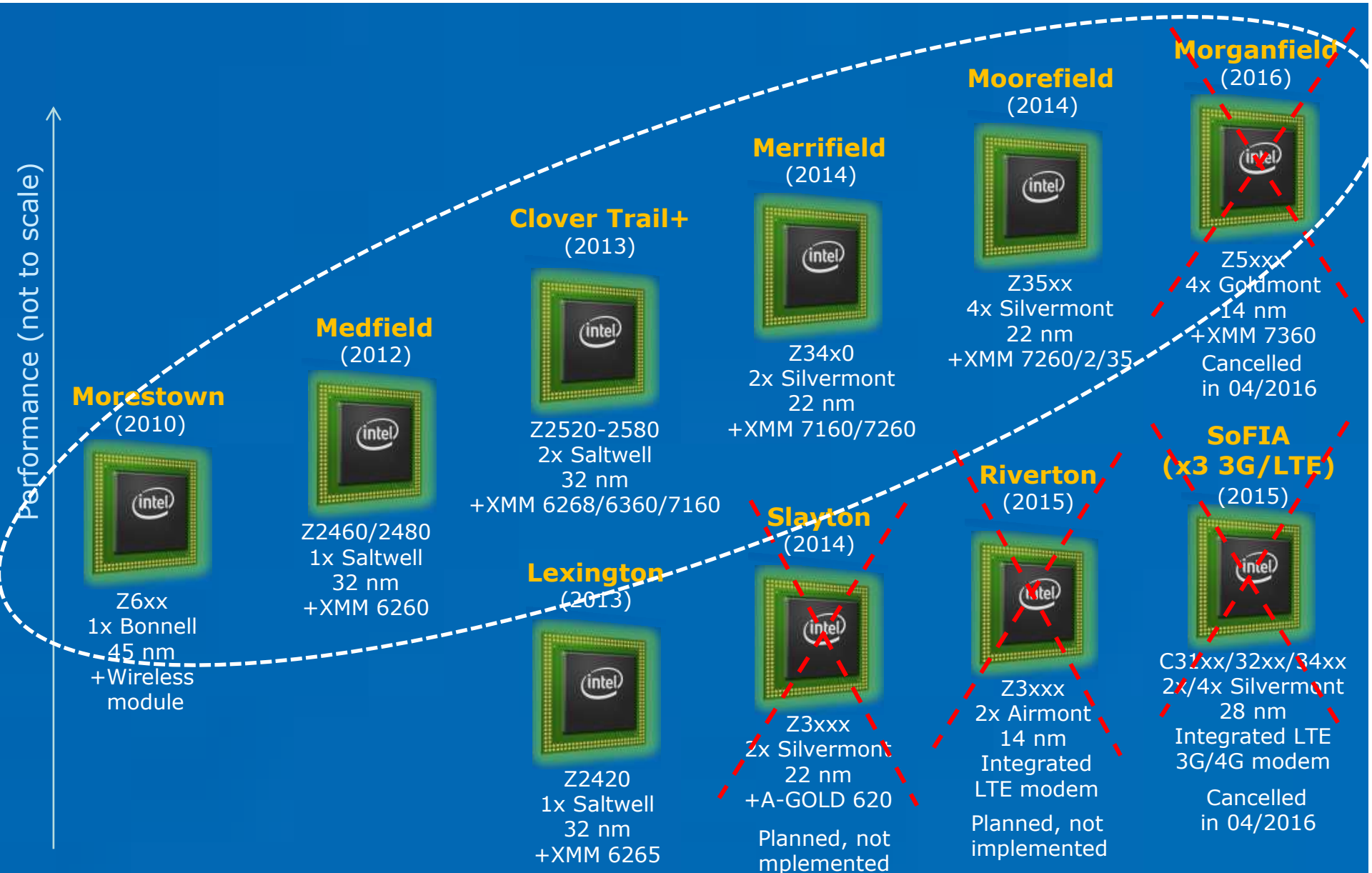
As already mentioned, Intel's smartphone families can be subdivided into two groups according to the targeted price/performance points, as shown below.



In this Section we discuss Intel's performance oriented smartphone platforms.

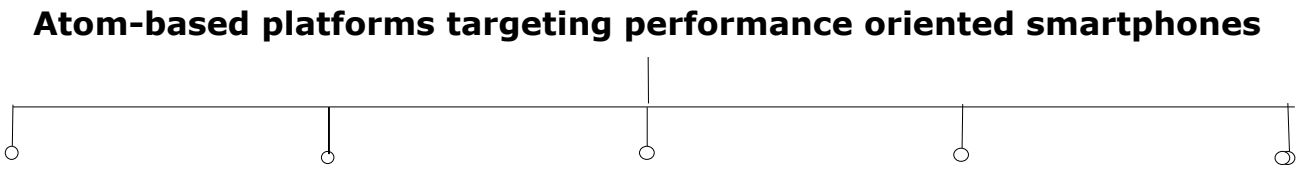
5.2.1 Overview of Intel's performance oriented smartphone platforms (2)

Intel's Atom-based smartphone platforms (based on [43])



5.2.1 Overview of Intel's performance oriented smartphone platforms (3)

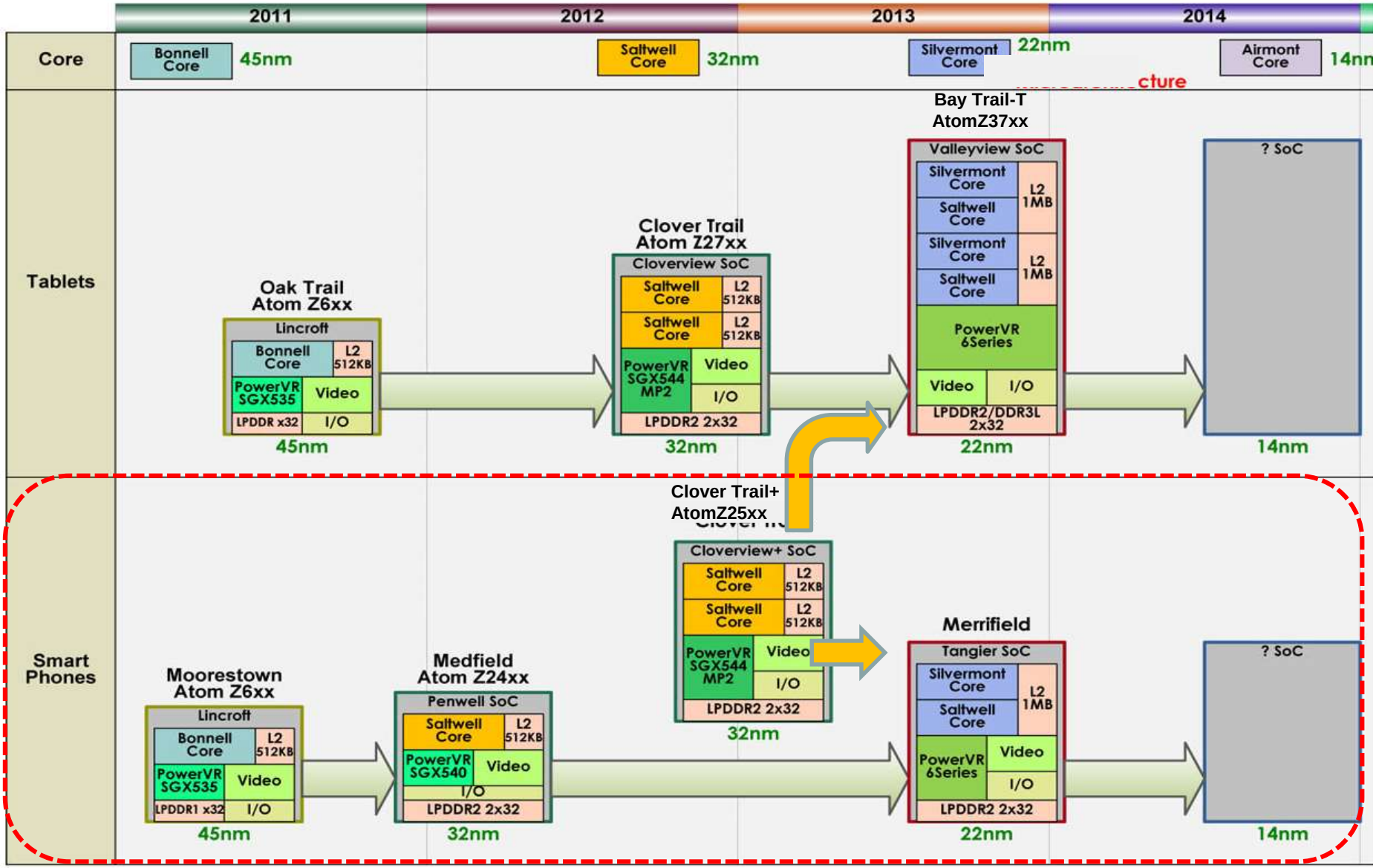
Overview of Atom-based platforms targeting performance oriented smartphones



	Moorestown	Medfield	Clover Trail+	Merrifield	Moorefield
Introduced	(05/2010)	01/2012	Q2/2013	02/2014	06/2014
AP processor	Lincroft	Pennwell	Cloverview	Tangier	Anniedale
Technology	45 nm	32 nm	32 nm	22 nm	22 nm
CPU microarchitecture	Bonnell 32-bit	Saltwell 32-bit	Saltwell 32-bit	Silvermont 64-bit	Silvermont 64-bit
No. of cores	1C	1C	2C	2C	4C
Chipset	MP20	SOC	SOC	SOC	SOC
OS	Moblin 2.1 MeeGo Android 2.1	Android 2.3.7/ 4.0/4/4.1.0.	Android 4.2	Android 4.4.2	Android 4..4.2

5.2.1 Overview of Intel's performance oriented smartphone platforms (4)

Evolution of Intel's high performance smart phone platforms [110]



5.2.1 Overview of Intel's performance oriented smartphone platforms (5)

Main features of the Atom-based platforms targeting performance oriented smartphones

Platform	Moorestown	Medfield	Clover Trail+	Merrifield	Moorefield
Available	(09/2009 announced)	01/2012	02/2013	02/2014	06/2014
Focus	High end smartphones	Mainstream smartphones	Smartphones	Smartphones	Smartphones
AP processor	Lincroft	Penwell	Cloverview	Tangier	Anniedale
Models	Z6xx	Z2460/Z2480	Z2520-Z2580	Z3460/Z3480	Z3530-Z3590
Technology	45nm	32nm	32nm	22nm	22nm
Die size	65 mm^2				
No. of trans.	140 mtrs				
CPU micro-arch.	Bonnell	Saltwell	Saltwell	Silvermont	Silvermont
32/64-bit	32-bit	32-bit	32-bit	64-bit	64-bit
No. of cores	1	1	2	2	4
HT	HT	HT	HT	no HT	no HT
fc [GHz] (Turbo)	0.9-1.9 GHz	1.2-2.0 GHz	1.2-2.0 GHz	1.6-2.13 GHz	1.33- 2.5 GHz
L2	512 kB	512 kB	2x512 kB	1 MB/2 cores	1 MB/2 cores
Mem. channels	Single 32-bit mem. ch. MC on proc. die	Dual 32-bit mem. ch. MC on proc. die	Dual 32-bit mem. ch. MC on proc. die	2x32-bit mem. ch. MC on proc. die	2x32-bit mem. ch. MC on proc. die
Memory	LPDDR1-400/DDR2-800	LPDDR2-800 POP	LPDDR2-1066 POP	LPDDR3-1066	LPDDR3-1600
GPU	GMA 600 (Power VR SGX 535)	Power VR SGX 540	Power VR SGX 544 MP2	Power VR G6400	Power VR G6430
DX	DX 9.0c	DX 9	DX 9.L3	DX10	DX10
Rear camera res.	5 Mpixel	8 Mpixel	13 Mpixel	13 Mpixel	13 Mpixel
GPU clock	200/400 MHz	400 MHz	300-533 MHz	400/457 MHz	457 MHz
ISP	—	ISP	ISP	ISP	ISP
Security Engine	—	Security Engine	Security Engine	Security Engine	Security Engine
Integr. baseband m.	No, wireless modem	No, XMM 6260	No, XMM 6268/6360/7160	No, XMM 7160/7260	No, XMM 7360
FSB	cDMI (8bit) (400 MT/s per dir.)	—	—	—	—
Proc. TDP	1.3-3.0 W				
Socket	BGA 518	BGA 617	BGA 760	PoP	PoP
Platform Cont. Hub	MP20 (Langwell)	—	—	—	—
OS at launch	Moblin 2.1 MeeGo/Android 2.1	Android 2.3.7/ 4.1.0	Android 4.2	Android 4.4.2	Android 4.4.2
Smartphone eExamples	Aava Virta Android LG GW990 both withdrawn	Lava Xolo X900 Lenovo K800 Motorola RAZRi Orange San Diego ZTE Grand X IN	Lenovo K900 ZTE Geek/ Grand X2 IN	Dell Venue 7 Dell Venue 8	Asus Fonepad 7 Asus Fonepad 8 Nokia N1, Dell Venue 8 7000,

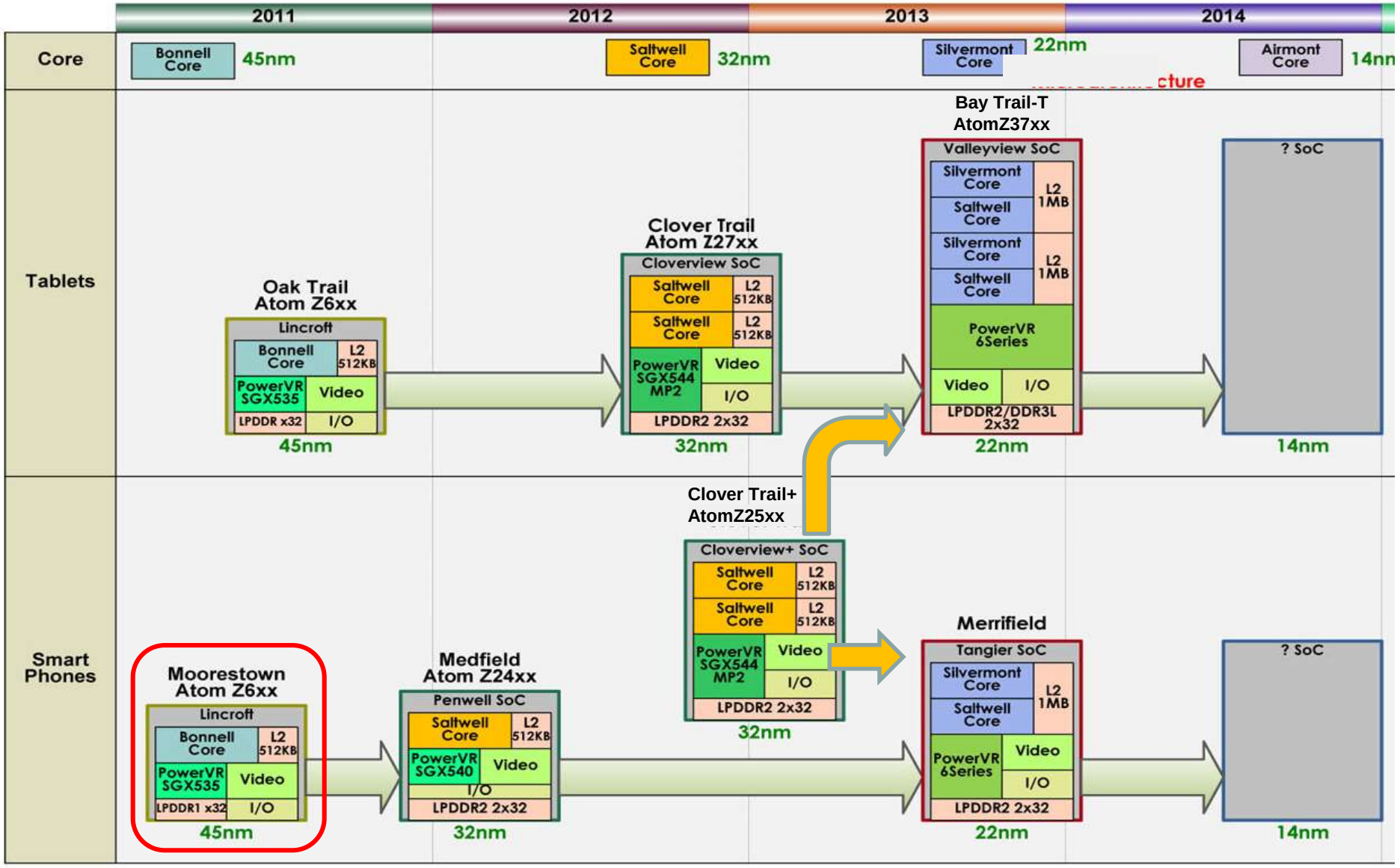
5.2.2 The Moorestown platform

5.2.2 The Moorestown platform

- It is Intel's first try to enter the smartphone space.
- Announced in 09/2009.
- Although it was a flop for Intel, as no one Moorestown-based smartphone design became marketed, it is of importance since Intel took over into the Moorestown platform a number of novel technologies that were introduced before into PCs and servers, like turbo boost technology (termed as Burst Mode or power gating, as discussed later in this Section.

5.2.2 The Moorestown platform (2)

Positioning the Moorestown platform in Intel's tablet and smart phone platforms [110]



5.2.2 The Moorestown platform (3)

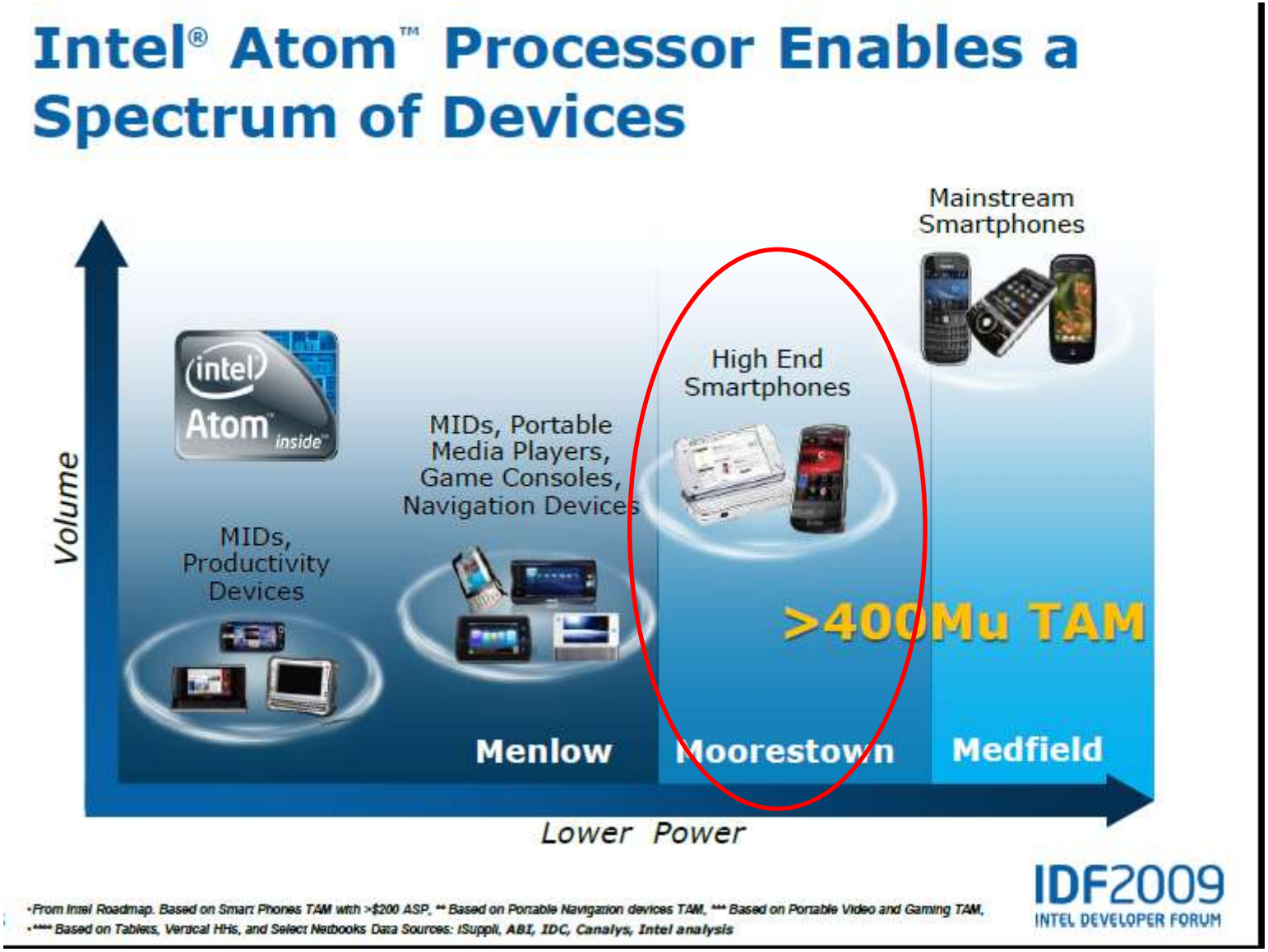
First reference to the Moorestown platform

Intel first mentioned it already at announcing the Atom line of processors in 4/2008, this indicates that the firm had had very high expectations concerning the market potential of this platform.

5.2.2 The Moorestown platform (4)

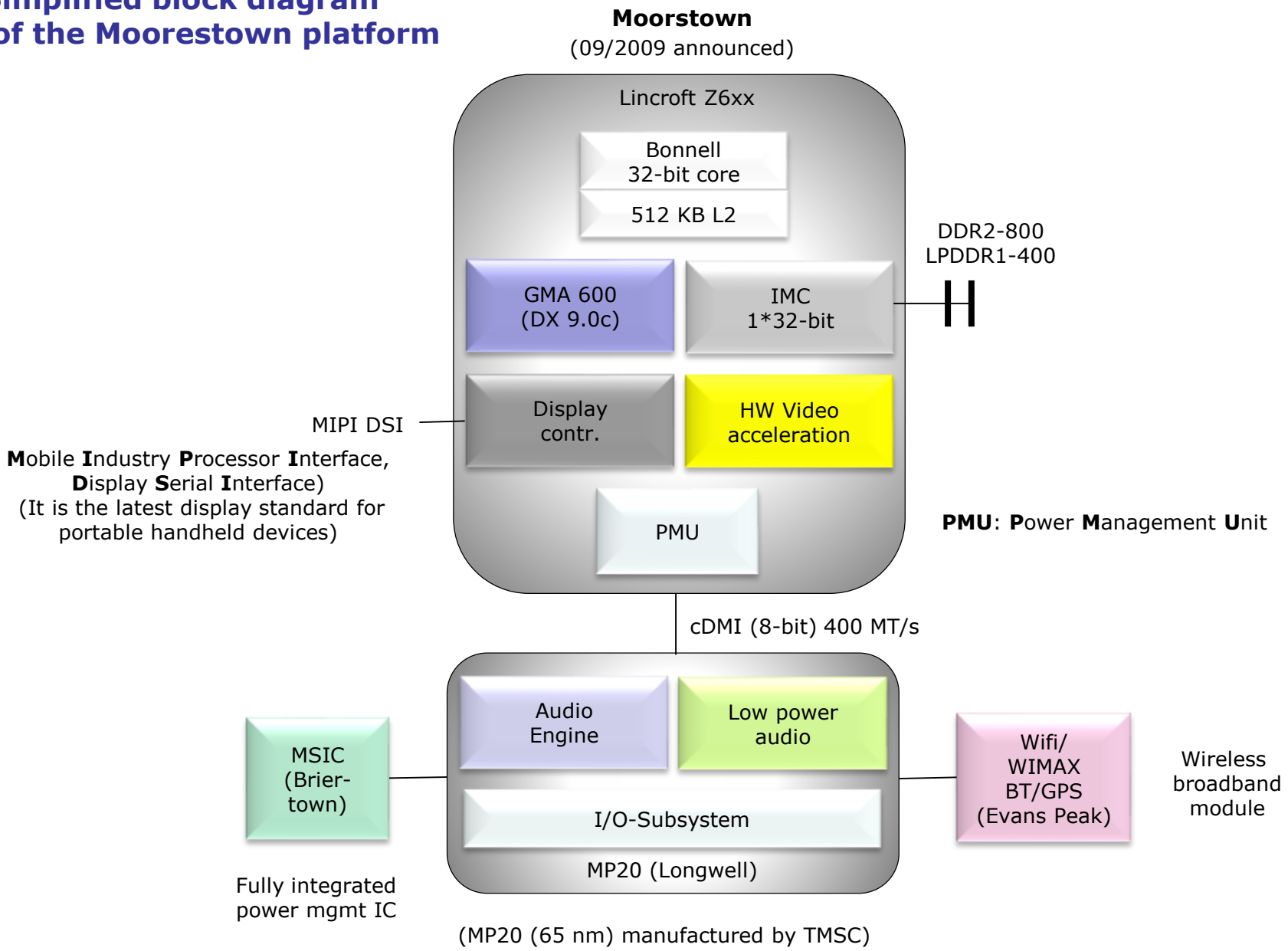
Announcing the Moorestown platform

Intel announced this platform at its IDF in 9/2009 while revealing certain technical details.



5.2.2 The Moorestown platform (5)

Simplified block diagram of the Moorestown platform



5.2.2 The Moorestown platform (6)

Remarks -1

We point out the following features of the Lincroft processor as used in the Moorestown platform:

- Processor models introduced
  - Z6xx

  Here we note that we designated the Lincroft processors by Z6xx without any specific model number.

  The reason for this is that we could not find any Moorestown related publication with model numbers specified.
- Core count/No. of memory channels
  - single core/single memory channel
- Microarchitecture
  - 32 bit Bonnell microarchitecture
- Technology, die size and transistor count
  - 45 nm technology, 65 mm2, 140 mtrs
- Key innovation to boost performance
  - Burst mode (Turbo Boost technology)
- Key innovation to lower power consumption
  - Distributed power gating
  - S0i1/S0i3 idle system states
- OS support
  - Moblin 2.1/MeeGo/Android 2.1

5.2.2 The Moorestown platform (7)

Remarks -2

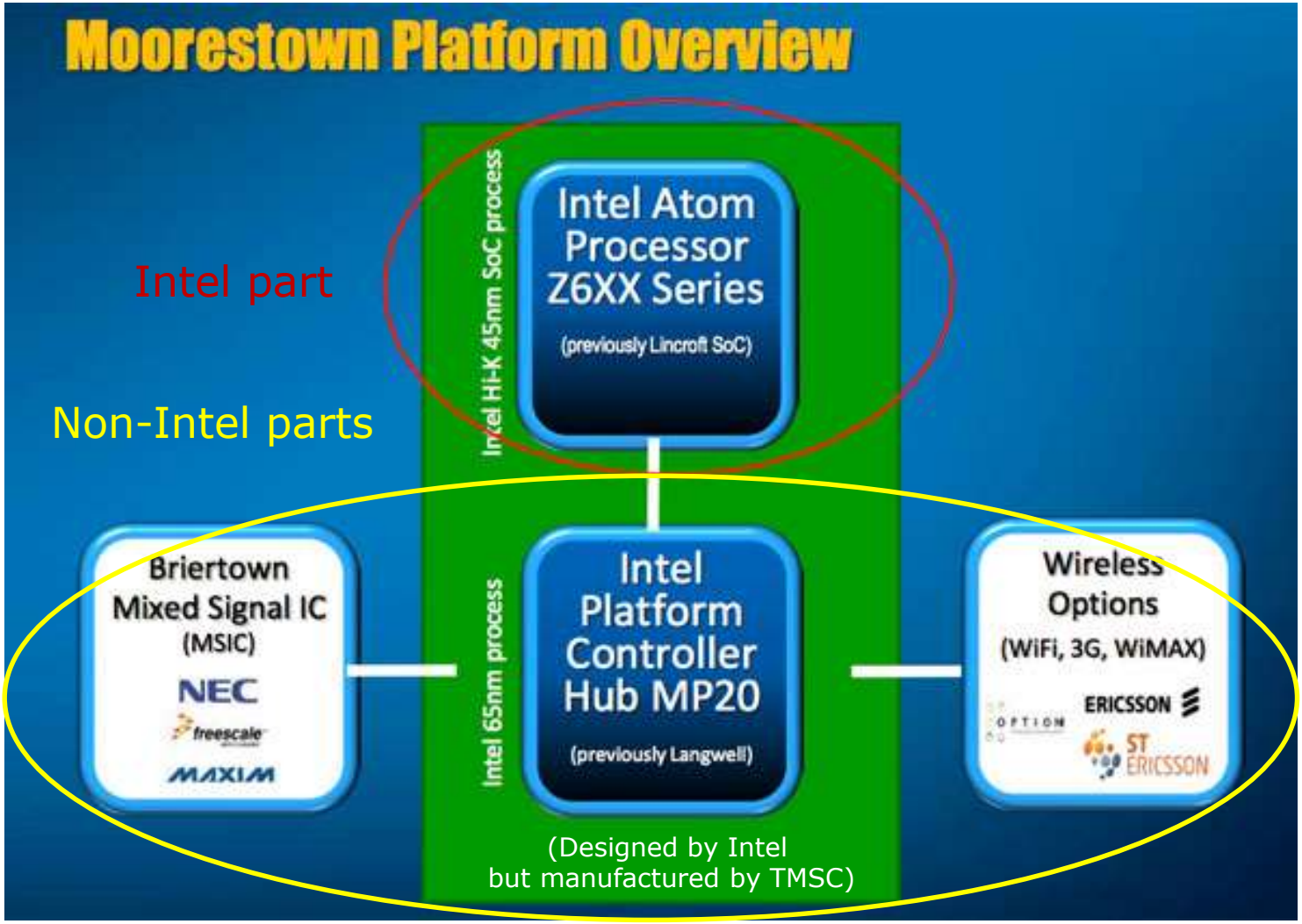
The Lincroft chip is used also in the Oak Trail tablet platform

Nevertheless, the Moorestown platform

- has a different companion chip (the MP20) rather than the SM35 of the Oak Trail platform,
- has a number of additional performance and low power features, detailed in this Section, and
- runs under the OSs Moblin 2.1, MeeGo and Android rather than Windos 7, Moblin and Android used for the Oak Trail platform.

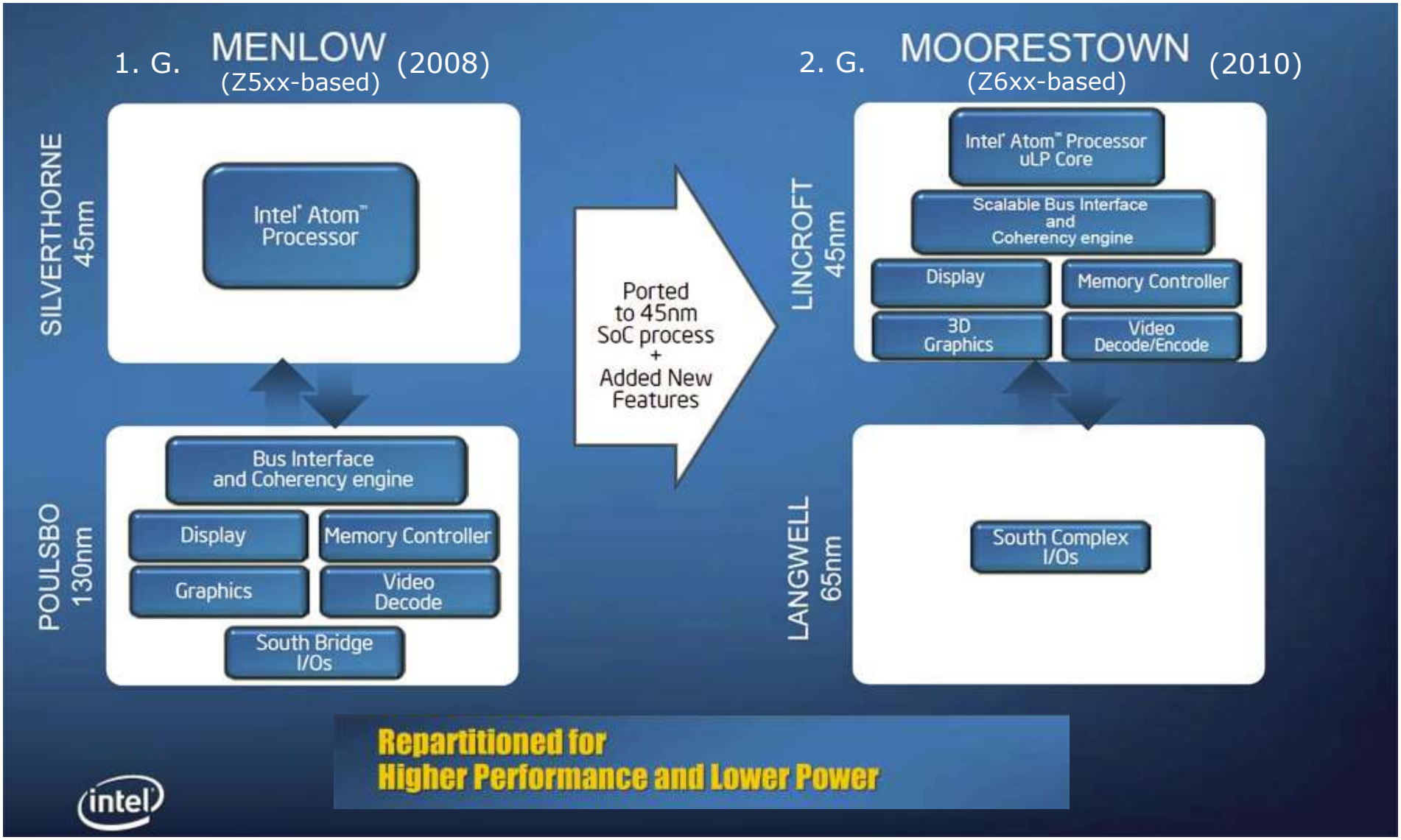
5.2.2 The Moorestown platform (8)

Including non-Intel fabricated parts into the Moorestown platform [54]



5.2.2 The Moorestown platform (9)

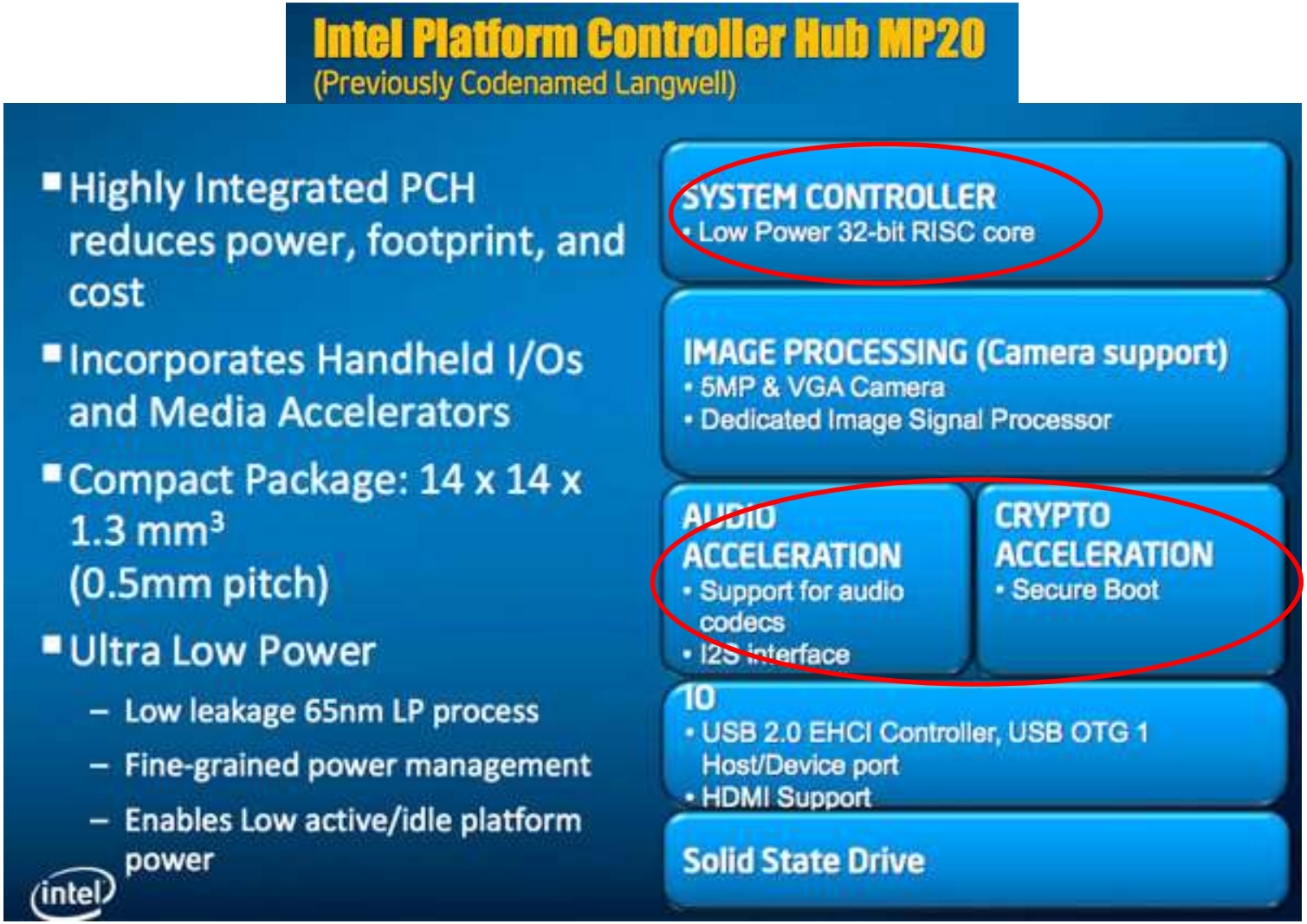
Evolution of the Moorestown platform architecture vs. the Menlow tablet platform [124]



5.2.2 The Moorestown platform (10)

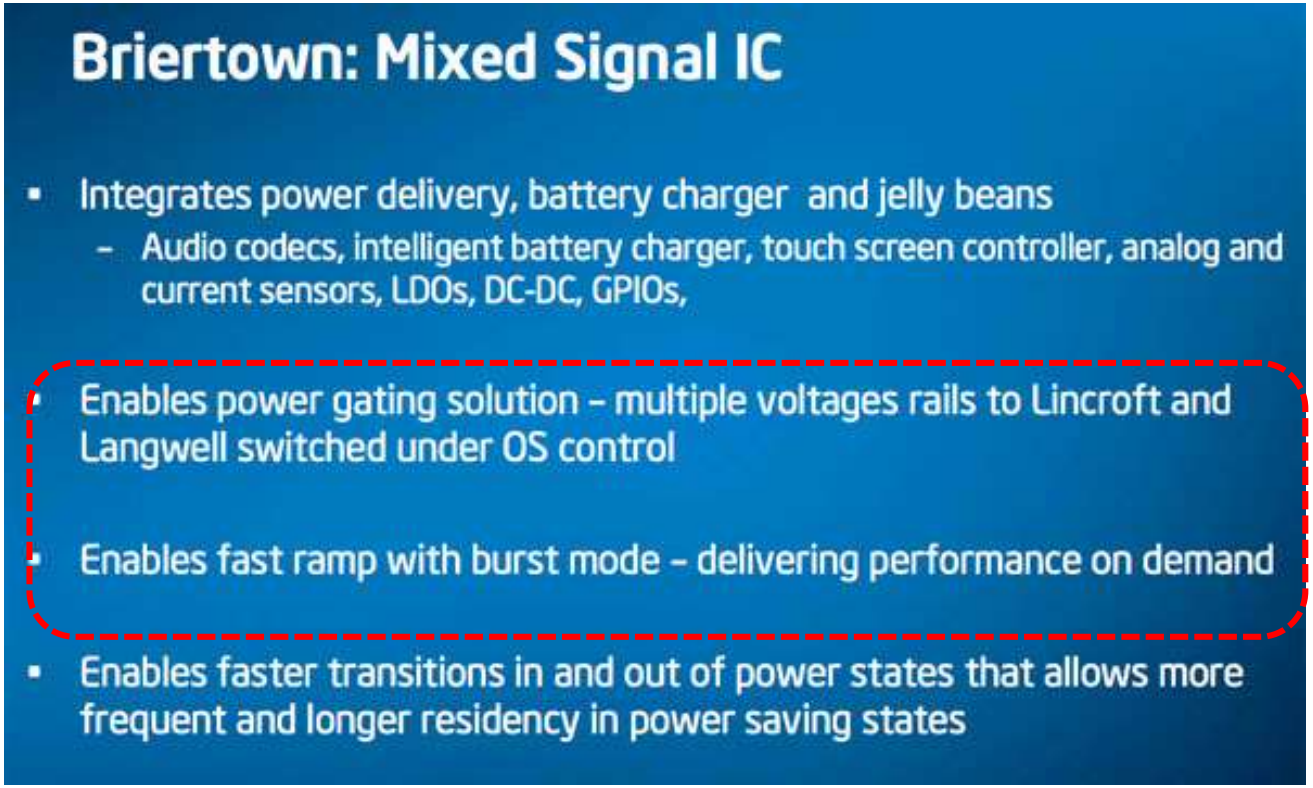
Features and block diagram of the MP20 (Langwell) PCH (Platform Controller Hub) [54]

It was designed by Intel but manufactured by TMSC in 65 nm technology.



5.2.2 The Moorestown platform (11)

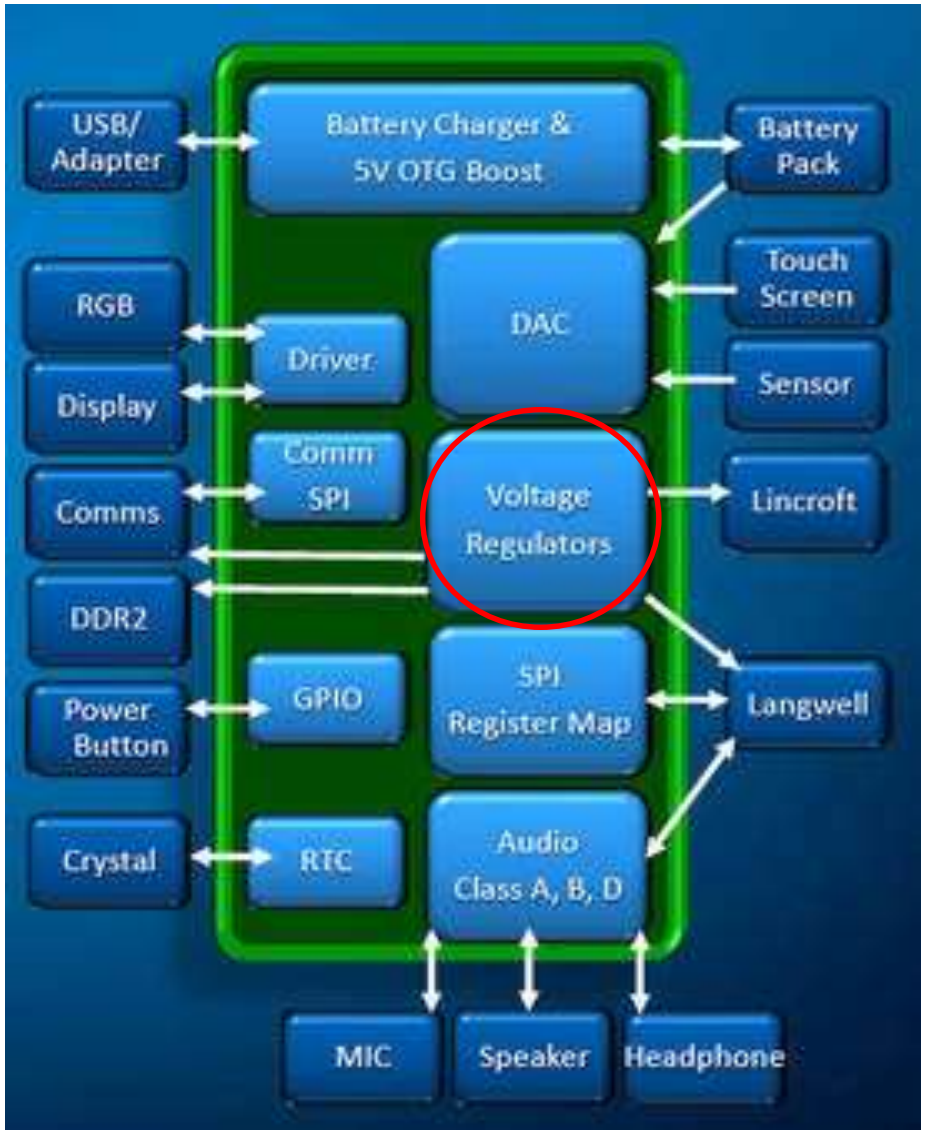
Tasks of the MSIC (Mixed Signal IC/Briertown) [54]



5.2.2 The Moorestown platform (12)

Block diagram of the MSIC (Mixed Signal IC/Briertown) [125]

It was designed by Intel, but its manufacturing has been outsourced to NEC, Freescale, and Maxim.



5.2.2 The Moorestown platform (13)

Main features of the Moorestown platforms targeting performance oriented smartphones

Platform	Moorestown	Medfield	Clover Trail+	Merrifield	Moorefield
Available	(09/2009 announced)	01/2012	02/2013	02/2014	06/2014
Focus	High end smartphones	Mainstream smartphones	Smartphones	Smartphones	Smartphones
AP processor	Lincroft	Penwell	Cloverview	Tangier	Anniedale
Models	Z6xx	Z2460/Z2480	Z2520-Z2580	Z3460/Z3480	Z3530-Z3590
Technology	45nm	32nm	32nm	22nm	22nm
Die size	65 mm^2				
No. of trans.	140 mtrs				
CPU micro-arch.	Bonnell	Saltwell	Saltwell	Silvermont	Silvermont
32/64-bit	32-bit	32-bit	32-bit	64-bit	64-bit
No. of cores	1	1	2	2	4
HT	HT	HT	HT	no HT	no HT
fc [GHz] (Turbo)	0.9-1.9 GHz	1.2-2.0 GHz	1.2-2.0 GHz	1.6-2.13 GHz	1.33- 2.5 GHz
L2	512 kB	512 kB	2x512 kB	1 MB/2 cores	1 MB/2 cores
Mem. channels	Single 32-bit mem. ch. MC on proc. die	Dual 32-bit mem. ch. MC on proc. die	Dual 32-bit mem. ch. MC on proc. die	2x32-bit mem. ch. MC on proc. die	2x32-bit mem. ch. MC on proc. die
Memory	LPDDR1-400/DDR2-800	LPDDR2-800 POP	LPDDR2-1066 POP	LPDDR3-1066	LPDDR3-1600
GPU	GMA 600 (Power VR SGX 535)	Power VR SGX 540	Power VR SGX 544 MP2	Power VR G6400	Power VR G6430
DX	DX 9.0c	DX 9	DX 9.L3	DX10	DX10
Rear camera res.	5 Mpixel	8 Mpixel	13 Mpixel	13 Mpixel	13 Mpixel
GPU clock	200/400 MHz	400 MHz	300-533 MHz	400/457 MHz	457 MHz
ISP	—	ISP	ISP	ISP	ISP
Security Engine	—	Security Engine	Security Engine	Security Engine	Security Engine
Integr. baseband m.	No, wireless modem	No, XMM 6260	No, XMM 6268/6360/7160	No, XMM 7160/7260	No, XMM 7360
FSB	cDMI (8bit) (400 MT/s per dir.)	—	—	—	—
Proc. TDP	1.3-3.0 W				
Socket	BGA 518	BGA 617	BGA 760	PoP	PoP
Platform Cont. Hub	MP20 (Langwell)	—	—	—	—
OS at launch	Moblin 2.1 MeeGo/Android 2.1	Android 2.3.7/ 4.1.0	Android 4.2	Android 4.4.2	Android 4.4.2
Smartphone eExamples	Aava Virta Android LG GW990 both withdrawn	Lava Xolo X900 Lenovo K800 Motorola RAZRi Orange San Diego ZTE Grand X IN	Lenovo K900 ZTE Geek/ Grand X2 IN	Dell Venue 7 Dell Venue 8	Asus Fonepad 7 Asus Fonepad 8 Nokia N1, Dell Venue 8 7000,

5.2.2 The Moorestown platform (14)

Lincroft's innovations targeting performance [93]

- Wide range of scalable frequencies for multimedia blocks
- Intel Hyper threading technology
- Burst Mode technology
- Bus Turbo technology

5.2.2 The Moorestown platform (15)

a) Burst Mode technology-1 [54]

- About two years after the introduction of the Bonnell CPU Intel introduced the Burst mode technology in their Atom line.
- With the Burst Mode additional P-states are exposed for the OS such that if there is a power headroom available, e.g. after an idle period, performance can be increased over the TDP limited performance for a short time.
- The Burst Mode introduced is controlled by the OS such that all available P-states (f_c/V_{core} states), including the P-states belonging to the Burst mode, are enumerated by the BIOS for the OS as available P-states.
- The OS directs the P-state usage according to the utilization grade of the CPU.

This means that if there is a power headroom, e.g. after an idle period, and there is need for high performance, the OS requests the highest P-state (Burst frequency) and lets operate the processor in the Burst Mode until the chip or the external case becomes too hot, i.e. until the chips junction temperature (Tj) or the case temperature (Tskin) becomes higher than a predefined value (assuming that there is need for the highest P-state.

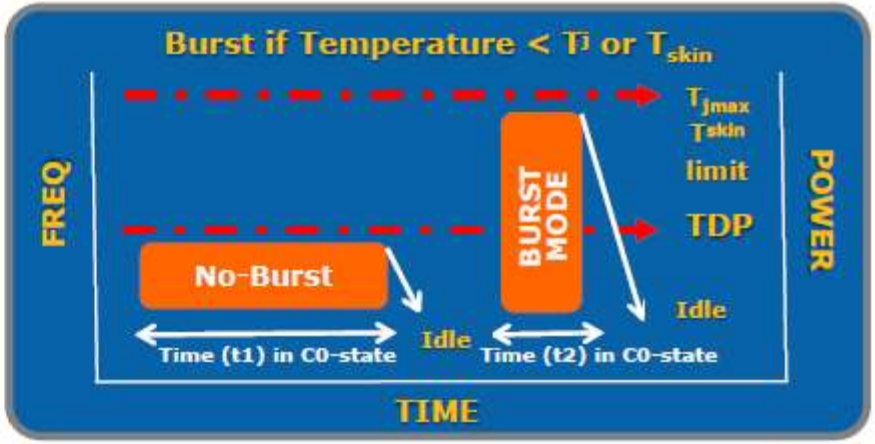
In these cases the processor will be throttled to a lower operating point (P-state).

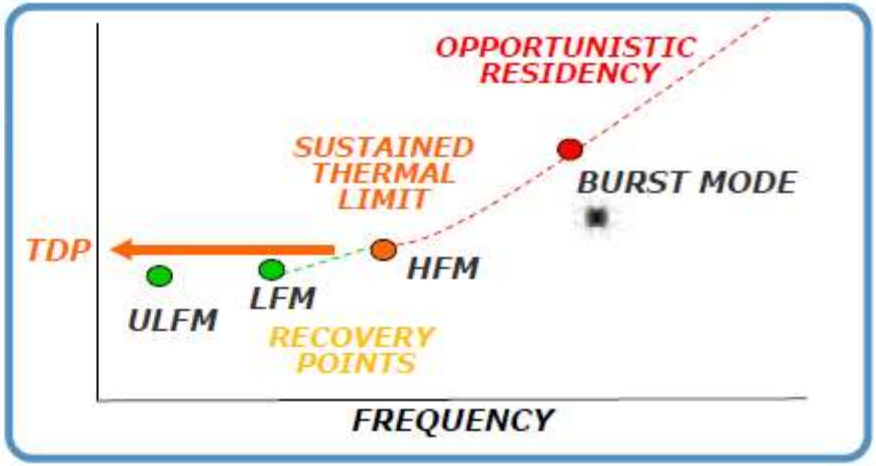
The next Figure illustrates the operation of the Burst Mode, as introduced in the Lincroft processor.

a) Burst Mode technology-2 [18]

It is designated also as the Burst Performance Technology (BPT).

- Takes advantage of Thermal headroom on T_J and T_{Skin} for short duration
- System reduces frequency to Recovery points when T_{Skin} thresholds are exceeded





Intel® BPT provides on-demand performance and Battery Life Saving without impacting thermal design

5.2.2 The Moorestown platform (17)

Remark 1

Skin temperature t_{skin} is the temperature of the computer case, like the case of a laptop.

If the laptop case becomes hotter than a given temperature it can be unpleasant for the user having the laptop on his or her lap.

Remark 2

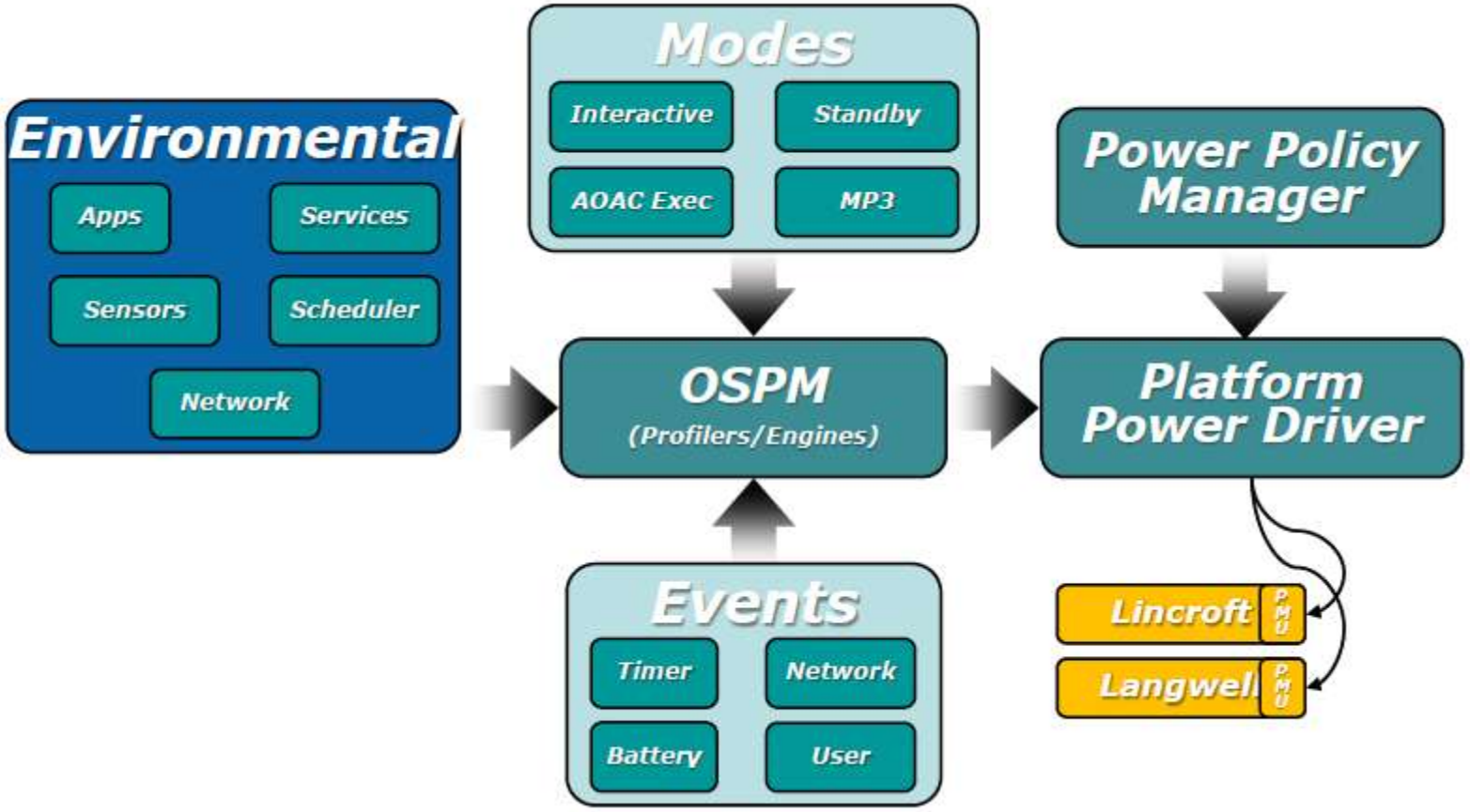
Here we note that the Burst mode as introduced into the Atom line is similar to the Turbo Boost technology introduced into the Nehalem processor in 11/2008 nevertheless it differs in implementation details.

On the other hand, subsequently also the Turbo Boost technology was further developed to the Turbo Boost technology 2.0 in Sandy Bridge processors (1/2011).

This technology was then introduced into the 22 nm Silvermont-based Atom processors.

5.2.2 The Moorestown platform (18)

Principle of Moorestown OS directed power management [18]

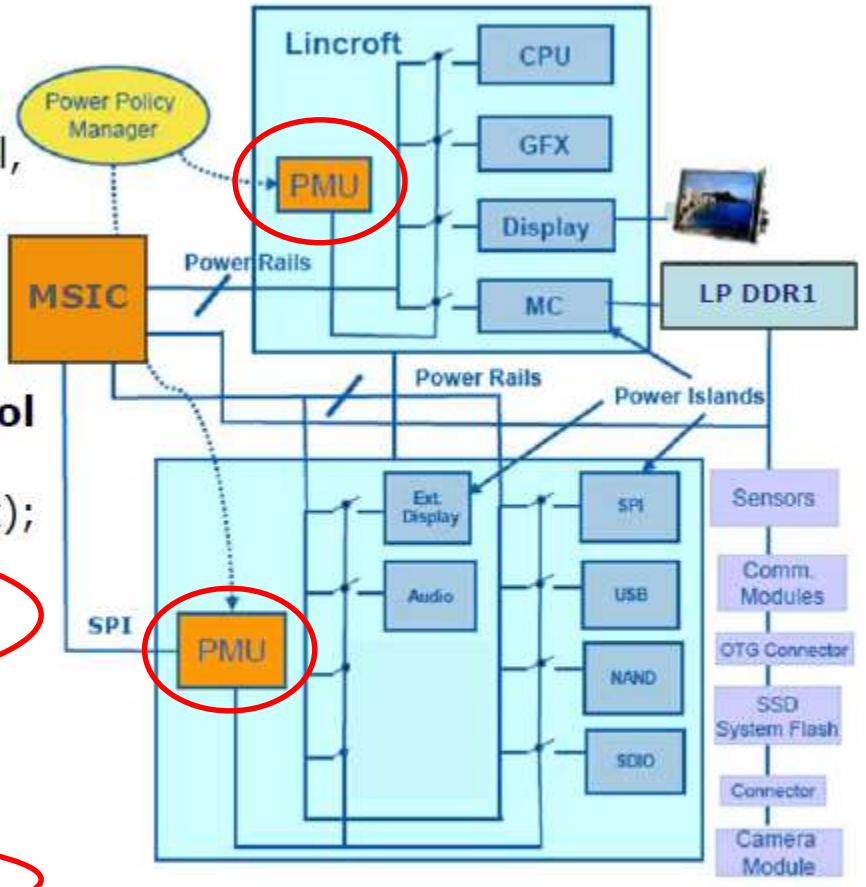


OSPM is an event-driven engine to actively manage power modes

5.2.2 The Moorestown platform (19)

Implementation of Moorestown OS directed power management [18]

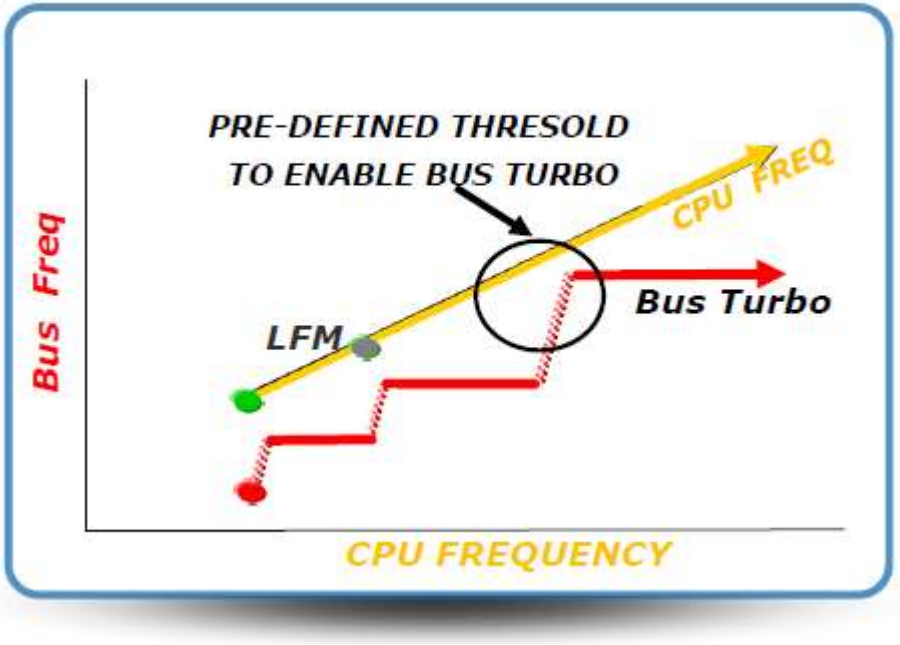
- **Well defined Operating Modes**
  - Standby, Internet Browsing, MP3 Playback, Video Playback, Voice Call, Video Capture, etc.
- **OS-Directed Power Management**
  - OSPM Policy Manager for Mode Control
- **OS-Transparent sub-system control with Firmware & hardware**
  - Idle States: System(Sx), Device(Dx);
  - Micro-controller based PMUs in Lincroft and Langwell provide autonomous PM events control
- **Fine-grain Power Management**
  - Power Islands for Optimum power-down of sub-systems
  - Aggressive Power and Clock gating
  - Integrated Clocks and PMIC VR power down via MSIC



5.2.2 The Moorestown platform (20)

b) Bus Turbo technology [18]

- Motivation
  - Reduce memory latency and increase bus BW when CPU bursting at higher frequencies
- Implementation
  - HW dynamically increases BUS freq. at pre-set CPU freq.
  - No need to re-lock PLL that provides clock to bus
    - Uses clock divider
  - Re-lock CPU PLL



"Bus Turbo Mode" provides substantially higher bus bandwidth

5.2.2 The Moorestown platform (21)

Lincroft's innovations targeting low power [93]

- Low power architecture features
- Distributed power gating
- S0i1/S0i3 idle system states
- Enhanced Geyserville technology

5.2.2 The Moorestown platform (22)

a) Distributed power gating

Intel introduced power gating into their Nehalem line of processors in 2008.

With the Lincroft chip of the Moorestown platform Intel made use of power gating also in their Atom-based mobile processors.

Intel designates power gating in the Lincroft processor as distributed power gating to stress that power gating is used in a large scale, i.e. for all functional units (except of the CPU).

5.2.2 The Moorestown platform (23)

Implementation of power gating in the Lincroft chip-1 [92]

- To reduce idle power the Lincroft chip is divided into nineteen power domains such that each functional unit acts as a power domain, except of the Atom core, as shown in the Figure below.
- 12 power rails provide power supply for the 19 power domains.
- If a functional unit is not in use the related power domain can be turned off by on-die power gates (power transistors).

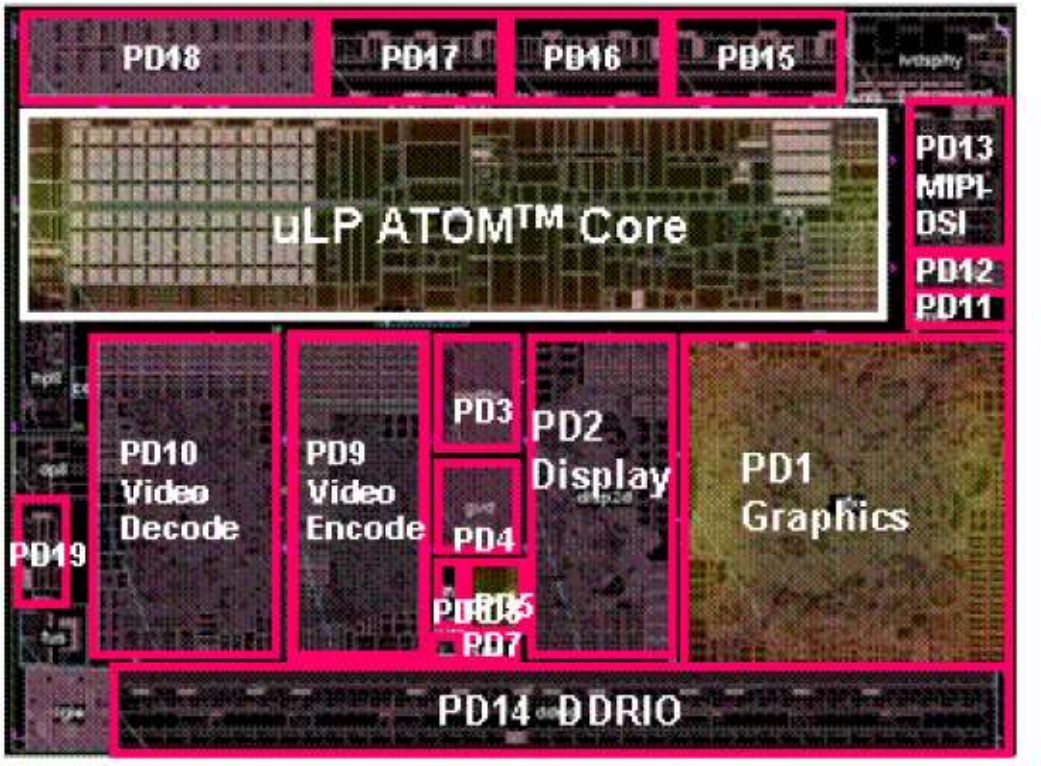


Figure: Powergated domains of the Lincoroft chip [92]

5.2.2 The Moorestown platform (24)

Implementation of power gating in the Lincroft chip-2 [92]

- The embedded powergate cells are switched on or off by powergate control signals that are daisy chained, as indicated below.

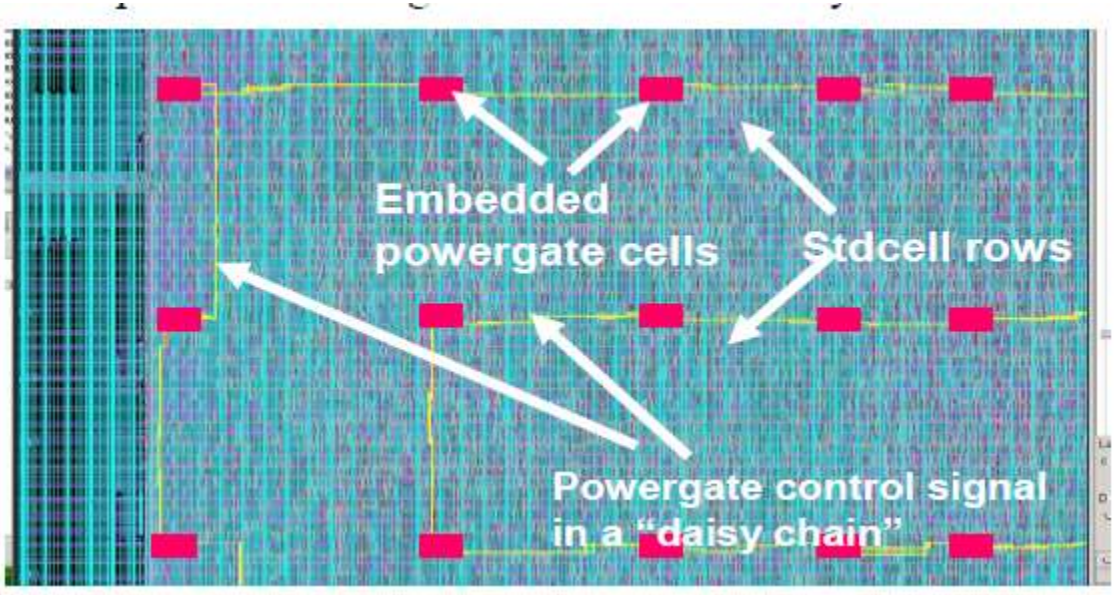


Figure: Distributed powergate cells in a powergated domain [92]

- Thus idle power is significantly reduced by shutting down unused portions of the chip.
- By contrast, the Atom core is power managed by C-states.

All-in-all, power gates cover about 70 % of the chip area.

5.2.2 The Moorestown platform (25)

Implementation of power gating in the Lincroft chip-3 [93]

- There is a SW interface for power management of the powergated islands.
- HW manages the sequencing of the powergate control signals.

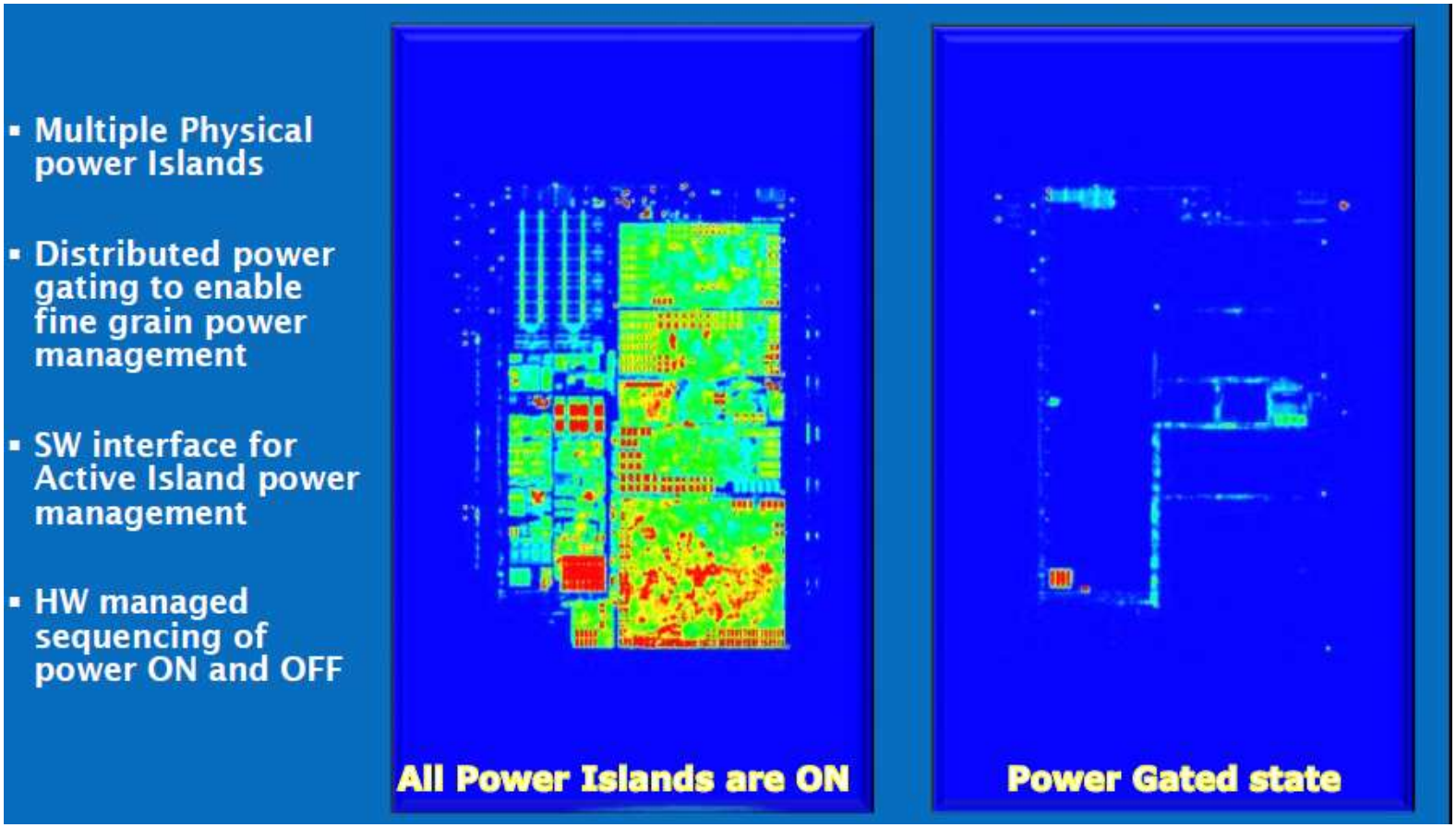


Figure: Infrared emission (IREM) image of a full on vs. powergated Licoln chip [93]

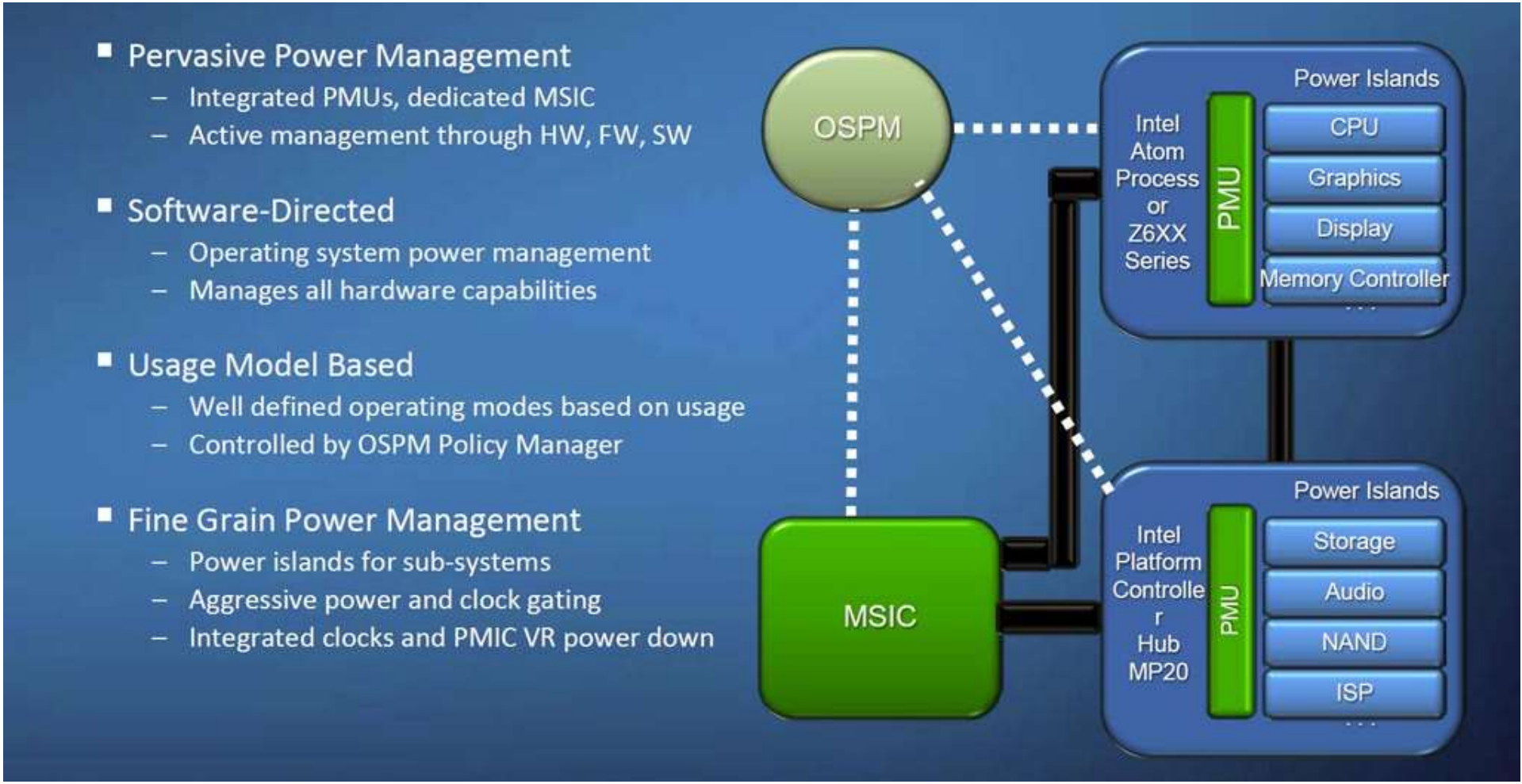
5.2.2 The Moorestown platform (26)

Implementation of power gating in the Lincroft chip-4 [93]

- Aggressive power gating enables up-to 50x reduction in idle power.

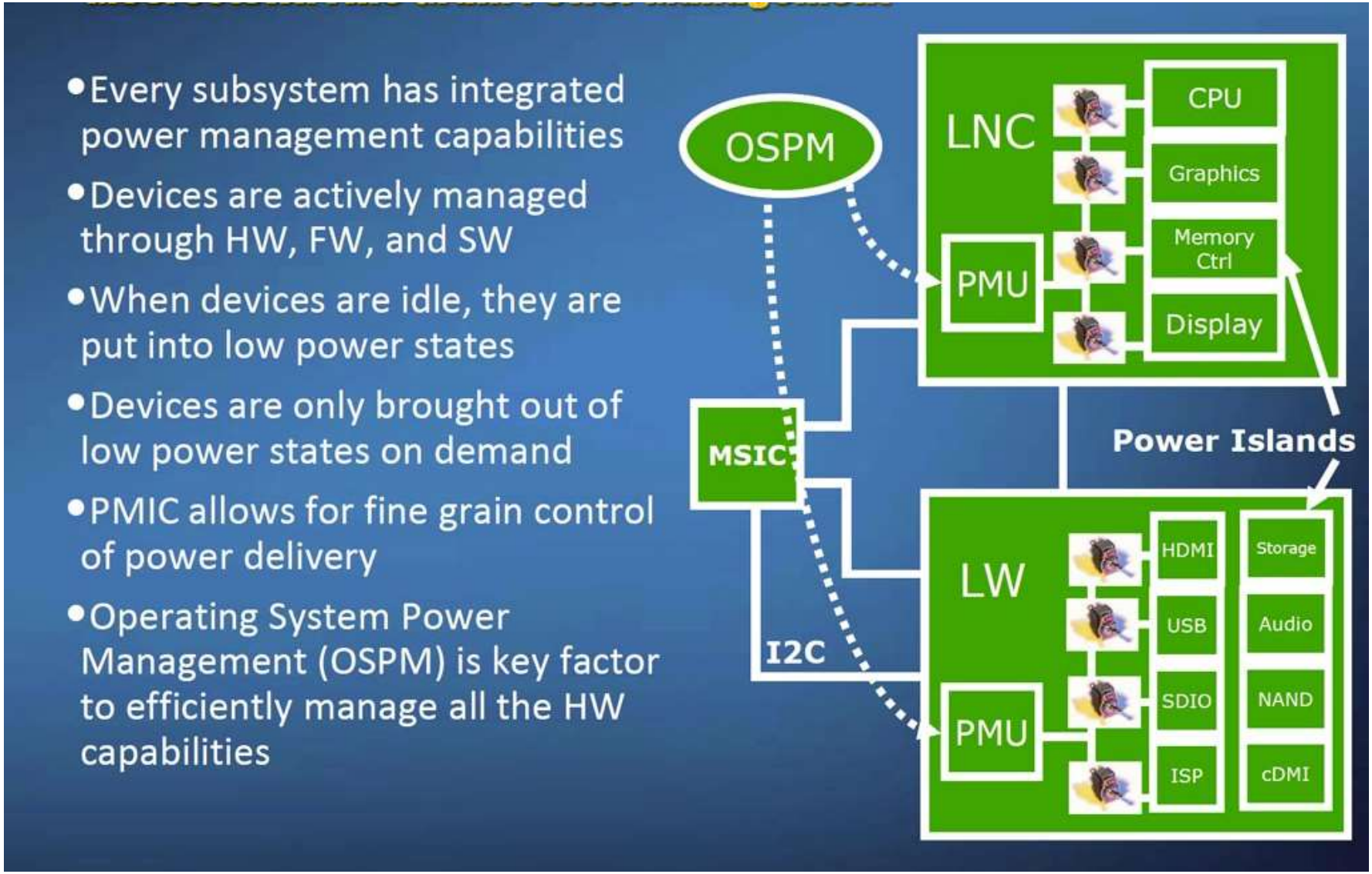
5.2.2 The Moorestown platform (27)

Principle of operation of Moorestown's power management-1 [124]

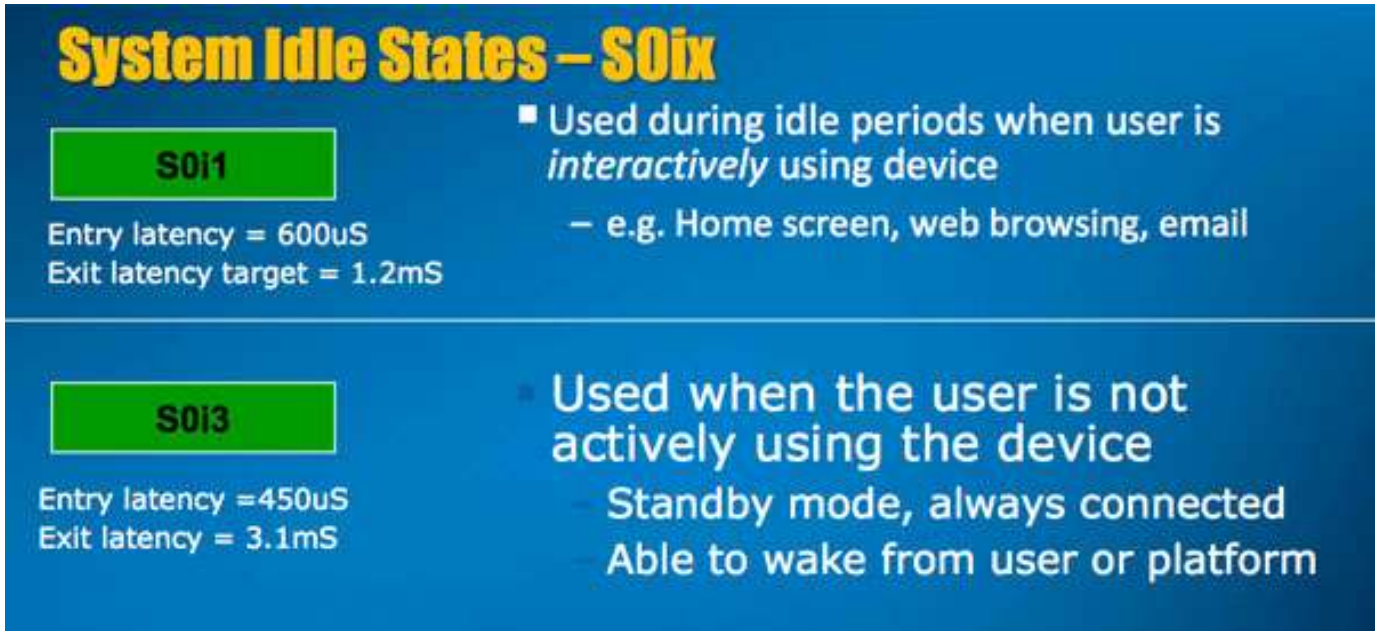


OSPM Directs Entire Platform to Lowest Power State

Principle of operation of Moorestown's power management-2 [124]



b) S0i1/S0i3 system idle states [54]



Idle power reduction of 50x with best in class latency for Always On Always Connected

5.2.2 The Moorestown platform (30)

Unit powering in the S0i1 and S0i3 system idle states [54]

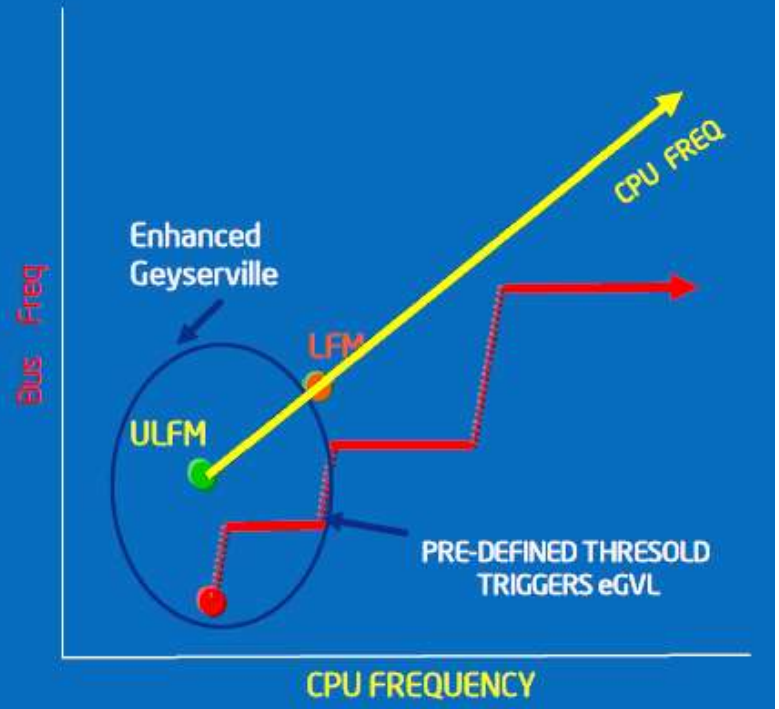
What 's up in S0i1 and S0i3?

Islands (Coalesced)	S0: C0-C6	S0i1	S0i3
C6 SRAM, Wake logic	ON	ON	OFF
DDR	ON/SR	SR	SR
Power Manager	ON	ON	OFF
Gfx	ON/Power-Gated	Power-Gated	OFF
Video Decode	ON/Power-Gated	Power-Gated	OFF
Video Encode	ON/Power-Gated	Power-Gated	OFF
Display Controller	ON/Power-Gated	Power-Gated	OFF
Links to IOH	ON/Power-Gated	Power-Gated	OFF
CPU	C-state dependent	C6	OFF
Display	ON	OFF	OFF

c) Enhanced Geyserville (eGVL) technology [93]

Enhanced Geyserville (eGVL)

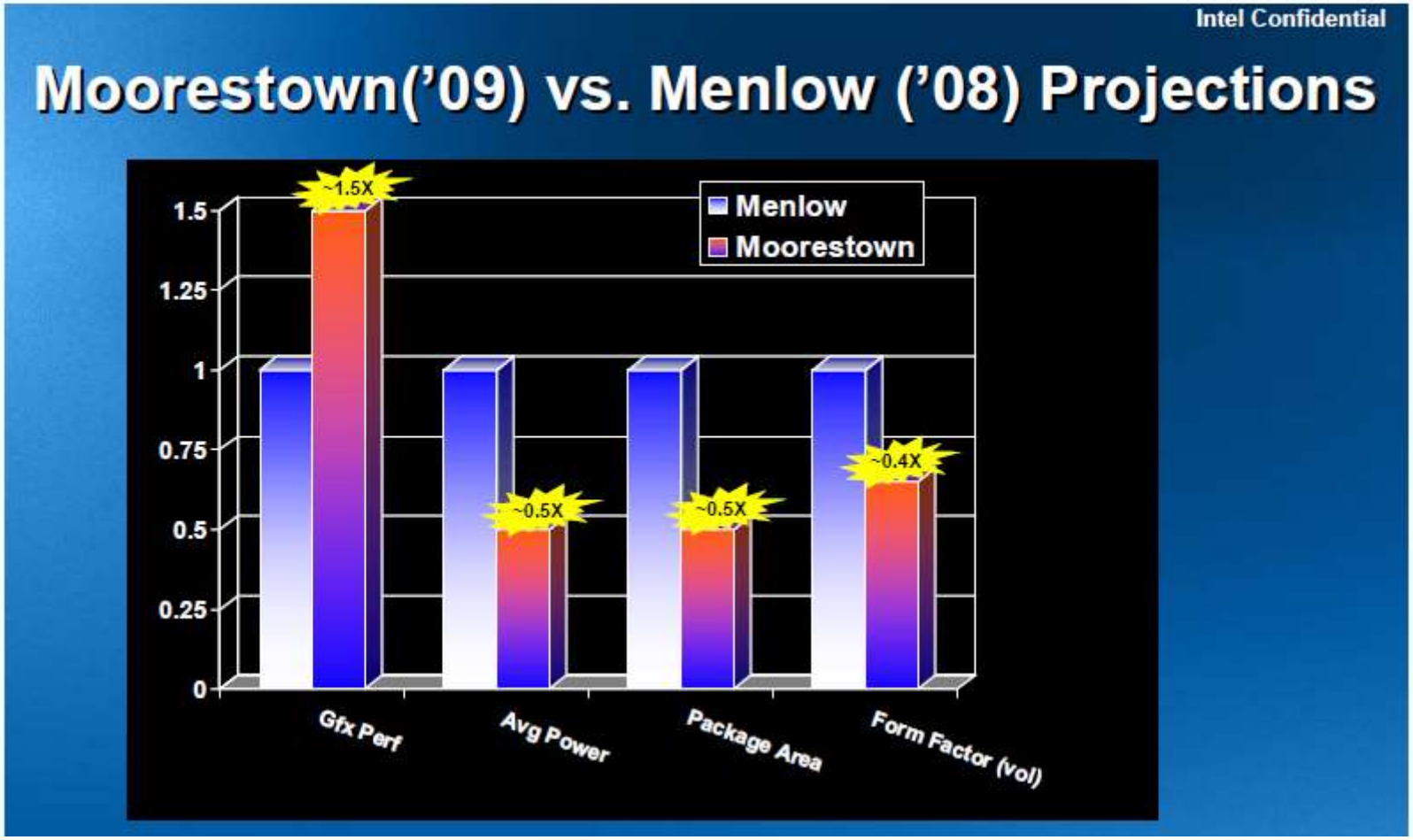
- Motivation
  - To provide lowest possible CPU frequency
  - To enable "As many P-states as possible" below LFM at Vmin
    - Linear savings of average power when CPU is not doing anything useful while in C0 state (cV^2F)
- Implementation
  - Added P-states below LFM at Vmin
  - OS can now request CPU to transition to these new P-states



eGVL mode provides additional range of low power operating point

5.2.2 The Moorestown platform (32)

Projected features of the Moorestown platform vs. the Menlo platform [99]



5.2.3 The Medfield platform

5.2.3 The Medfield platform

- Announced: 9/2009
- First Medfield smartphones: Q2/2012
- Based on the 32 nm Silvermont CPU, it is Intel's first SOC platform for smartphones.
- It targets the Android OS.

5.2.3 The Medfield platform (2)

Target market segment

Medfield targets the mainstream smartphone market space, as indicated below.

*From Intel Roadmap. Based on Smart Phones TAM with >$200 ASP, ** Based on Portable Navigation devices TAM, *** Based on Portable Video and Gaming TAM, **** Based on Tablets, Vertical HHs, and Select Netbooks Data Sources: iSuppli, ABI, IDC, Canalys, Intel analysis*

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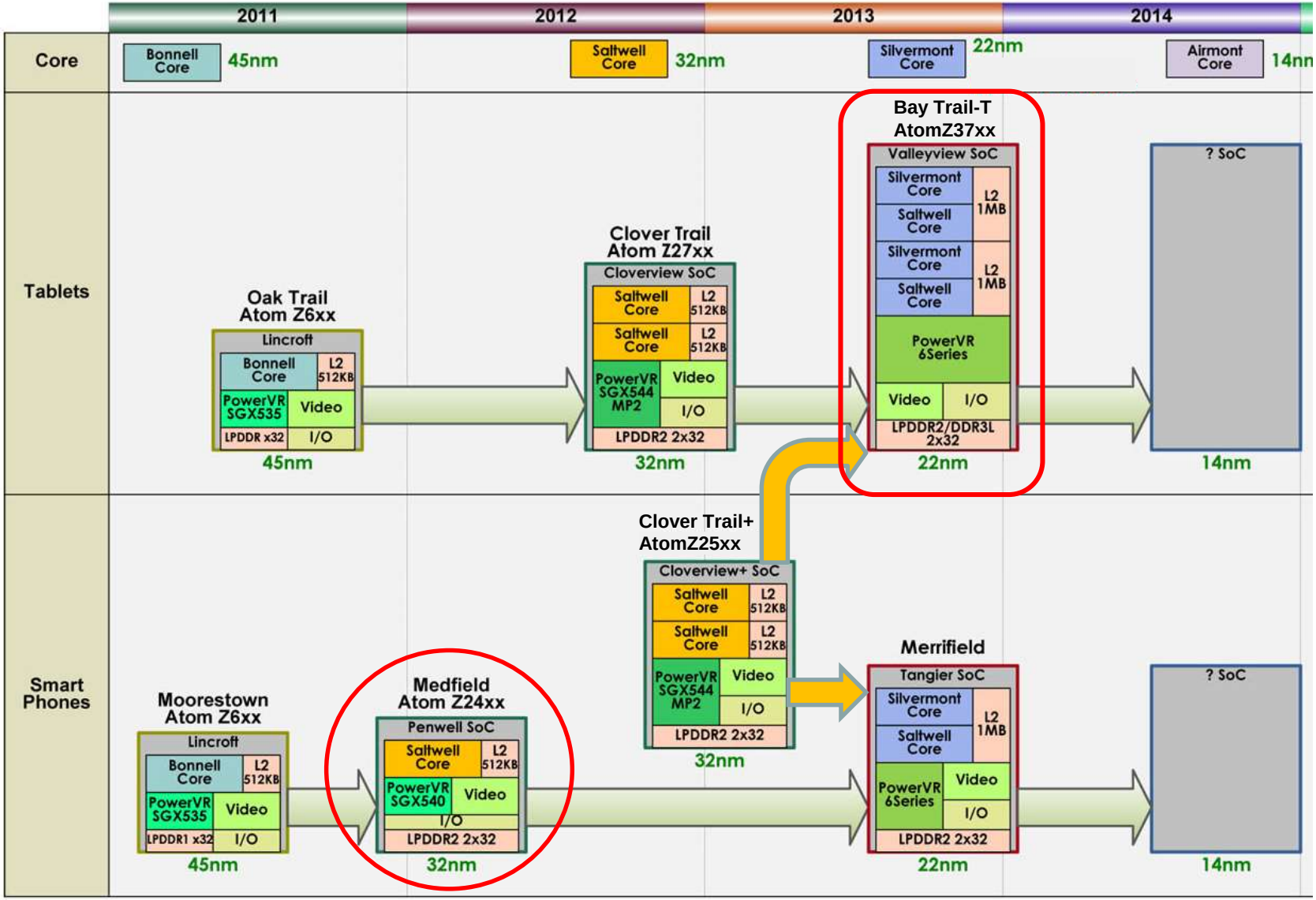
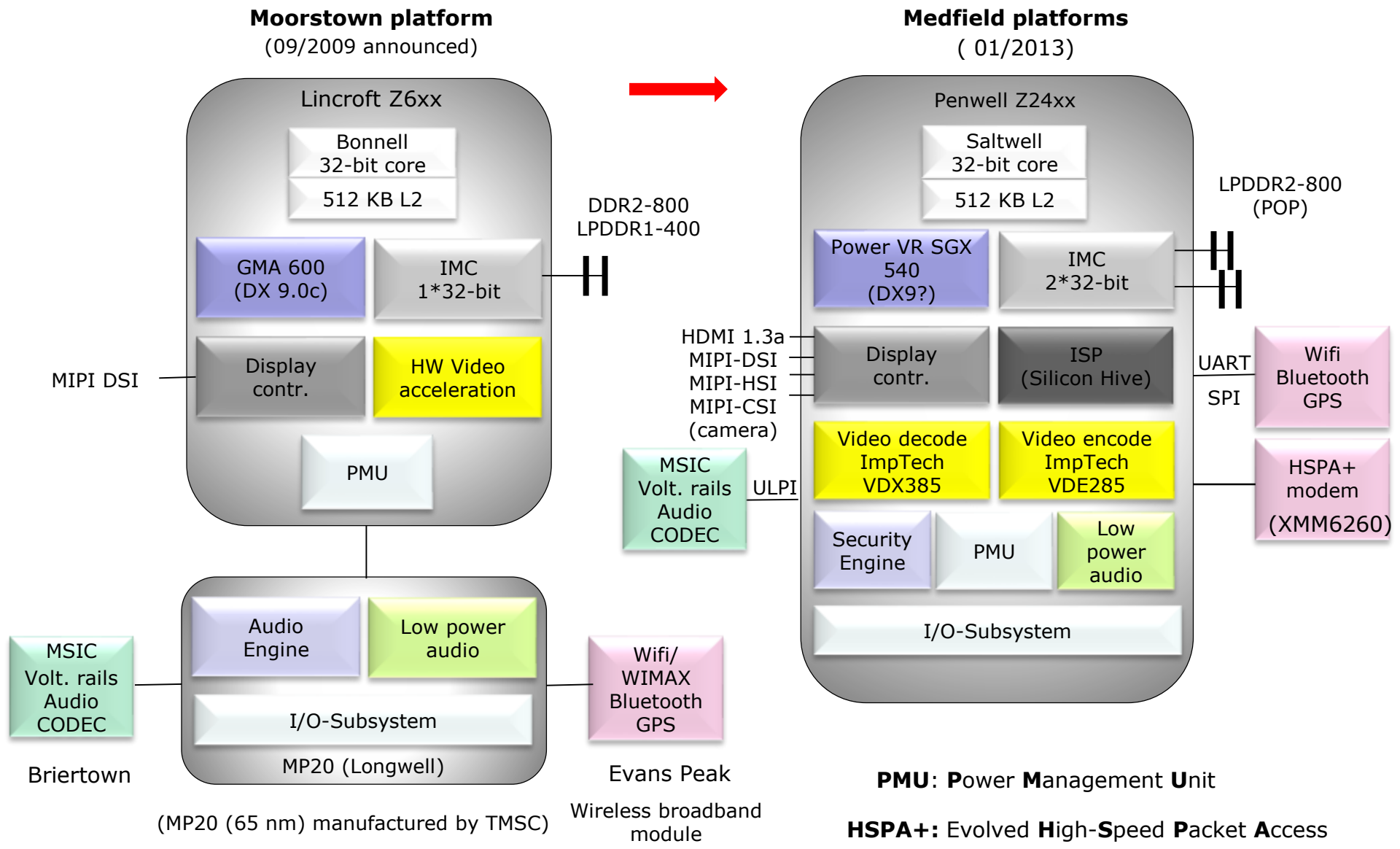
5.2.3 The Medfield platform (3)

Positioning the Medfield smartphone platform in Intel's tablet and smartphone platforms [110]



5.2.3 The Medfield platform (4)

Evolution of the Medfield platform

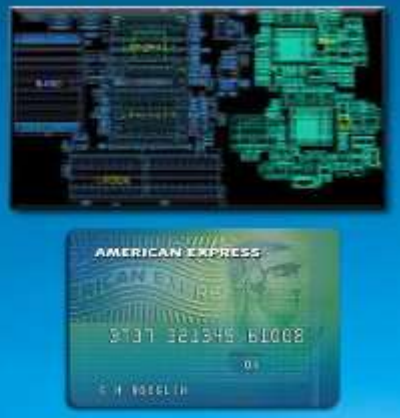


PMU: **P**ower **M**anagement **U**nit

HSPA+: Evolved **H**igh-**S**peed **P**acket **A**ccess

5.2.3 The Medfield platform (5)

Contrasting key features of the Moorestown and the Medfield platforms [58]

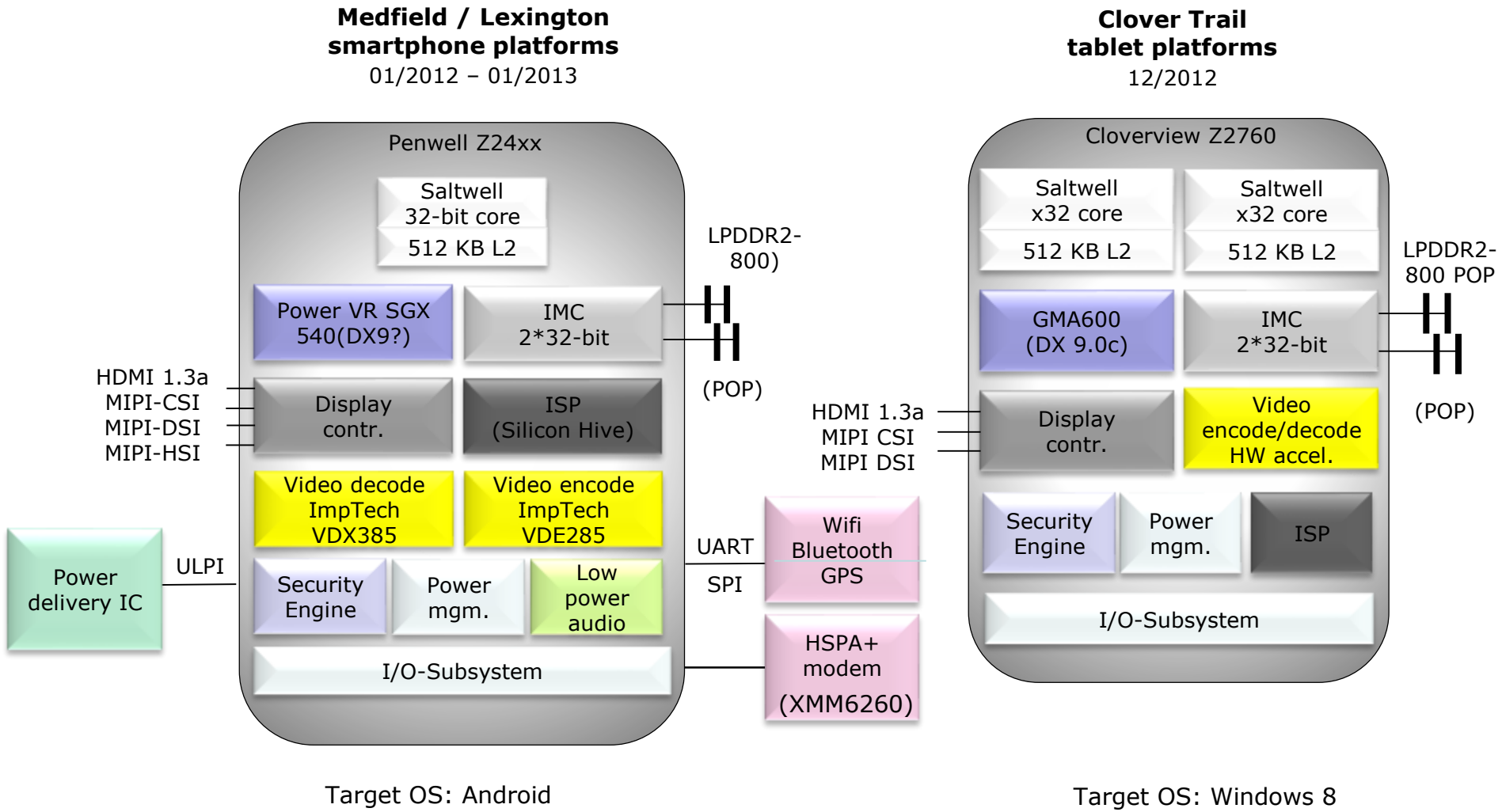
	Moorestown (45nm)	Medfield (32nm)	
			
Board size	5,000mm2	4,150mm2	(↓ 17%)
Standby power	21mW	14mW	(↓ 33%)
Browsing power	1.2W	0.85W	(↓ 29%)
Video	+ 720p encode	+ 1080p encode	
Camera	5 mega-pixel	up to 16 mega-pixel	
Graphics	800 MPPS	2,000 MPPS	(↑ 250%)

MPPS: Mega Pixels per Sec.

5.2.3 The Medfield platform (6)

Remark

Features and architecture of the Penwell processor targeting smartphones under Android is very similar to the Clover View processor targeting Windows 8 tablets, as indicated below.



5.2.3 The Medfield platform (7)

Main features of the Medfield platforms targeting performance oriented smartphones

Platform	Moorestown	Medfield	Clover Trail+	Merrifield	Moorefield
Available	(09/2009 announced)	01/2012	02/2013	02/2014	06/2014
Focus	High end smartphones	Mainstream smartphones	Smartphones	Smartphones	Smartphones
AP processor	Lincroft	Penwell	Cloverview	Tangier	Anniedale
Models	Z6xx	Z2460/Z2480	Z2520-Z2580	Z3460/Z3480	Z3530-Z3590
Technology	45nm	32nm	32nm	22nm	22nm
Die size	65 mm^2				
No. of trans.	140 mtrs				
CPU micro-arch.	Bonnell	Saltwell	Saltwell	Silvermont	Silvermont
32/64-bit	32-bit	32-bit	32-bit	64-bit	64-bit
No. of cores	1	1	2	2	4
HT	HT	HT	HT	no HT	no HT
fc [GHz] (Turbo)	0.9-1.9 GHz	1.2-2.0 GHz	1.2-2.0 GHz	1.6-2.13 GHz	1.33- 2.5 GHz
L2	512 kB	512 kB	2x512 kB	1 MB/2 cores	1 MB/2 cores
Mem. channels	Single 32-bit mem. ch. MC on proc. die	Dual 32-bit mem. ch. MC on proc. die	Dual 32-bit mem. ch. MC on proc. die	2x32-bit mem. ch. MC on proc. die	2x32-bit mem. ch. MC on proc. die
Memory	LPDDR1-400/DDR2-800	LPDDR2-800 POP	LPDDR2-1066 POP	LPDDR3-1066	LPDDR3-1600
GPU	GMA 600 (Power VR SGX 535)	Power VR SGX 540	Power VR SGX 544 MP2	Power VR G6400	Power VR G6430
DX	DX 9.0c	DX 9	DX 9.L3	DX10	DX10
Rear camera res.	5 Mpixel	8 Mpixel	13 Mpixel	13 Mpixel	13 Mpixel
GPU clock	200/400 MHz	400 MHz	300-533 MHz	400/457 MHz	457 MHz
ISP	—	ISP	ISP	ISP	ISP
Security Engine	—	Security Engine	Security Engine	Security Engine	Security Engine
Integr. baseband m.	No, wireless modem	No, XMM 6260	No, XMM 6268/6360/7160	No, XMM 7160/7260	No, XMM 7360
FSB	cDMI (8bit) (400 MT/s per dir.)	—	—	—	—
Proc. TDP	1.3-3.0 W				
Socket	BGA 518	BGA 617	BGA 760	PoP	PoP
Platform Cont. Hub	MP20 (Langwell)	—	—	—	—
OS at launch	Moblin 2.1 MeeGo/Android 2.1	Android 2.3.7/ 4.1.0	Android 4.2	Android 4.4.2	Android 4.4.2
Smartphone eExamples	Aava Virta Android LG GW990 both withdrawn	Lava Xolo X900 Lenovo K800 Motorola RAZRi Orange San Diego ZTE Grand X IN	Lenovo K900 ZTE Geek/ Grand X2 IN	Dell Venue 7 Dell Venue 8	Asus Fonepad 7 Asus Fonepad 8 Nokia N1, Dell Venue 8 7000,

5.2.3 The Medfield platform (8)

Key features of the Medfield platform to be discussed

a) Introducing Burst Technology to increase performance

b) Introduction of the S0i1/S0i3 Ultra low power system states

c) Stacked (Package-on-Package (PoP)) LPDDR2 memory

d) HSPA+ 3G wireless broadband modem (XMM6220)

5.2.3 The Medfield platform (9)

a) Introducing Burst Technology to increase performance [111], [112]

- The Burst Technology of the Saltwell-based Medfield platform is very similar to the Burst Technology introduced in the Saltwell-based Clover Trail tablet platform and provides about the same benefits as Intel's Turbo Boost technology found in x86-based processors, introduced in the Nehalem family.
- It allows the CPU core to run at higher clock speed than limited by the TDP (Thermal Design Power) of the chip for short periods of time if
  - there is a thermal headroom,
  - the OS requests higher performance and
  - specified temperature limits (Tjmax (junction temperature) and Tskin (the temperature of the case, like the case of a tablet)

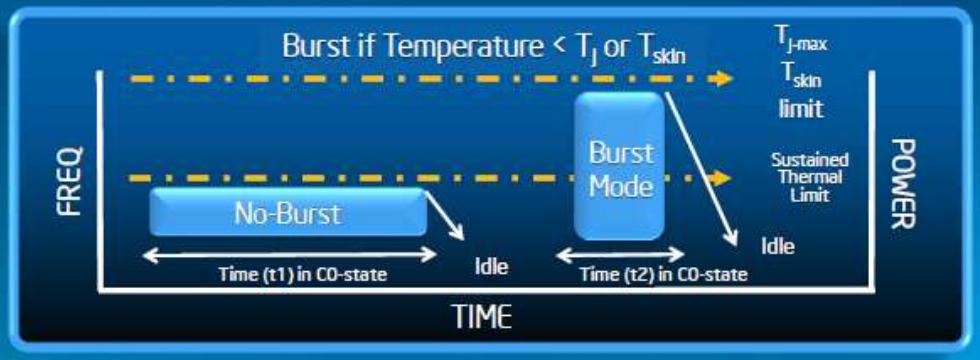
  will not be exceeded.
- The intended operating mode is to allow the processor to wake up from an idle state, perform the work to be done and return to the idle state as quickly as possible, as indicated in the next Figure.

5.2.3 The Medfield platform (10)

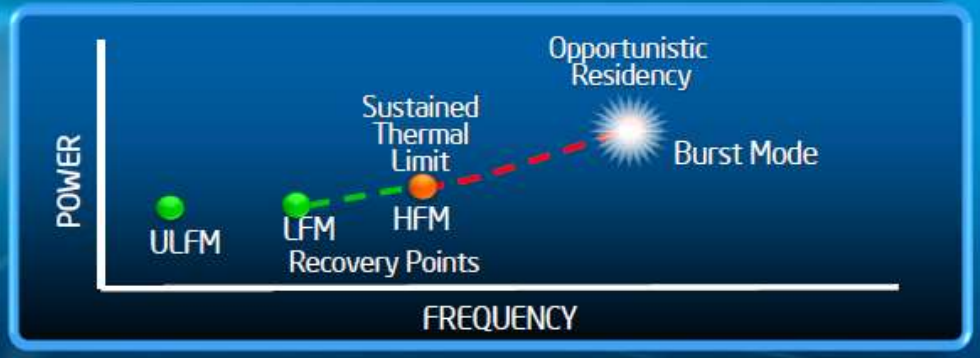
b) Use of Burst technology to increase performance [58]

Intel® Burst Performance Technology

- Takes advantage of thermal headroom (up to $T_{j\text{-}max}$ or T_{skin}) to deliver highest frequencies



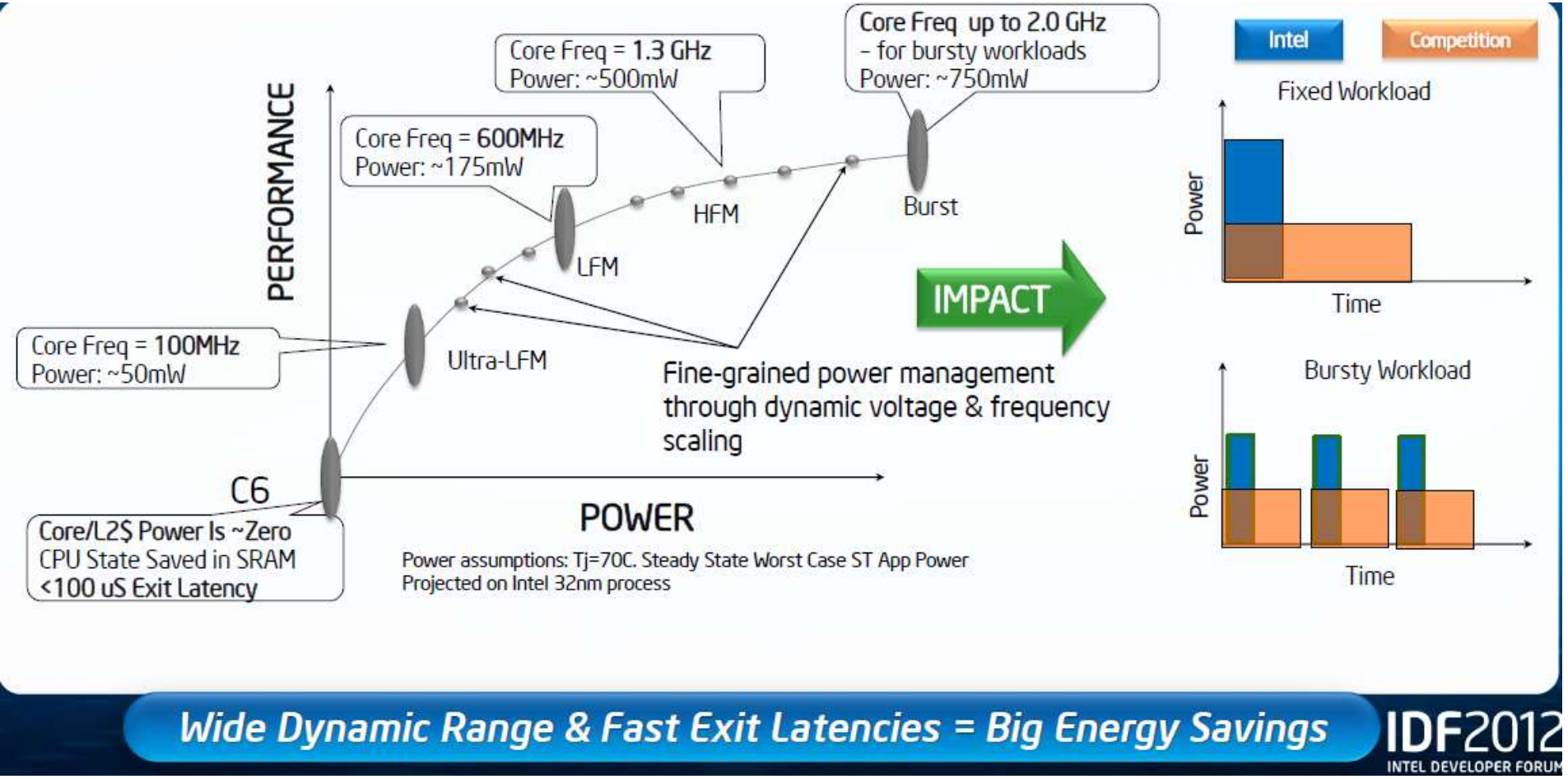
- Races to Idle once "burst mode" performance is not needed



"Performance On-Demand" without Impacting Thermal Design

5.2.3 The Medfield platform (11)

The wide core frequency – power consumption range of the Penwell processor [58]



5.2.3 The Medfield platform (12)

Power consumption of the Medfield CPU at different clock frequencies [58]

Medfield CPU Frequency vs. Power

	100MHz	600MHz	1.3GHz	2.0GHz	
SoC Power consumption	~50 mW	~175 mW	~500 mW	~750 mW	

5.2.3 The Medfield platform (13)

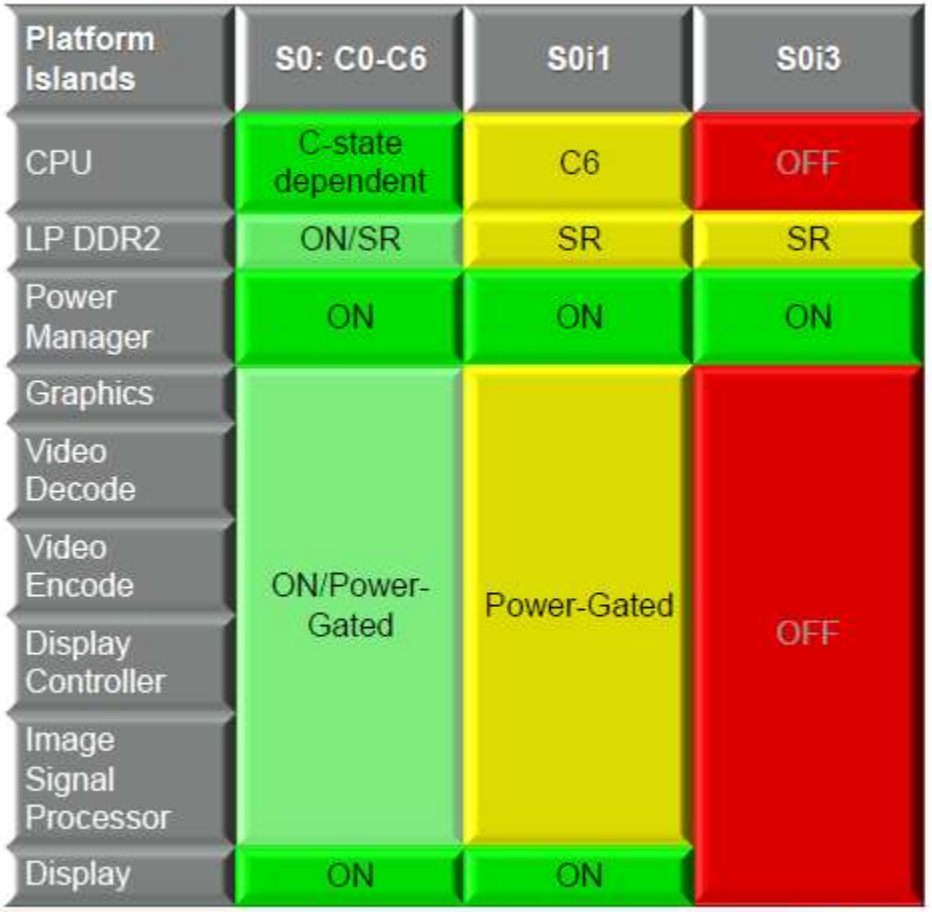
c) Introduction of the S0i1/S0i3 Ultra low power system states [126]

S0i1

- Used during idle (e.g. home screen, web browsing)
- Ultra Low Power: mW
- Entry-Exit Latency: µs

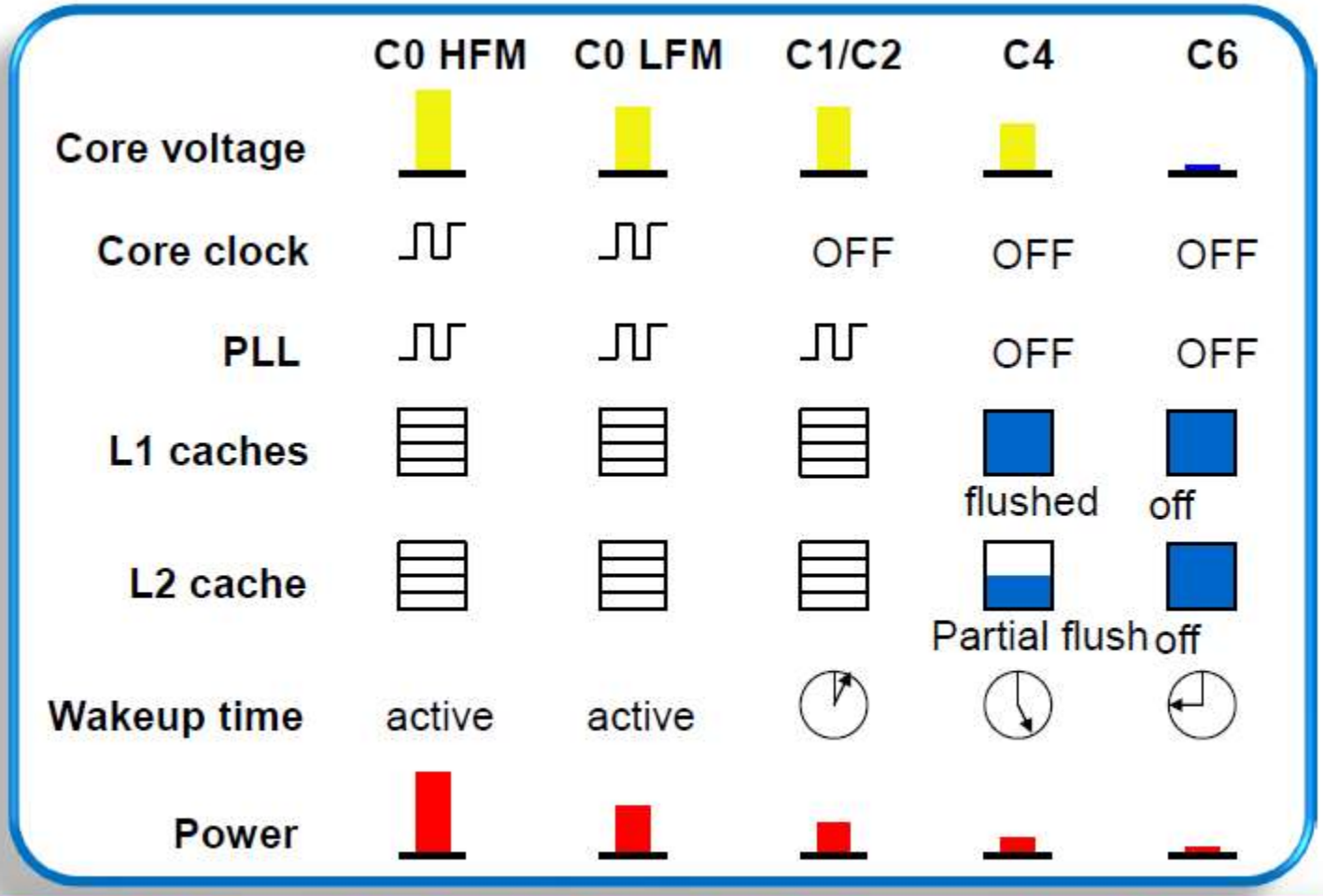
S0i3 / S3

- Used when NOT interacting with the device (e.g. standby mode)
- SoC power: µW
- Entry-Exit Latency: ms



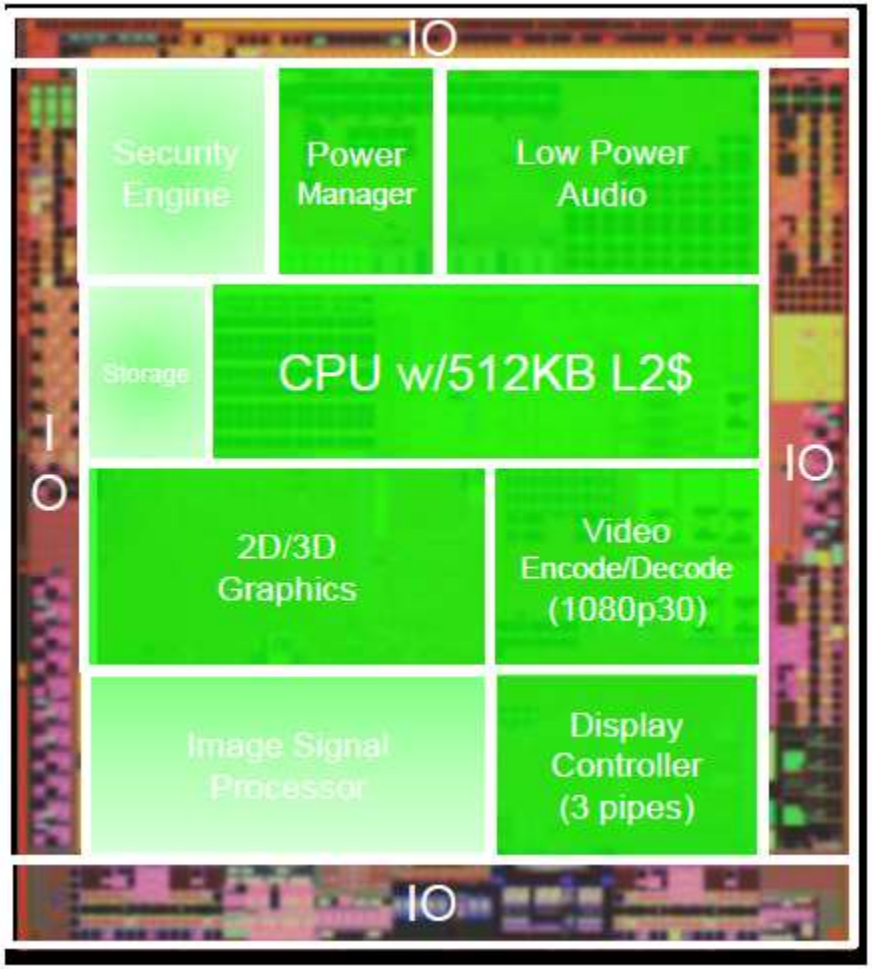
Achieves Ultra Low Power States with Best-in-Class Latency

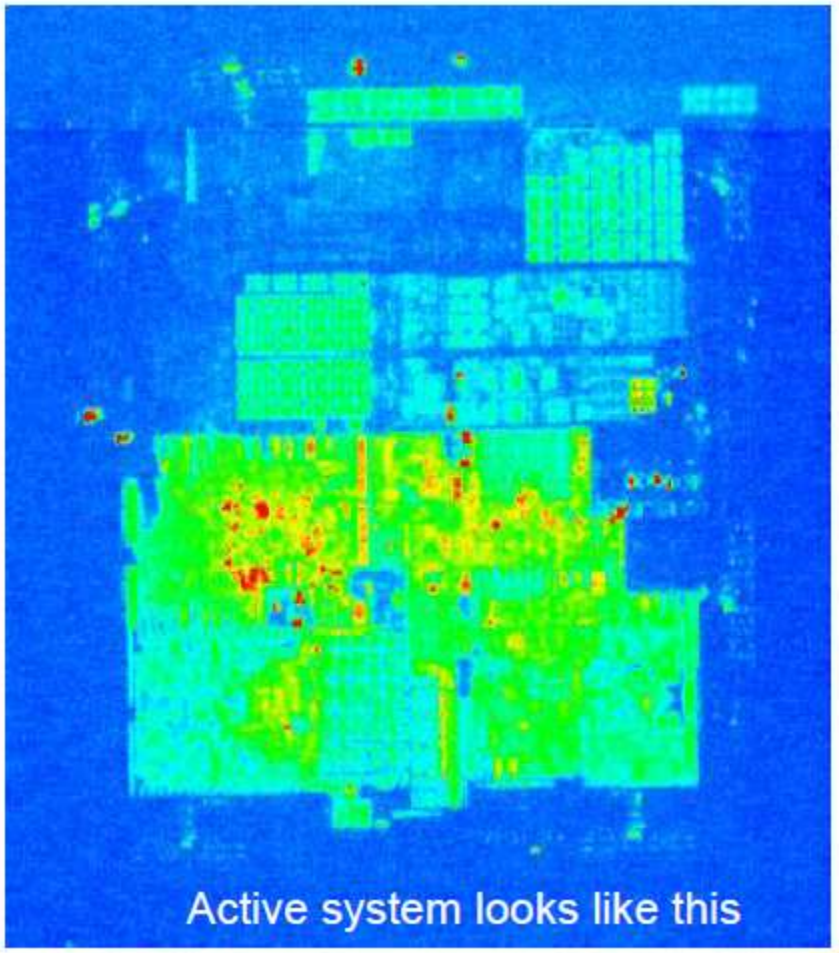
The C-states of Medfield [126]



5.2.3 The Medfield platform (15)

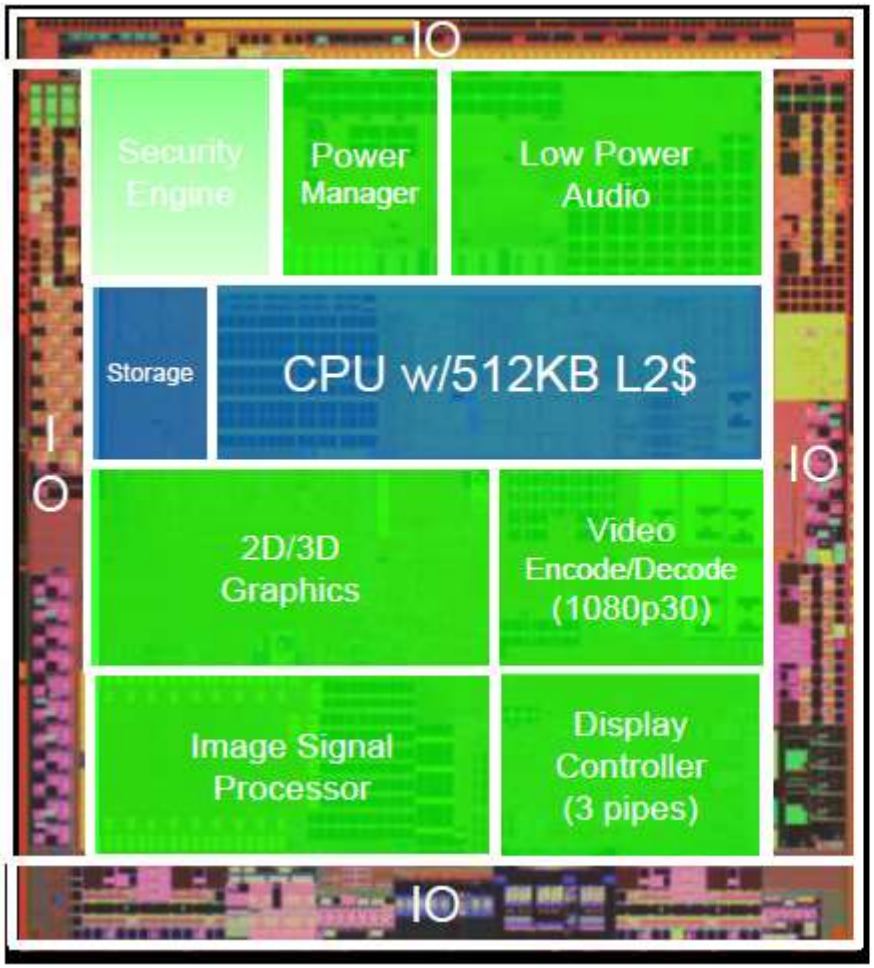
Infrared emission (IREM) image of the Penwell die when the CPU is active [126]

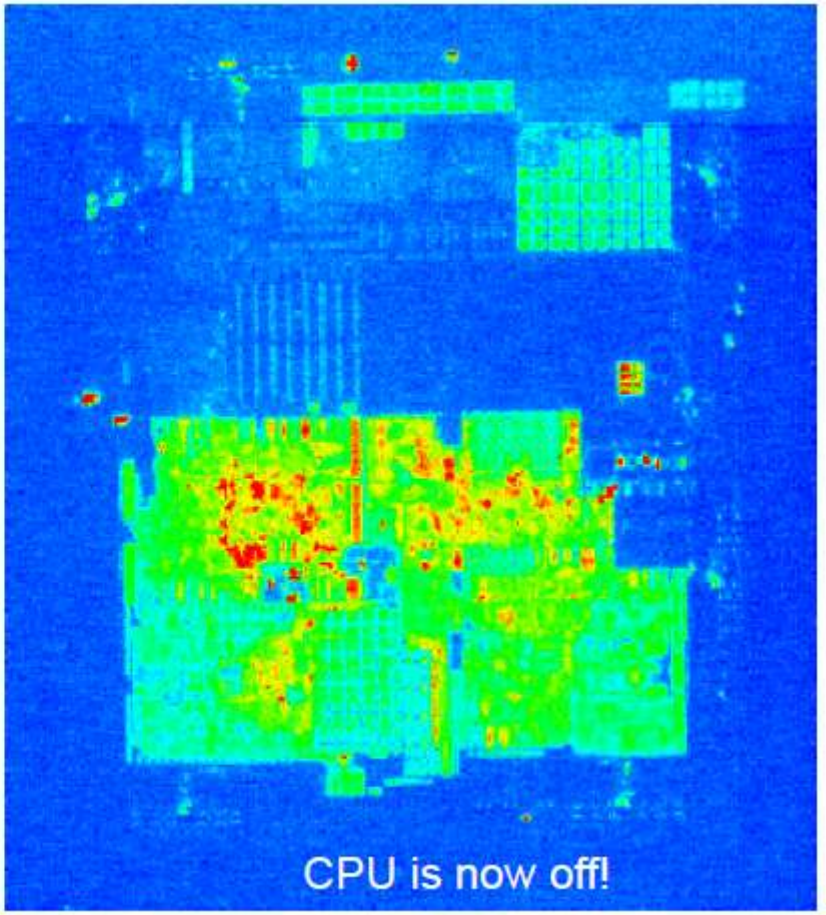




5.2.3 The Medfield platform (16)

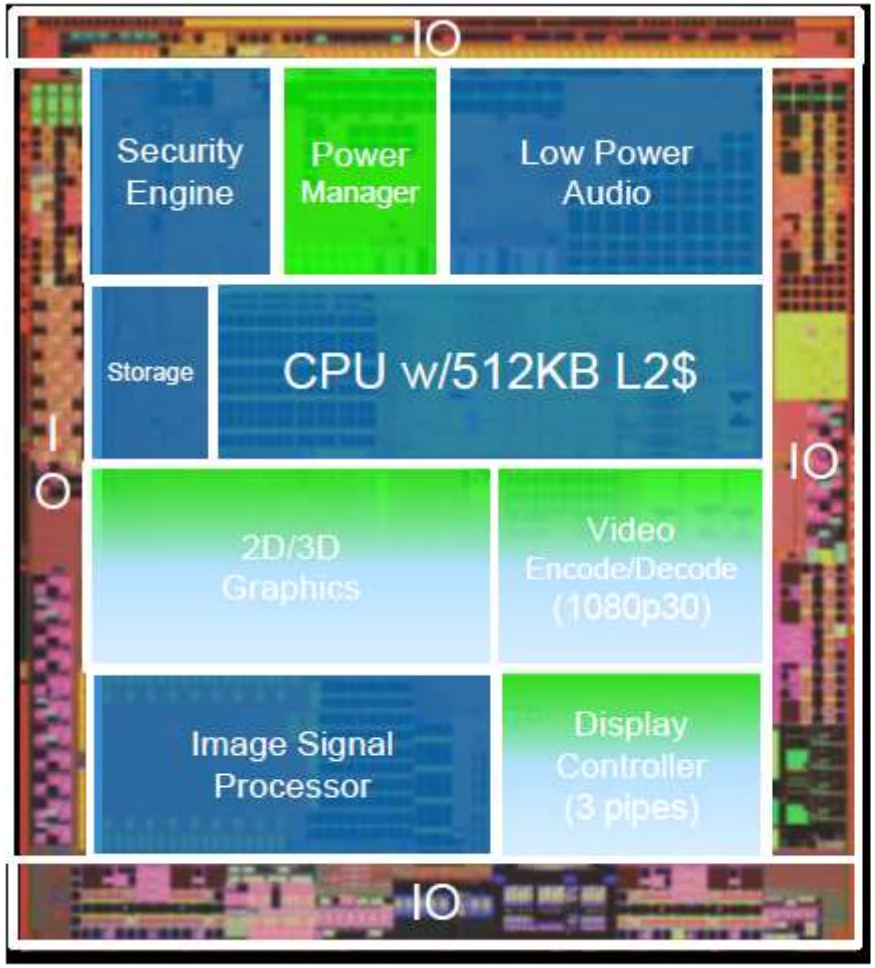
Infrared emission (IREM) image of the Penwell die when the CPU is off [126]

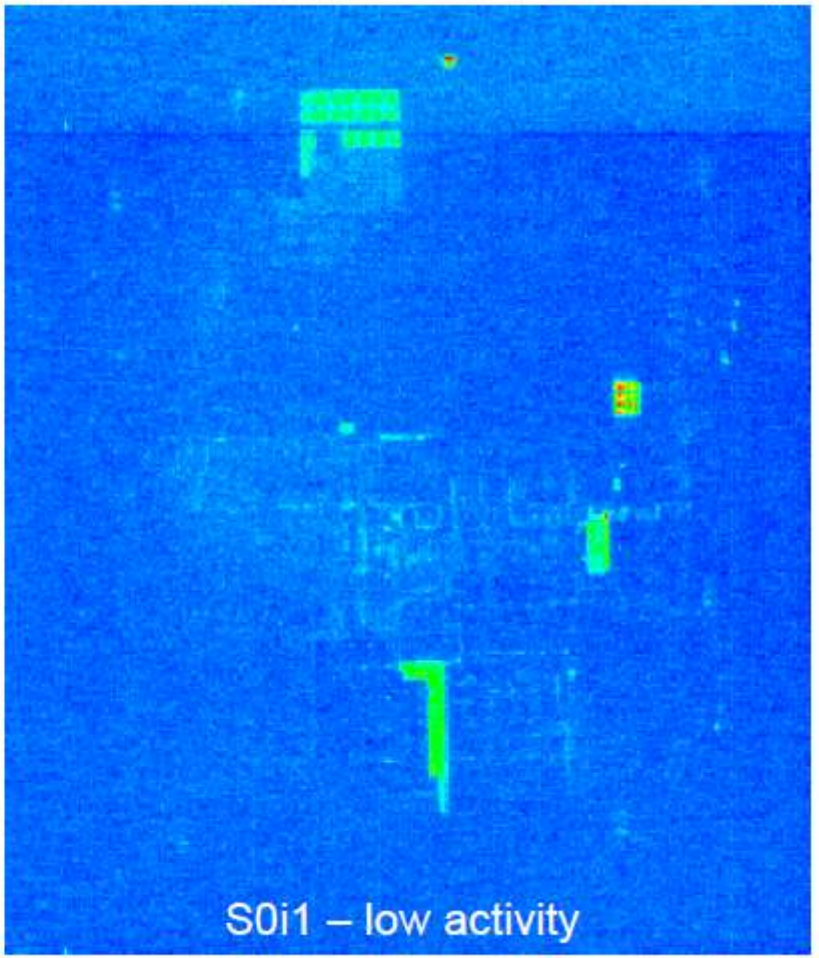




5.2.3 The Medfield platform (17)

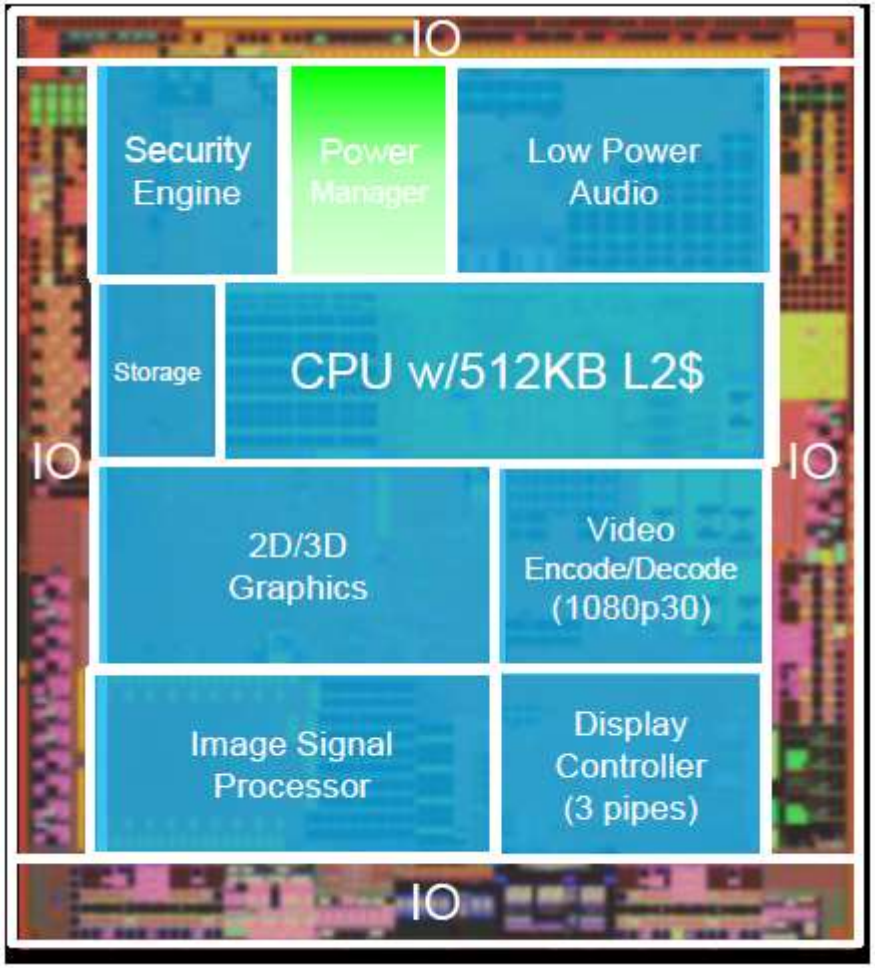
Infrared emission (IREM) image of the Penwell die when it is in the S0i1 system state [126]

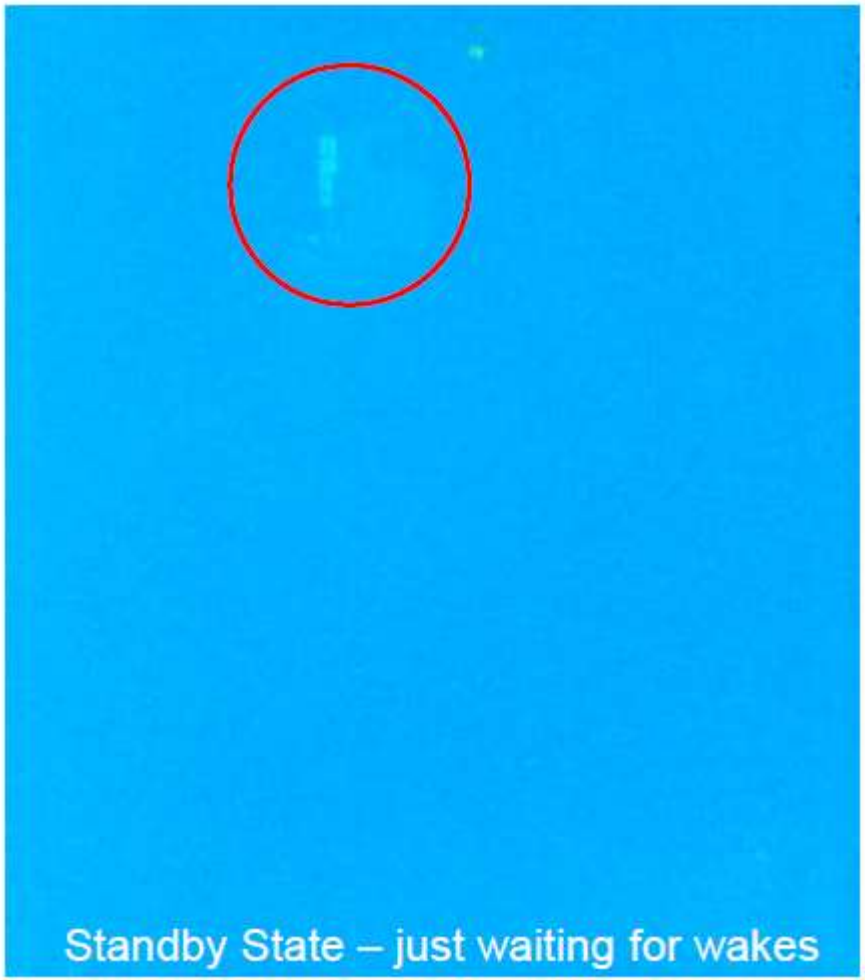




5.2.3 The Medfield platform (18)

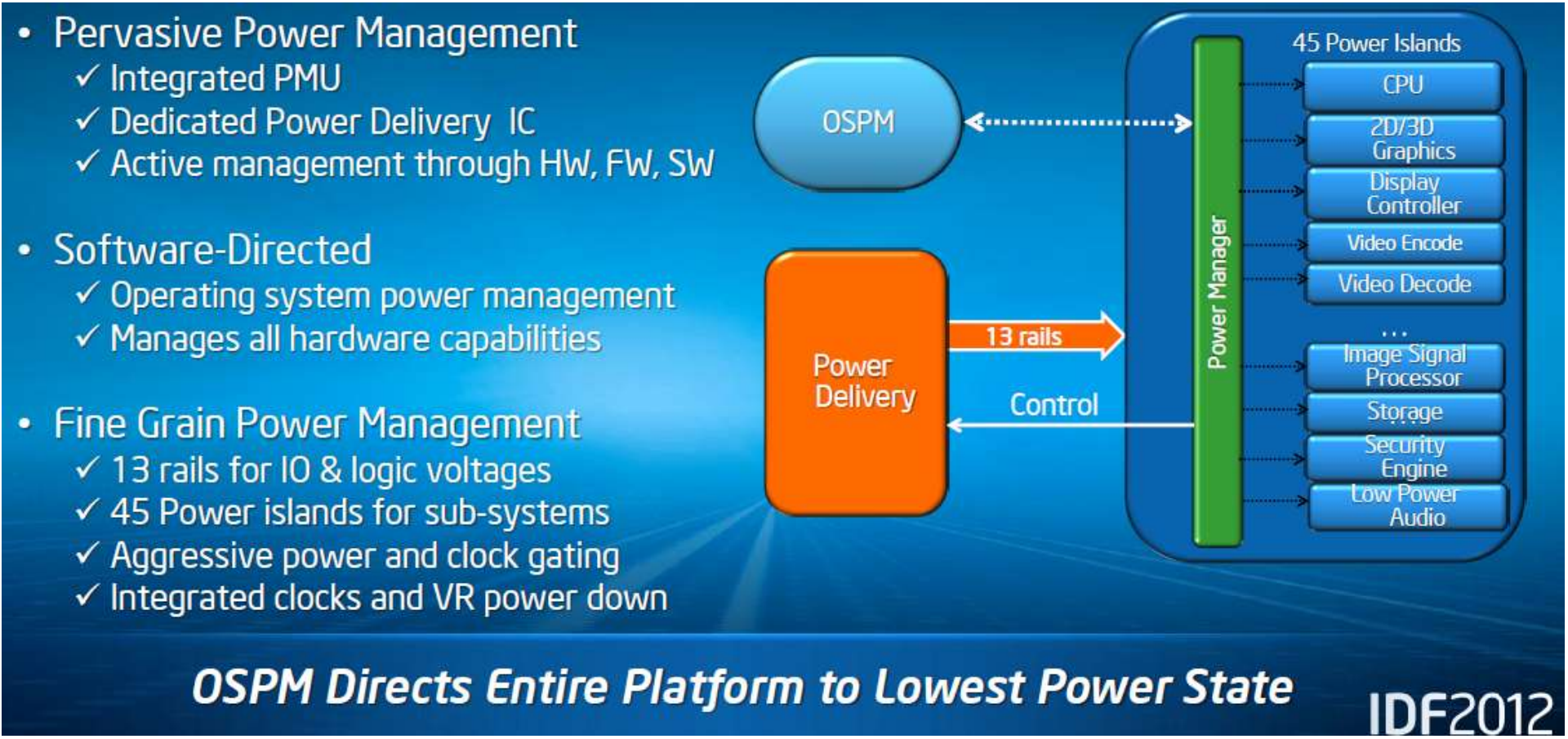
Infrared emission (IREM) image of the Penwell die when it is in the S0i3 system state [126]





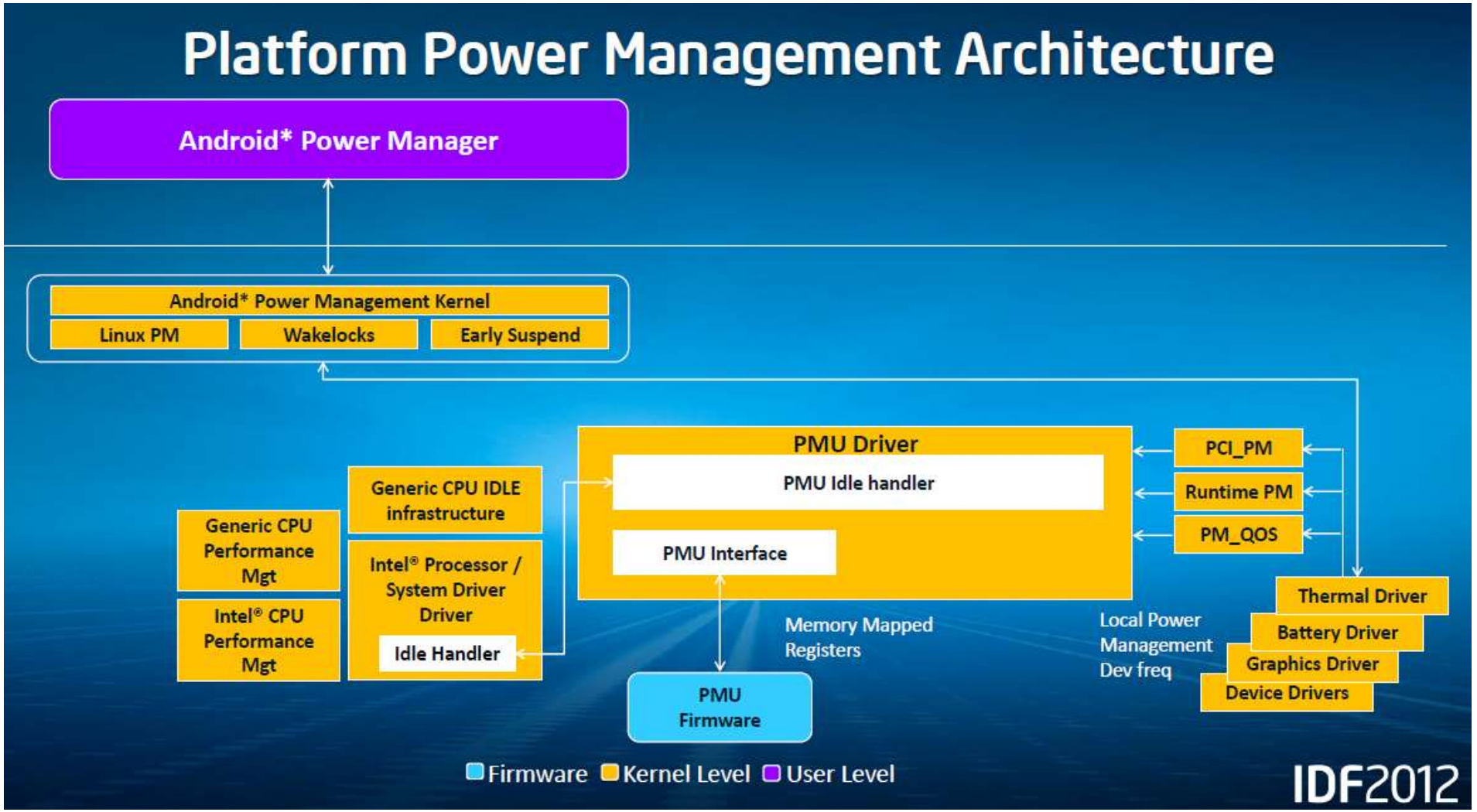
5.2.3 The Medfield platform (19)

The OS power management of the Medfield platform [58]



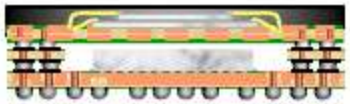
5.2.3 The Medfield platform (20)

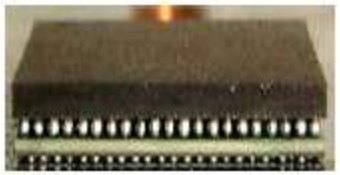
The platform power management architecture of Medfield [58]



5.2.3 The Medfield platform (21)

d) Stacked (Package-on-Package (PoP)) LPDDR2 memory [126]





Package-on-Package (POP)
- 12 x 12 mm PoP FCMB4 – 32nm
- Non PoP SoC < 0.8 mm
- PoP z height < 1.4mm
- OEM/ODM can solder up to 2 GB of LPDDR2 memory on top of SOC

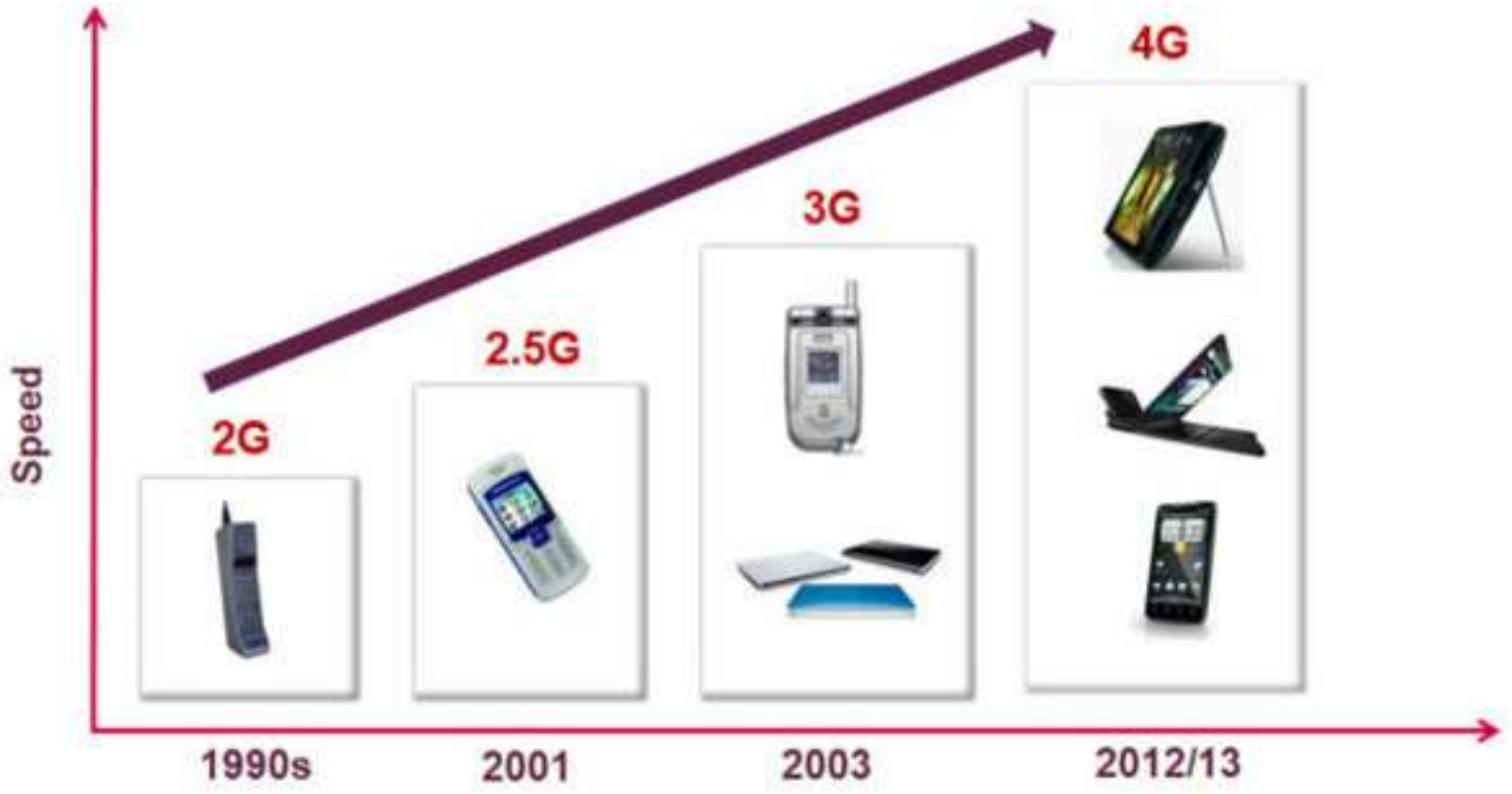
- **Memory Peak Bandwidth**
  - ✓ 6.4GB/s @ 800MT/s
  - ✓ Channels and ranks
- **Dual 32 bit channels**
  - ✓ Supports 1 or 2 ranks per channel
- **Memory Size and Density**
  - ✓ Supports total memory size of 128MB, 256MB, 512MB and 1GB per channel
  - ✓ Supports 1Gb, 2Gb and 4Gb chip densities
- **Other Features**
  - ✓ Aggressive power management to reduce power consumption
  - ✓ Proactive page closing policies to close unused pages
  - ✓ Supports different physical mappings of bank addresses to optimize for performance

5.2.3 The Medfield platform (22)

e) HSPA+ 3G wireless broadband modem (XMM6220)

Brief introduction to wireless broadband standards

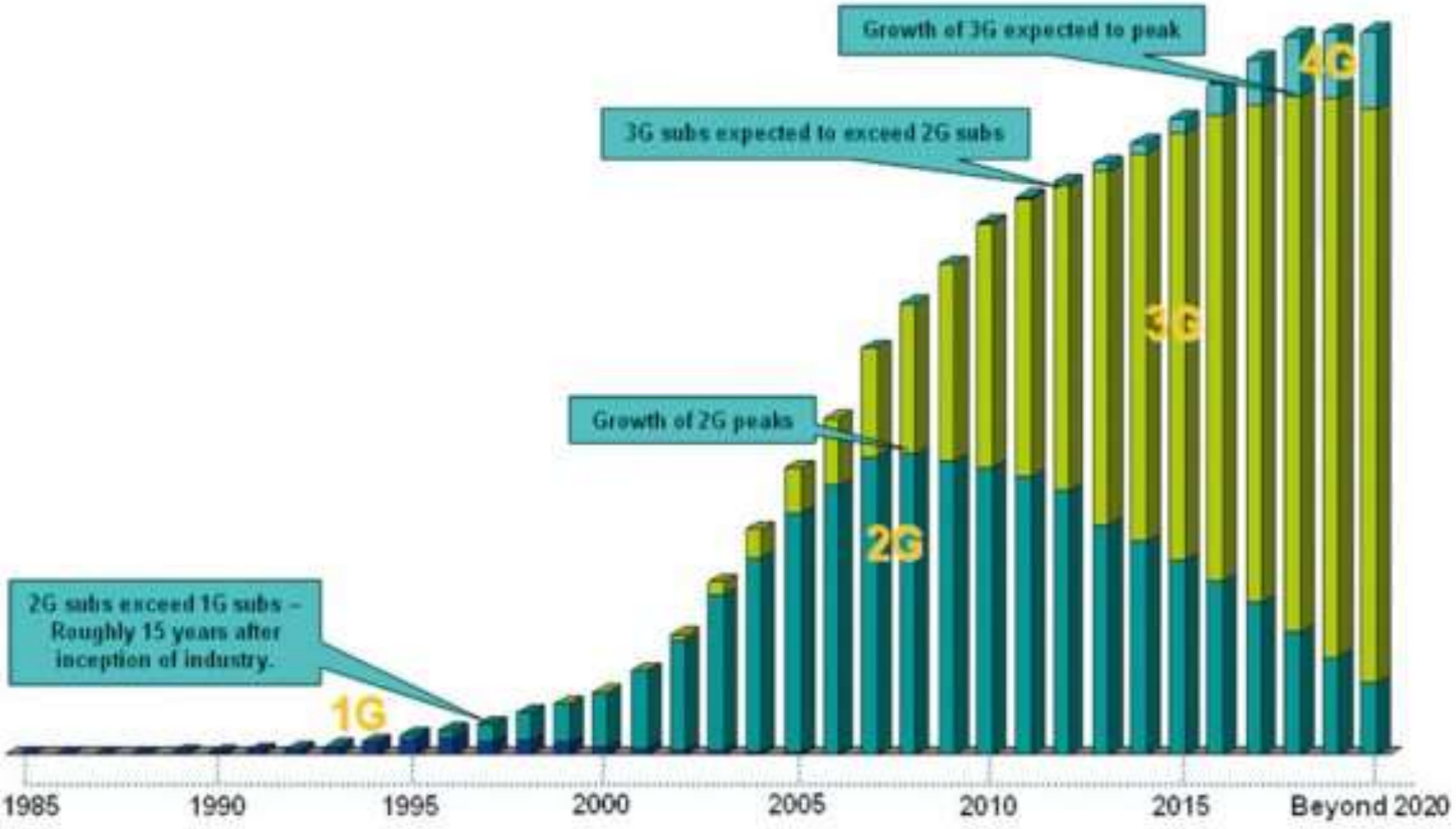
Subsequent generations [127]



Courtesy of Ofcom

5.2.3 The Medfield platform (24)

Use of subsequent generations of wireless broadband standards [127]



Source: CDG subs: subscribers

5.2.3 The Medfield platform (25)

3G wireless broadband standards – the HSPA standard

- HSPA (High-Speed Packet Access) is a 3GPP standard for wireless broadband communication defined by the 3GPP Organization (3rd Generation Partnership Project, established in 2008).
- 3GPP unites six telecommunications standard development organizations and provides 3GPP standards, such as HSPA or LTE.

  HSPA is the most widely deployed 3G broadband standard, in 10/2012 about 500 HSPA commercial networks were is use in more than 180 countries.
- Subsequent releases of HSPA (see the next Figure) support already HSPA+ with increasingly higher speeds, thus for commercial purposes HSPA+ is often branded as being a 3.5G or even a 4G standard.

The evolution of HSPA

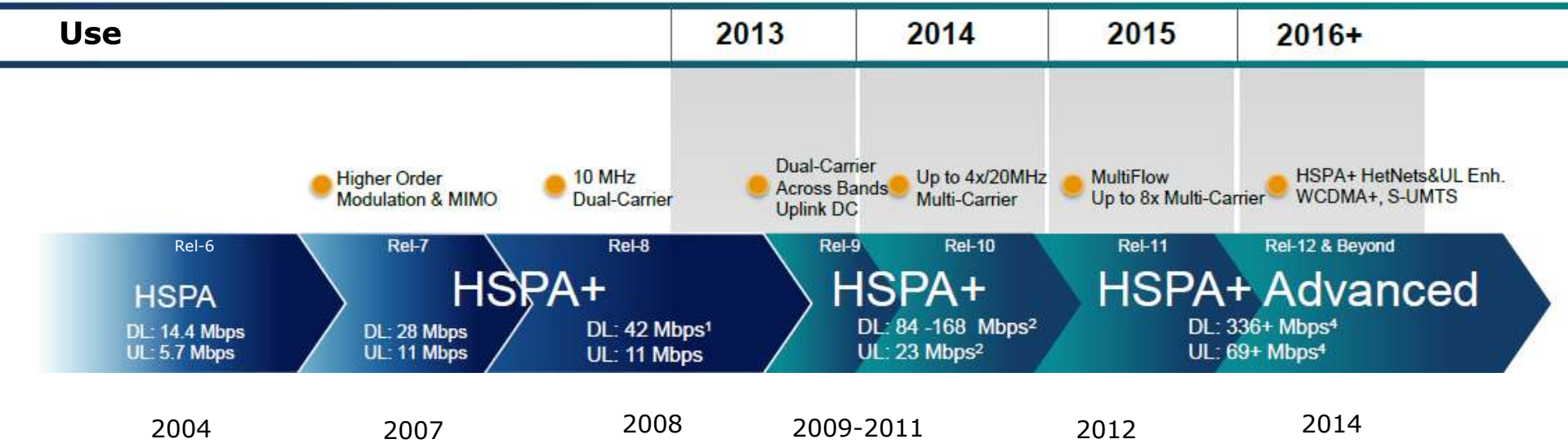


Figure: Peak download (DL) and upload (UL) speeds of subsequent HSPA releases [128]

5.2.3 The Medfield platform (26)

Peak speed requirements of 4G services [129]

The 4G specifications, termed as the International Mobile Telecommunications Advanced (IMT-Advanced) specifications include the following peak speed requirements (2008):

- For low mobility communication (such as from pedestrians and stationary users): 1 Gb/s
- For high mobility communication (such as from trains and cars): 100 Mb/s

4G wireless broadband standards

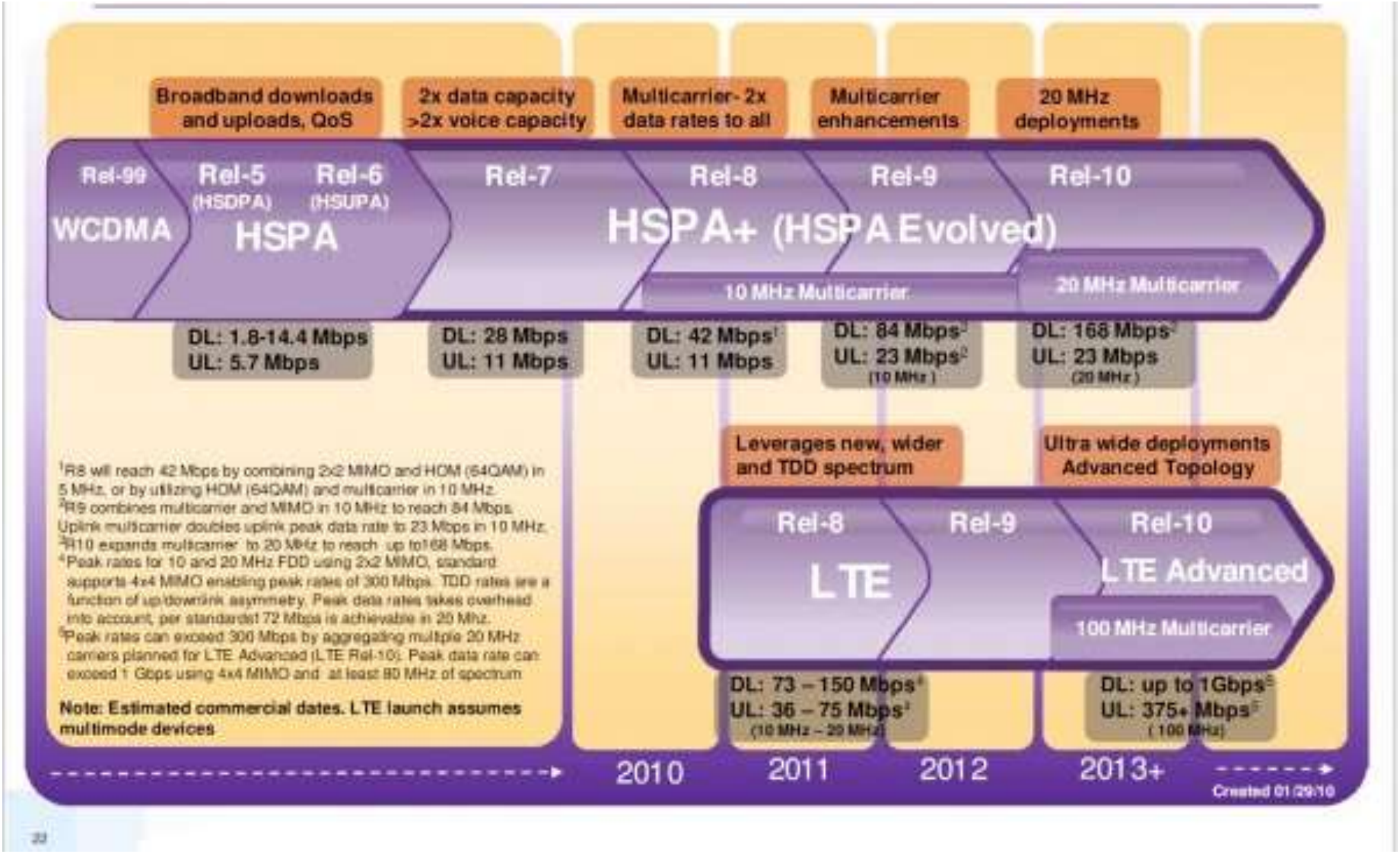
- Mobile WiMAX (Worldwide Interoperability for Microwave Access)

  It was originally the IEEE 802.16m-2011 wireless broadband standard that has been commercialized under the designation WiMAX by the WiMAX Forum industry alliance).
- LTE or 4G LTE (Long Term Evolution)

  It is a 3GPP (3rd Generation Partnership Project) standard published first as the Release 7 document series.
- Although the first releases of the Mobile WiMAX and LTE standards do not comply with the IMT-Advanced peak speed requirement of 1 Gb they are typically branded as 4G services as they can be considered as forerunners of IMT-compliant versions of 4G wireless broadband standards.

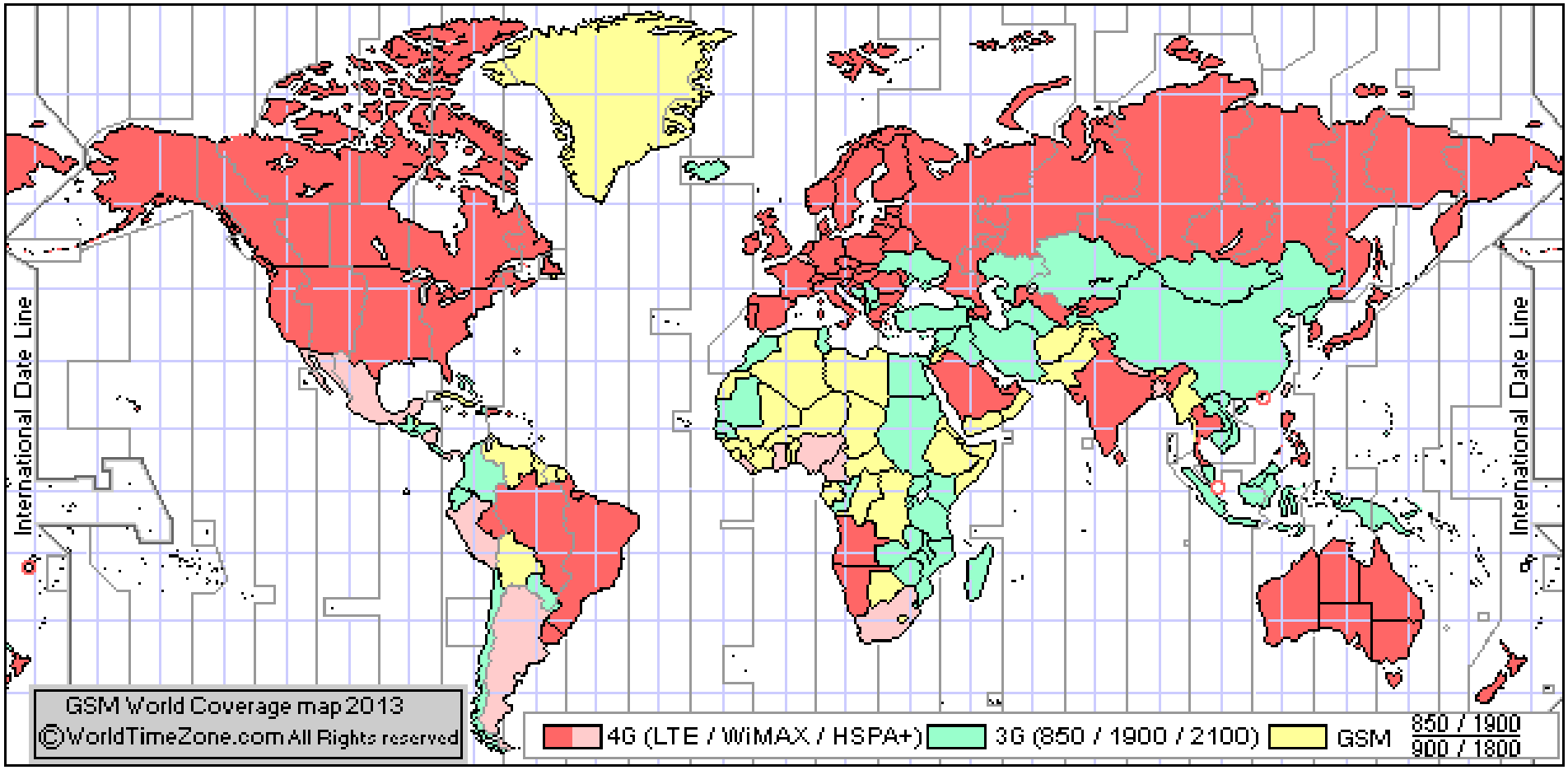
5.2.3 The Medfield platform (27)

LTE as a parallel evolution path to HSPA [127]



5.2.3 The Medfield platform (28)

World coverage of wireless broadband standards [130]



In many countries, LTE, WiMAX, HSPA+, 3G UMTS, GSM networks coexist.

5.2.3 The Medfield platform (29)

Evolution of using wireless broadband standards [127]

Market impact	2003	2006	2009	2010	2016
Peak rate	384 kbps	7 Mbps	42 Mbps	~150 Mbps	~1 Gbps
Typical user rate downlink	~200 kbps	1–2 Mbps	2–10 Mbps	10–20 Mbps	~30–100 Mbps
Typical user rate uplink	64 kbps	64–884 Mbps	0.5–4.5 Mbps	5–10 Mbps	~10–60 Mbps

Wifi for supporting hot spot coverage

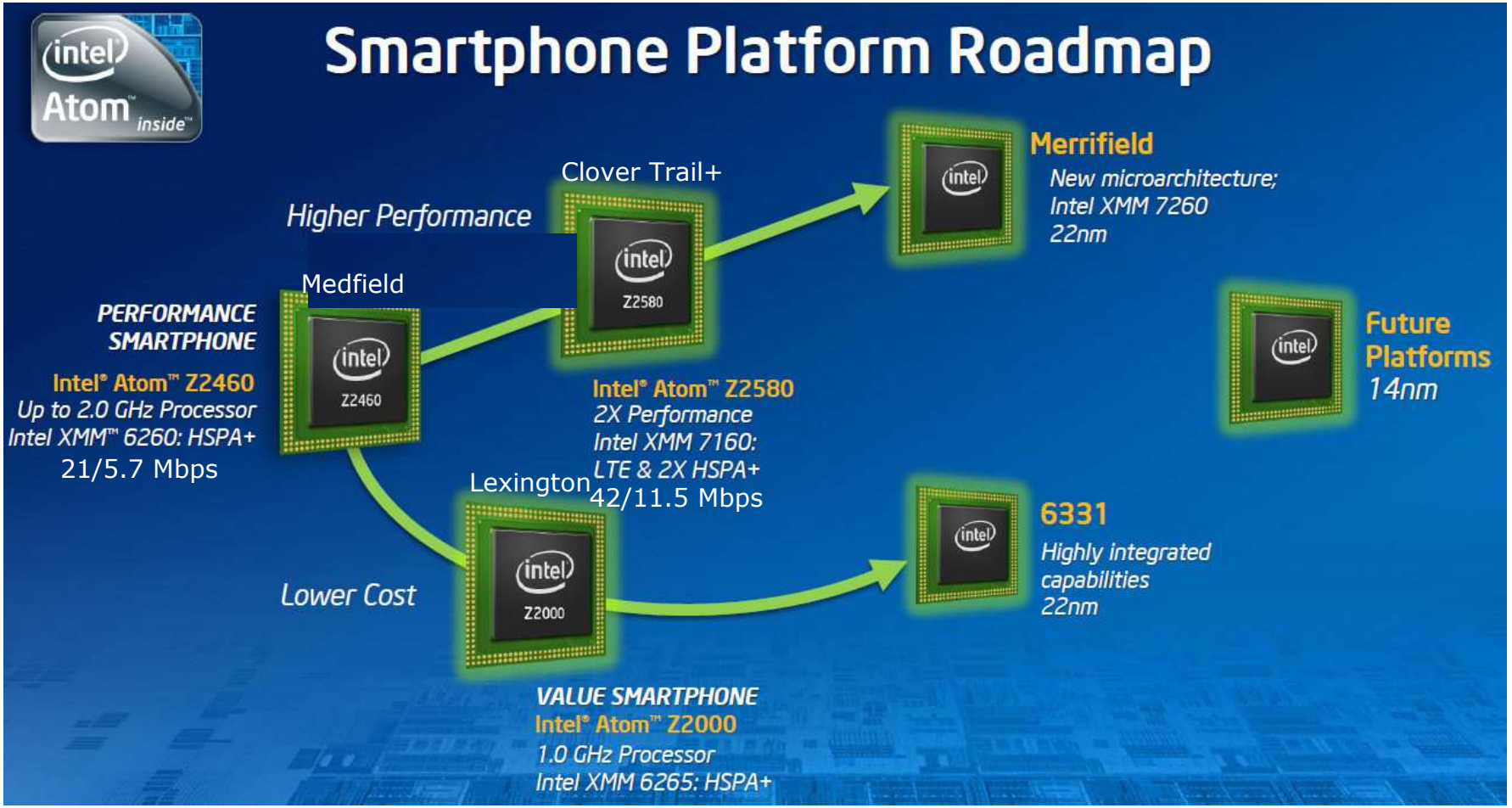
5.2.3 The Medfield platform (30)

Support of Intel's smartphone platforms by wireless broadband connection

- Intel's first smartphone platform with wireless broadband connection was the Medfield platform.
- It was equipped with the XMM 6260 3G broadband modem.
- The XMM 6260 was originally designed by the German firm Infineon Technologies AG.
- It was announced in 2/2010 with immediate availability at the Mobile World Congress.
- The XMM 6260 is a slim 3G HSPA+ modem that is based on two highly integrated Infineon devices:
  - the X-GOLD™626 baseband processor and
  - the SMARTi™UE2 Radio Frequency (RF) transceiver.
- It supports the HSPA+ Rel. 7 3GPP standard [131].
- In 8/2010 Intel acquired Infineon's Wireless Solution business.
- Next, based on this acquisition Intel developed the XMM line of wireless broadband modems further on and equipped their smartphone platforms with subsequent models of the XMM line, as indicated in the next Figure.

5.2.3 The Medfield platform (31)

Intel's smartphone roadmap from 2012 [176]



5.2.3 The Medfield platform (32)

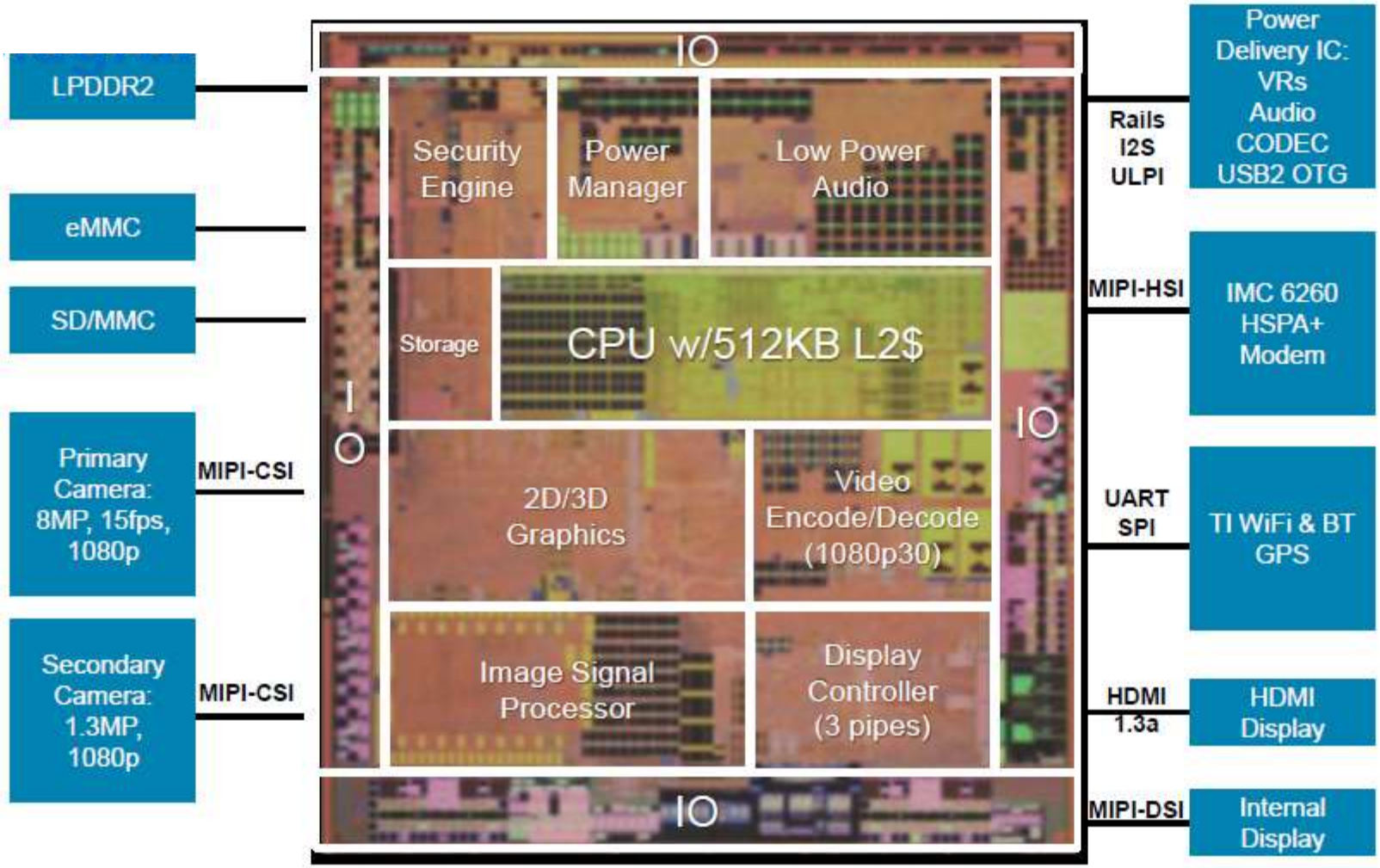
Wireless broadband support of Intel's smartphone platforms (Based mainly on [113])

Platform	Models	Broadband unit	Supported 3G/4G standard	Download speed Mbps	Upload speed Mbps
Medfield	Z2480/ Z2460	XMM 6260	HSPA+ ~Rel. 7	21 Mbps	5.4 Mbps
Lexington	Z2420	XMM 6265	HSPA+ ~Rel. 7	21 Mbps	11.5 Mbps
Clover Trail+	Z2580- Z2520	XMM 7160	LTE & HSPA+ Rel. 9	42 Mbps	11.5 Mbps
Merrifield	n.a.	XMM 7260	LTE Rel. 9	150 Mbps	?? Mbps

5.2.3 The Medfield platform (33)

Implementation of the Medfield platform

Block diagram of the Penwell processor [126]

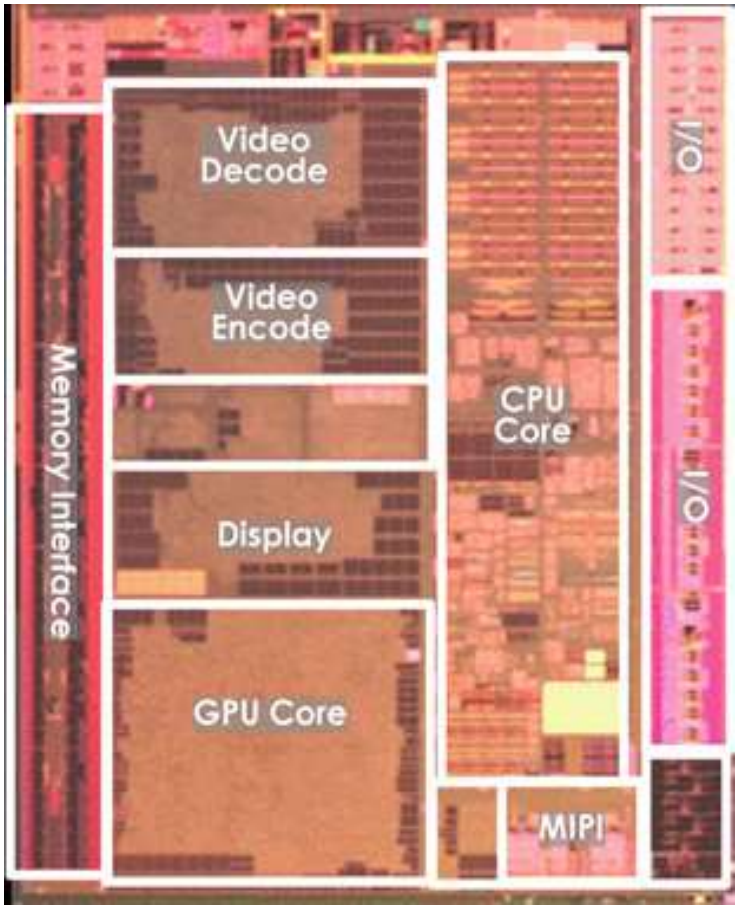


EMMC: Embedded Multi-Media Controller

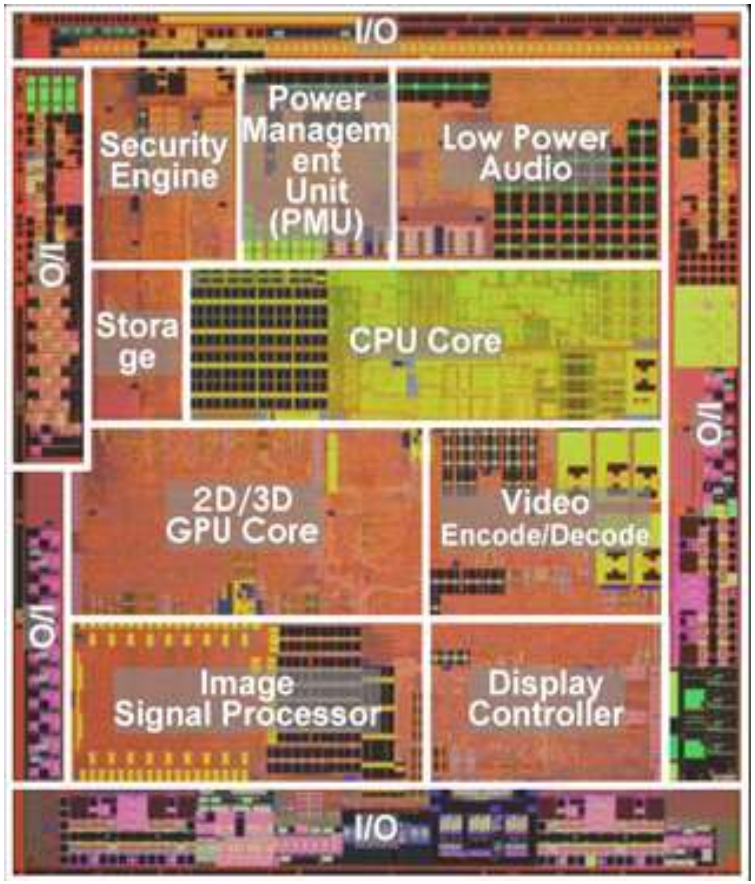
5.2.3 The Medfield platform (34)

Comparing the layout of the Lincroft (Moorestown) and Penwell (Medfeld) dies [132]

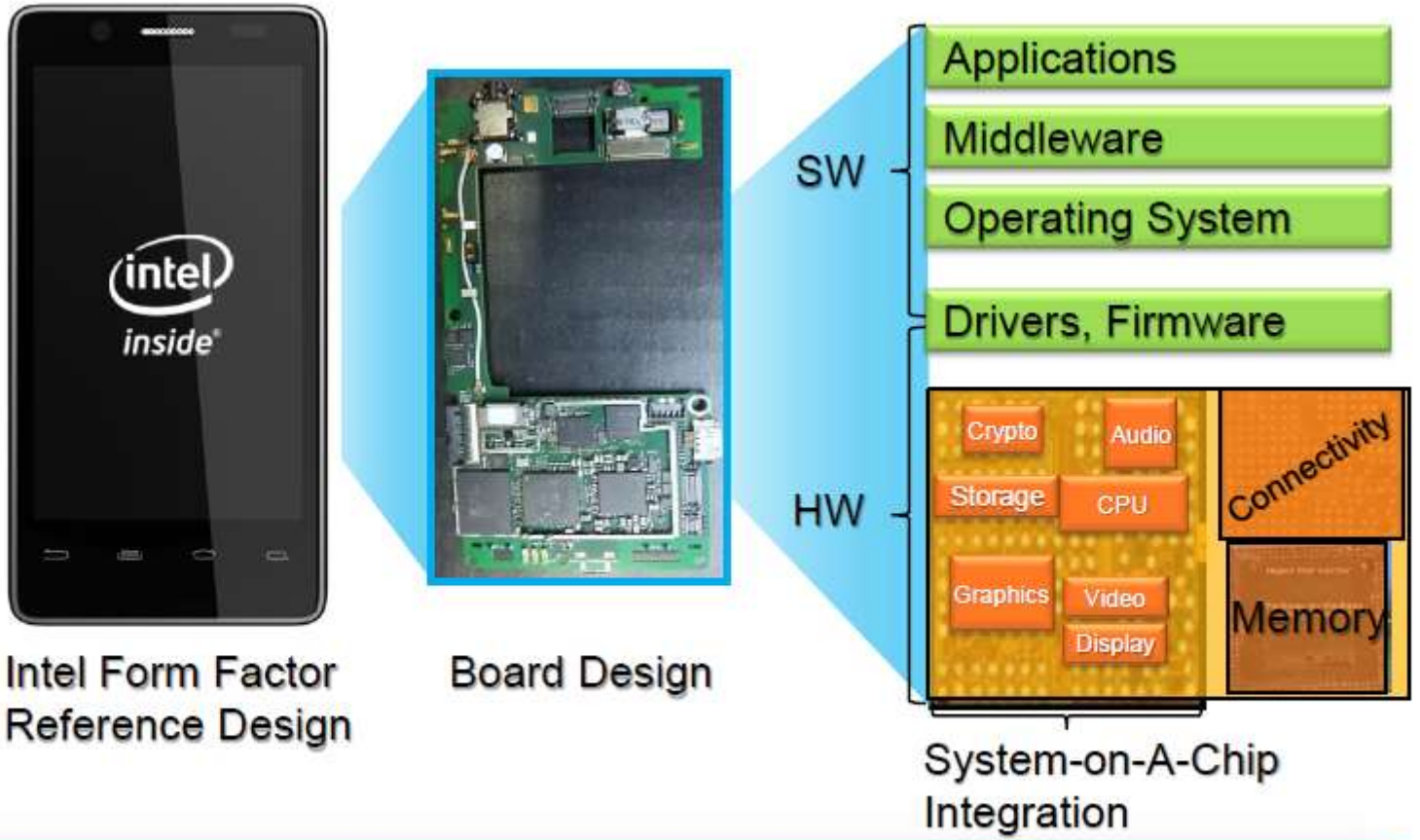
Lincroft (Moorestown) 32 nm



Penwell (Medfield) 32 nm

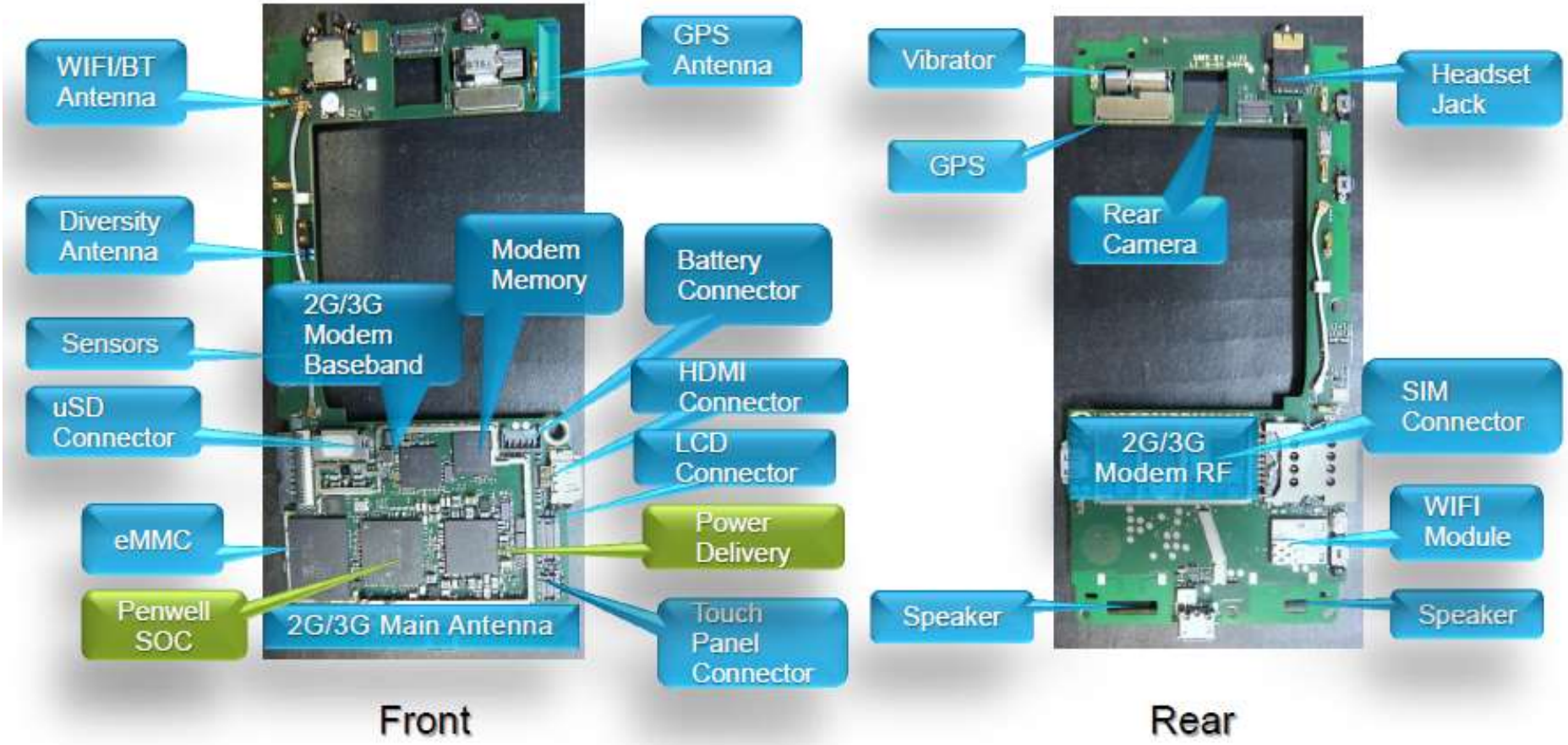


System layout of Medfield [126]



5.2.3 The Medfield platform (36)

System ingredients of Medfield [126]



5.2.3 The Medfield platform (37)

Power consumption and performance figures of the Medfield reference design [133]

5.2.3 The Medfield platform (38)

Market reception of the Medfield platform

Due to its favorable performance and power consumption features the Medfield platform became Intel's first platform that attracted smartphone firms to built their designs on it, including

- Lava Xolo X900
- Lenovo K800
- Motorola RAZRi
- Orange San Diego
- ZTE Grand X IN

5.2.3 The Medfield platform (39)

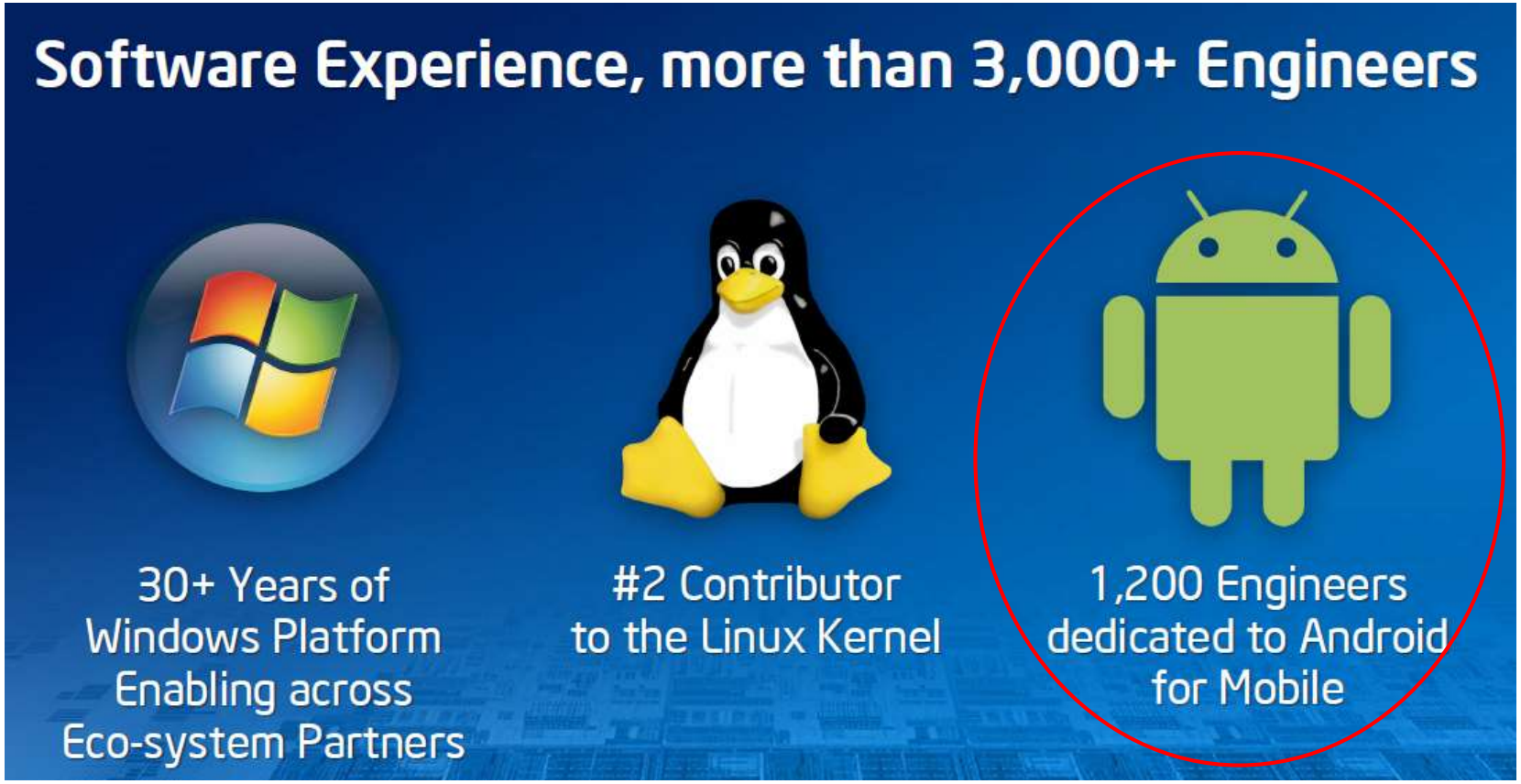
Medfield based smartphones and tablets [58]

5.2.3 The Medfield platform (40)

Intel's effort to conquer the mobile market

Intel devoted unbelievable huge human resources to beat market leading ARM-based smartphones and tablets in performance and power consumption.

As an example, in their 2012 Investor meeting (5/2012) Intel revealed that more than 3000 engineers are working on OS support, among them about 1200 engineers are dedicated to optimize microarchitectures running Android, as indicated below [43].



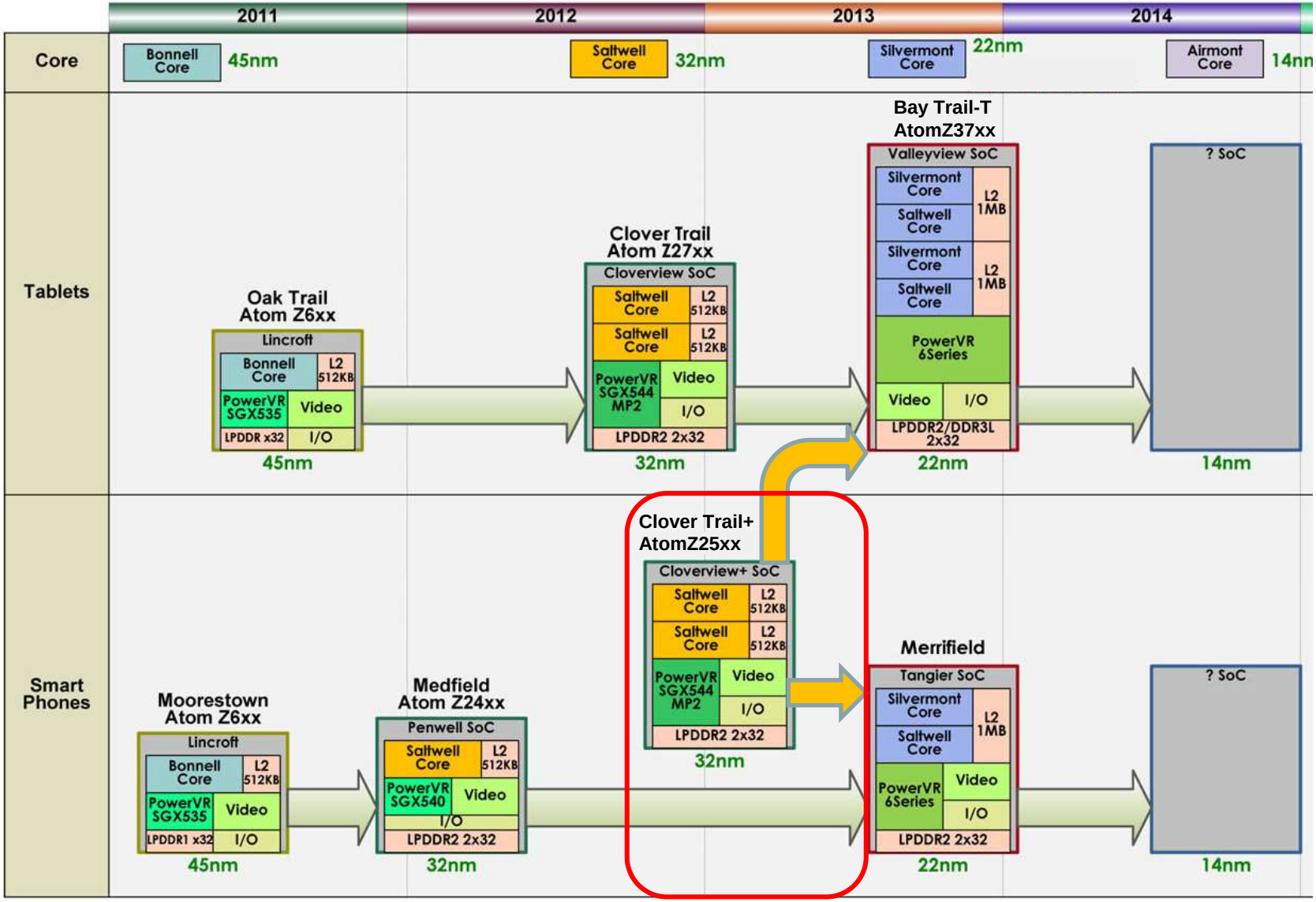
5.2.4 The Clover Trail+ platform as a smartphone platform

5.2.4 The Clover Trail+ platform as a smartphone platform

- Disclosed already in Intel's smartphone roadmap from 5/2012 (see next slide).
- Introduced in 2/2013 at the Mobile World Congress (MWC) primarily for Android smartphones, but used later on also for Android tablets.

5.2.4 The Clover Trail+ platform as a smartphone platform (2)

Positioning the Clover Trail+ platform in Intel's tablet and smart phone platforms [110]



5.2.4 The Clover Trail+ platform as a smartphone platform (3)

Contrasting the Medfield and Clover Trail+ smartphone reference designs-1 [135]

The Clover Trail+ platform is a significantly enhanced smartphone platform when compared with the previous Medfield platform, as the next Figure shows.

5.2.4 The Clover Trail+ platform as a smartphone platform (4)

Contrasting the Medfield and Clover Trail+ smartphone reference designs-2 [135]

	Medfield Smartphone Reference Design	Clover Trail+ Smartphone Reference Design
CPU	Intel® Atom™ SC @2.0** GHz	Intel® Atom™ DC Processor @ 2.0** GHz
Cores/Threads	1C / 2T	2C / 4T
Process	32nm	32nm
Cellular	Intel® XMM™ 6260 - HSPA+ 21Mbps	Intel® XMM™ 6360 (HSPA+ 42 Mbps)
GPU	SGX 540 @ 400 MHz	SGX 544MP2 up to 533MHz
RAM	1 GB LPDDR2 @ 400 MHz (2GB Max)	2 GB LPDDR2 @ 1066MTS
Internal Storage	64GB NAND Package Max	256GB NAND Package Max
Camera	8 MP with AF/LED Flash, 1080p30 video recording, 1.3 MP front facing	16 MP with AF/LED Flash, 1080p30 video recording, 2 MP front facing
Imaging	Image Signal Processor	Image Signal Processor
Supported OS	Android 4.0.4 (Ice Cream Sandwich)	Android 4.2 (Jelly Bean)

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5.2.4 The Clover Trail+ platform as a smartphone platform (5)

Wireless broadband support of Intel's smartphone platforms (Based mainly on [113])

Platform	Models	Broadband unit	Supported 3G/4G standard	Download speed Mbps	Upload speed Mbps
Medfield	Z2480/ Z2460	XMM 6260	HSPA+ ~Rel. 7	21 Mbps	5.4 Mbps
Lexington	Z2420	XMM 6265	HSPA+ ~Rel. 7	21 Mbps	11.5 Mbps
Clover Trail+	Z2580- Z2520	XMM 7160	LTE & HSPA+ Rel. 9	42 Mbps	11.5 Mbps
Merrifield	n.a.	XMM 7260	LTE Rel. 9	150 Mbps	?? Mbps

5.2.4 The Clover Trail+ platform as a smartphone platform (6)

Main features of the Clover Trail+ platforms targeting performance oriented smartphones

Platform	Moorestown	Medfield	Clover Trail+	Merrifield	Moorefield
Available	(09/2009 announced)	01/2012	02/2013	02/2014	06/2014
Focus	High end smartphones	Mainstream smartphones	Smartphones	Smartphones	Smartphones
AP processor	Lincroft	Penwell	Cloverview	Tangier	Anniedale
Models	Z6xx	Z2460/Z280	Z2520-Z2580	Z3460/Z3480	Z3530-Z3590
Technology	45nm	32nm	32nm	22nm	22nm
Die size	65 mm^2				
No. of trans.	140 mtrs				
CPU micro-arch.	Bonnell	Saltwell	Saltwell	Silvermont	Silvermont
32/64-bit	32-bit	32-bit	32-bit	64-bit	64-bit
No. of cores	1	1	2	2	4
HT	HT	HT	HT	no HT	no HT
fc [GHz] (Turbo)	0.9-1.9 GHz	1.2-2.0 GHz	1.2-2.0 GHz	1.6-2.13 GHz	1.33- 2.5 GHz
L2	512 kB	512 kB	2x512 kB	1 MB/2 cores	1 MB/2 cores
Mem. channels	Single 32-bit mem. ch. MC on proc. die	Dual 32-bit mem. ch. MC on proc. die	Dual 32-bit mem. ch. MC on proc. die	2x32-bit mem. ch. MC on proc. die	2x32-bit mem. ch. MC on proc. die
Memory	LPDDR1-400/DDR2-800	LPDDR2-800 POP	LPDDR2-1066 POP	LPDDR3-1066	LPDDR3-1600
GPU	GMA 600 (Power VR SGX 535)	Power VR SGX 540	Power VR SGX 544 MP2	Power VR G6400	Power VR G6430
DX	DX 9.0c	DX 9	DX 9.L3	DX10	DX10
Rear camera res.	5 Mpixel	8 Mpixel	13 Mpixel	13 Mpixel	13 Mpixel
GPU clock	200/400 MHz	400 MHz	300-533 MHz	400/457 MHz	457 MHz
ISP	—	ISP	ISP	ISP	ISP
Security Engine	—	Security Engine	Security Engine	Security Engine	Security Engine
Integr. baseband m.	No, wireless modem	No, XMM 6260	No, XMM 6268/6360/7160	No, XMM 7160/7260	No, XMM 7360
FSB	cDMI (8bit) (400 MT/s per dir.)	—	—	—	—
Proc. TDP	1.3-3.0 W				
Socket	BGA 518	BGA 617	BGA 760	PoP	PoP
Platform Cont. Hub	MP20 (Langwell)	—	—	—	—
OS at launch	Moblin 2.1 MeeGo/Android 2.1	Android 2.3.7/ 4.1.0	Android 4.2	Android 4.4.2	Android 4.4.2
Smartphone eExamples	Aava Virta Android LG GW990 both withdrawn	Lava Xolo X900 Lenovo K800 Motorola RAZRi Orange San Diego ZTE Grand X IN	Lenovo K900 ZTE Geek/ Grand X2 IN	Dell Venue 7 Dell Venue 8	Asus Fonepad 7 Asus Fonepad 8 Nokia N1, Dell Venue 8 7000,

5.2.4 The Clover Trail+ platform as a smartphone platform (7)

Model features of the processors of the Clover Trail+ platform [135]

	Z2580	Z2560	Z2520
CPU Frequency	Up to 2.0Ghz	Up to 1.6Ghz	Up to 1.2Ghz
Process Tech	32nm		
CPU performance	Dual Core with HT (4 Threads)		
Memory	LPDDR2 2x32-bit 1066MTS		
Video Dec/Enc	1080p30 /1080p30		
Enhanced Video codecs	MPEG-4,H.264,DivX,VC-1,WMV-9,VP6		
Enhanced Audio codecs	AMR-NB AMR-WB AAC , MP3 MIDI, WMA		
Display support	WUXGA (1920x1200)		
Graphics	SGX 544MP2 533 MHz Boost	SGX 544MP2 400 MHz	SGX 544MP2 300 MHz
Camera	Primary: 16MP; Secondary: 2MP		
Advanced imaging features	Continuous shooting, continuous viewfinder, mobile HDR, 2-axis DVS		
Modem	XMM™ 6360		

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5.2.4 The Clover Trail+ platform as a smartphone platform (8)

Comparing the model features of the Medfield and Clover Trail+ processors [135]

Intel Clover Trail+ SoC Lineup				
	Intel Atom Z2580	Intel Atom Z2560	Intel Atom Z2520	Intel Atom Z2460
CPU Cores/Threads	2 / 4	2 / 4	2 / 4	1 / 2
CPU Max Turbo Frequency	2.0GHz	1.6GHz	1.2GHz	2.0GHz
CPU Max Non-Turbo Frequency	933MHz	933MHz	933MHz	900MHz
CPU Low Frequency Mode	800MHz	800MHz	800MHz	600MHz
L2 Cache	2 x 512KB	2 x 512KB	2 x 512KB	512KB
Memory Interface	2 x 32-bit LPDDR2-1066			2 x 32-bit LPDDR2-800
Display support	1920 x 1200			1024 x 768
GPU	PowerVR SGX 544MP2			PowerVR SGX 545
GPU Max Turbo Frequency	533MHz	400MHz	300MHz	533MHz
Baseband Pairing	XMM 6360			XMM 6260

5.2.4 The Clover Trail+ platform as a smartphone platform (9)

Performance and current consumption (in Ampere) of recent smartphones and tablets-1

ABI Research compared performance and power consumption of the dual core 2.0 GHz Clover Trail+ based Lenovo K900 smartphone that is equipped with two Imagination Technologies PowerVR SGX 544 GPU cores with latest smartphone and tablet platforms, such as

- Samsung Nexus 10 tablet powered by a dual-core 1.7GHz Cortex-A15 and a Mali-T604 GPU,
- Samsung i9500 Galaxy S4 smartphone with a "big.LITTLE" Exynos Octa with a quad-core 1.6GHz Cortex-A15 and quad-core 1.2GHz Cortex-A7 coupled with a PowerVR SGX 544MP3 GPU,
- Samsung i337 Galaxy S4 smartphone with a 1.9GHz Qualcomm APQ8064T Snapdragon 600 with four Krait 300 cores and an Adreno 320 GPU and
- Asus Nexus 7 tablet with an Nvidia Tegra3 with four 1.2GHz Cortex-A9 cores and a ULP GeForce GPU [136].

5.2.4 The Clover Trail+ platform as a smartphone platform (10)

Performance and current consumption (in Ampere) of recent smartphones and tablets-2

ABI Research did not specify the benchmark programs run.

Table 1 Processor	intel Z2580 (CloverTrail+)			Samsung Exynos 5250			Samsung Exynos Octa			Qualcomm APQ8064T			Nvidia Tegra 3		
Phone	Lenovo K900			Samsung Nexus 10			Samsung Galaxy S4 i9500			Samsung Galaxy S4 i377			Asus Nexus 7		
Core	Saltwell x2			Arm A15 x2			Arm A15 x4 + A7 x4			Krait 300 x4			Arm A9 x4		
Speed	2GHz			1.7GHz			1.6GHz			1.9GHz			1.3GHz		
		0.2	Display		0.5	Display		0.18	Display		0.176	Display		0.234	Display
Display	Score	Avg I	Peak I	Score	Avg I	Peak I	Score	Avg I	Peak I	Score	Avg I	Peak I	Score	Avg I	Peak I
RAM	8703	0.55	0.9	2243	1.42	1.63	3838	1.27	1.56	4235	0.563	1.084	1529	0.389	0.682
CPU	5547	0.85	1.05	3104	0.98	1.23	5277	1.38	1.71	5378	1.794	2.104	2886	0.896	1.186
2D graphics	1579	0.235	0.724	1478	0.46	1.15	1624	0.276	0.8	1549	0.409	1.104	298	0.217	0.511
3D graphics	6664	0.27	0.61	3819	0.72	1.37	8653	0.368	0.96	6628	0.578	1.404	1188	0.458	0.826
Pi	1.33	0.366	0.97	1.26	0.459	1.73	1.4	0.483	1.24	1.9	0.233	0.733	1.56	0.38	0.766
1080p Record		0.737	1.27		1.56	3.6		0.772	1.15		0.682	1.13			
Source: ABI Research															

Table: Performance and power consumption (given in Ampere drawn) of recent smartphones and tablets [136]

As the table shows, from the comparable CPU performance configurations (see CPU score) Intel's chip drew 0.85A of average current vs. 1.38A for the Samsung Exynos Octa, and 1.79A for the Qualcomm APQ8064T, ABI found [136].

This means that

- Intel's Z2580 based Clover Trail+ platform delivered comparable performance to the Samsung Exynos Octa and the Qualcomm APQ8064T.
- But Intel's chip consumed only 60 percent of the current of the Exynos Octa, and less than half (47 percent) of the current of the Qualcomm chip.

(The Octa chip is found within European versions of the Samsung Galaxy S4, while the Qualcomm chip is used in the U.S. version [136]).

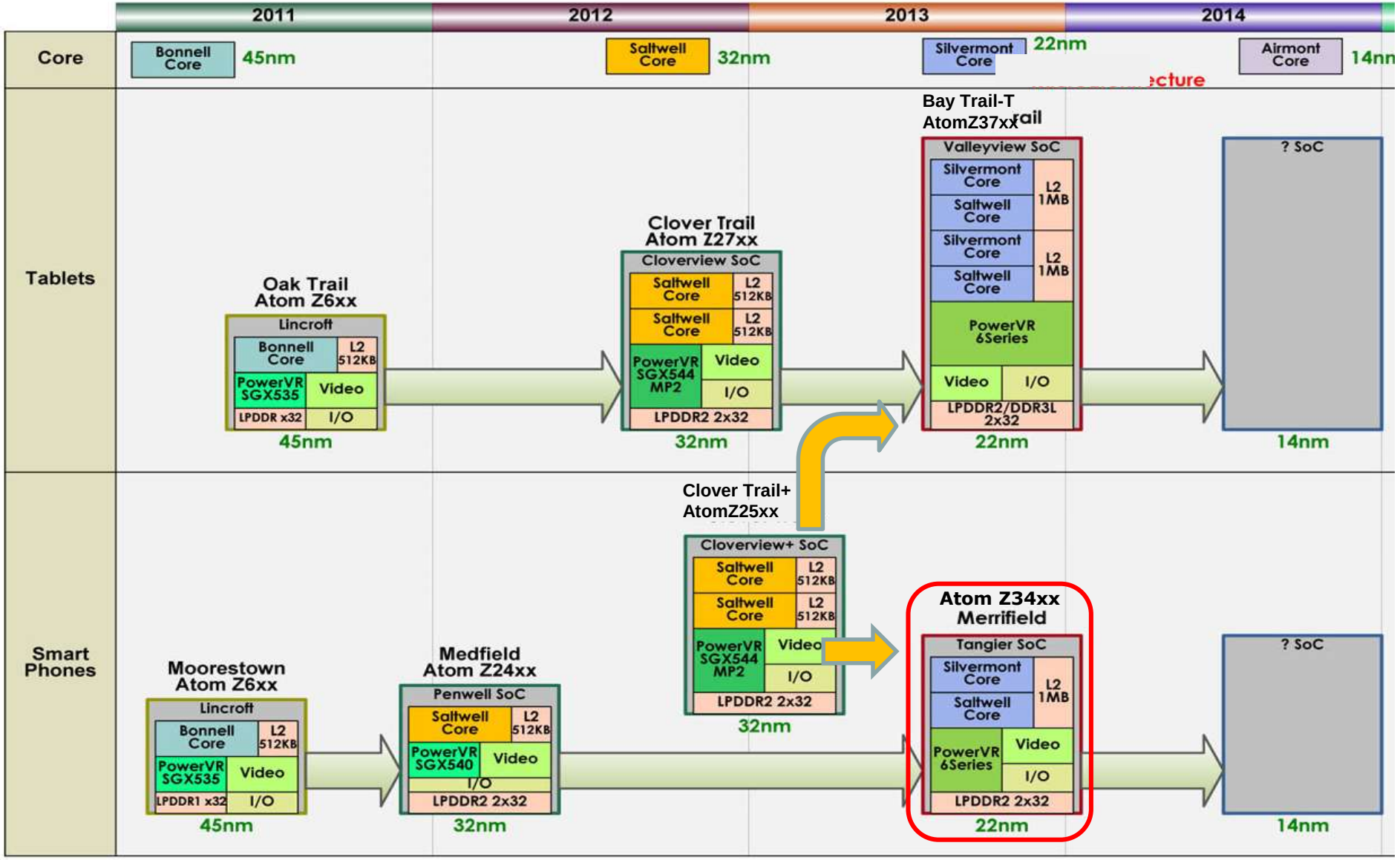
5.2.5 The Merrifield platform

5.2.5 The Merrifield platform

- It is based on the 22 nm Silvermont CPU.
- It is Intel's first 64-bit smartphone platform.
- Announced with no technical details in 6/2013 at Computex.
- Launched in 02/2014.

5.2.5 The Merrifield platform (2)

Positioning the Merrifield platform in Intel's tablet and smart phone platforms [110]



5.2.5 The Merrifield platform (3)

Main features of the Merrifield platforms targeting performance oriented smartphones

Platform	Moorestown	Medfield	Clover Trail+	Merrifield	Moorefield
Available	(09/2009 announced)	01/2012	02/2013	02/2014	06/2014
Focus	High end smartphones	Mainstream smartphones	Smartphones	Smartphones	Smartphones
AP processor	Lincroft	Penwell	Cloverview	Tangier	Anniedale
Models	Z6xx	Z2460/Z2480	Z2520-Z2580	Z3460/Z3480	Z3530-Z3590
Technology	45nm	32nm	32nm	22nm	22nm
Die size	65 mm^2				
No. of trans.	140 mtrs				
CPU micro-arch.	Bonnell	Saltwell	Saltwell	Silvermont	Silvermont
32/64-bit	32-bit	32-bit	32-bit	64-bit	64-bit
No. of cores	1	1	2	2	4
HT	HT	HT	HT	no HT	no HT
fc [GHz] (Turbo)	0.9-1.9 GHz	1.2-2.0 GHz	1.2-2.0 GHz	1.6-2.13 GHz	1.33- 2.5 GHz
L2	512 kB	512 kB	2x512 kB	1 MB/2 cores	1 MB/2 cores
Mem. channels	Single 32-bit mem. ch. MC on proc. die	Dual 32-bit mem. ch. MC on proc. die	Dual 32-bit mem. ch. MC on proc. die	2x32-bit mem. ch. MC on proc. die	2x32-bit mem. ch. MC on proc. die
Memory	LPDDR1-400/DDR2-800	LPDDR2-800 POP	LPDDR2-1066 POP	LPDDR3-1066	LPDDR3-1600
GPU	GMA 600 (Power VR SGX 535)	Power VR SGX 540	Power VR SGX 544 MP2	Power VR G6400	Power VR G6430
DX	DX 9.0c	DX 9	DX 9.L3	DX10	DX10
Rear camera res.	5 Mpixel	8 Mpixel	13 Mpixel	13 Mpixel	13 Mpixel
GPU clock	200/400 MHz	400 MHz	300-533 MHz	400/457 MHz	457 MHz
ISP	—	ISP	ISP	ISP	ISP
Security Engine	—	Security Engine	Security Engine	Security Engine	Security Engine
Integr. baseband m.	No, wireless modem	No, XMM 6260	No, XMM 6268/6360/7160	No, XMM 7160/7260	No, XMM 7360
FSB	cDMI (8bit) (400 MT/s per dir.)	—	—	—	—
Proc. TDP	1.3-3.0 W				
Socket	BGA 518	BGA 617	BGA 760	PoP	PoP
Platform Cont. Hub	MP20 (Langwell)	—	—	—	—
OS at launch	Moblin 2.1 MeeGo/Android 2.1	Android 2.3.7/ 4.1.0	Android 4.2	Android 4.4.2	Android 4.4.2
Smartphone eExamples	Aava Virta Android LG GW990 both withdrawn	Lava Xolo X900 Lenovo K800 Motorola RAZRi Orange San Diego ZTE Grand X IN	Lenovo K900 ZTE Geek/ Grand X2 IN	Dell Venue 7 Dell Venue 8	Asus Fonepad 7 Asus Fonepad 8 Nokia N1, Dell Venue 8 7000,

5.2.5 The Merrifield platform (4)

Competing designs to Intel ’s Merrifield platform

- Qualcomm’s Snapdragon S5
- Samsung’s Exynos 5 Octa and
- Nvidia’s Tegra 4.

5.2.5 The Merrifield platform (5)

Key features of the Merrifield line of processors [178]

Intel Merrifield & Moorefield specs							
	Intel Atom Z3460	Intel Atom Z3480	Intel Atom Z3530	Intel Atom Z3560	Intel Atom Z3570	Intel Atom Z3580	Intel Atom Z35960
Launch date	Q1/2014	Q1/2014	Q2/2014	Q2/2014	Q3/2014	Q2/2014	Q1/2015
Codename	Merrifield		Moorefield				
CPU Cores/Threads	2/2		4/4				
CPU Max Turbo Clock	1.60 GHz	2.13 GHz	1.33 GHz	1.83 GHz	2.0 GHz	2.33 GHz	2.5 GHz
GPU	PowerVR G6400		PowerVR G6430				
Max GPU Clock	457 MHz	533MHz	533 MHz	533MHz	640 MHz	640 MHz	640 MHz
No. of mem. channels	2x 32-bit		2x 32-bit				
Memory	LPDDR3-1066		LPDDR3-1600				
Companion XMM chip at intro.	XMM 6360 3G (HSPA+) DS: 42 Mbps		XMM7160 4G (LTE) DS: 150 Mbps				

5.2.5 The Merrifield platform (6)

Platform comparison: The Merrifield platform vs. the Moorefield platform [179]

Intel® processor Z2580 (Clover Trail+) vs. Intel® processor Z3480 (Merrifield)

Intel® processor Z2580 (Clover Trail+)		Intel® processor Z3480 (Merrifield)
Intel® Atom™ DC Processor with up to 2.0 GHz	CPU	Intel® Atom™ DC Processor with up to 2.13 Ghz
2C / 4T	Cores/Threads	2C , new micro architecture with out-of-order execution
32nm	Process	22nm
Intel XMM 6360 (HSPA+ 42 Mbps)	Cellular	Intel XMM 7160 – LTE 150Mbps DL / (HSPA+ 42 Mbps),
PowerVR SGX544MP2	GPU	PowerVR G6400 Quad Cluster new architecture with media compute via OpenCL, RenderScript
2 GB Max LPDDR2	RAM	4GB Max LPDDR3 @ 533MHz
256GB Package Max	Internal Storage	256GB Package Max
Rear facing: 13MP Max, 1080p30 Front-facing camera: 2MP Max	Camera	Rear facing: 13MP Max hardware capable, 1080p60 Front-facing camera: 2.1MP Max
Image Signal Processor	Imaging	Next Gen Intel Image Signal Processor
n/a	Video Processor	New: dedicated, programmable video signal processor
Android 4.1* (Jelly Bean)	Supported OS	Android* 4.4.2[2]

* Android is a trademark of Google Inc.; 1 At launch; 2 Depending on Google's release timing

5.2.5 The Merrifield platform (7)

Key innovations introduced along with the Silvermont-based Merrifield smartphone and Bay trail-T tablet platforms [137]

Performance and power consumption results are against Intel's prior smartphone platform.

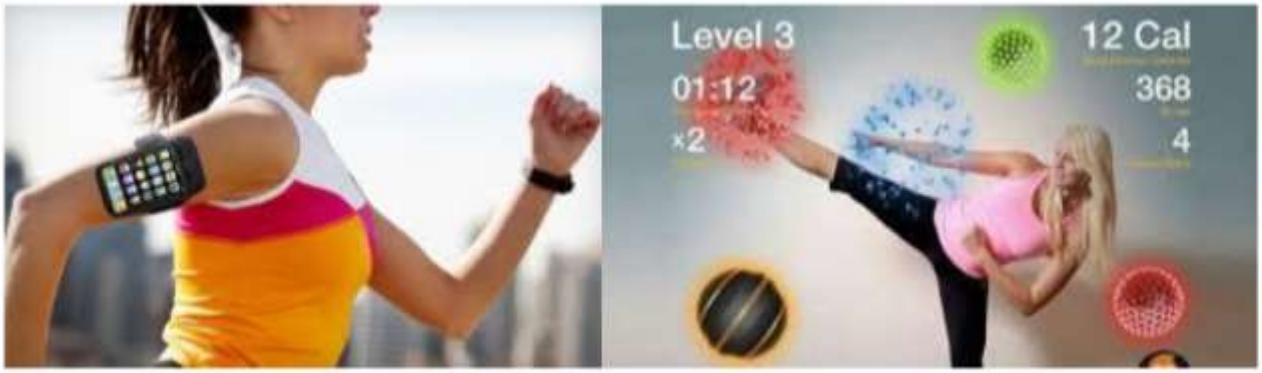
5.2.5 The Merrifield platform (8)

Main features of Intel's XMM6360/7160/7260 baseband modems [180]

Intel Baseband Comparison			
	XMM6360	XMM7160	XMM7260
Package Size, Type, Geometry	8.5 x 7.5 mm x 1.0 mm 40nm TSMC	9.5 x 7.5 mm x 1.0 mm 40nm TSMC	"Equivalent to 7160" 28nm TSMC
LTE	N	LTE FDD Cat. 3 (102 Mbps) Cat. 4 Upgrade (150 Mbps)	LTE-A TDD/FDD with Carrier Aggregation, Cat. 6 (300 Mbps)
HSPA+	DC-HSPA+ (HSDPA Cat 24 - 42 Mbps, HSUPA Cat 7 - 11.2 Mbps)	DC-HSPA+ (HSDPA Cat 24 - 42 Mbps, HSUPA Cat 6 - 5.7 Mbps)	DC-HSPA+ (? Category or MIMO layers)
CDMA	N	N	N
TD-SCDMA	N	N (TDD-LTE and TD-SCDMA compatible, not enabled, may be enabled later with 7162 coprocessor)	Y
Voice Enabled	Y	Y	Y
Transceiver	SMARTi UE3 7.0 x 7.5 mm 65nm CMOS	SMARTi 4G 7.0 x 7.5 mm 65nm CMOS	"Next Gen" (?) mm 65nm CMOS

5.2.5 The Merrifield platform (9)

Integrated sensor hub [179]



Intel® Atom™ processor Z34/Z35 integrate a low power sensor solution.

This allows to deliver contextual information to apps with motion & gesture sensing, audio sensing, location sensing and contextual analyses with out draining the battery

Example Solutions:

Life Visualization

Record and analyze user's personal data history to view and track behaviors

Device Personalization

Automatic adjustment of your device settings (ring tone, wireless access) based on user context to improve ease of use

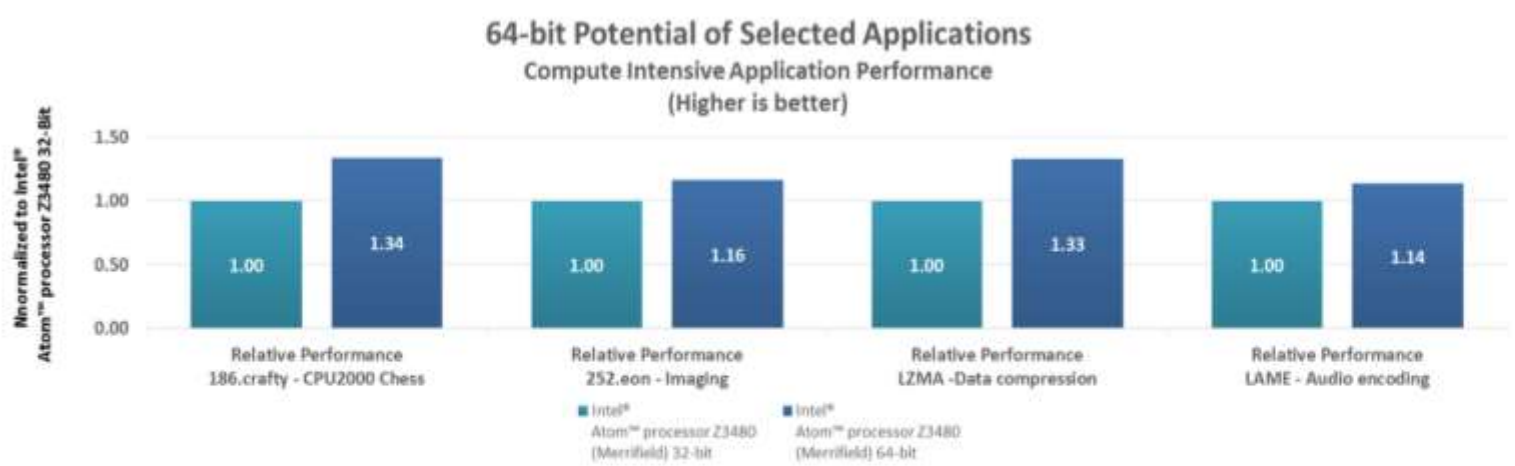
Predictive Assistant

Keeps users a step ahead by learning their habits and preferences & present information before they ask for it

5.2.5 The Merrifield platform (10)

Performance increase for 64-bit processing vs. 32-bit processing on an Atom Z3480 (Merrifield) processor [179]

Performance estimates for compute intensive applications: 32 bit vs. 64 bit



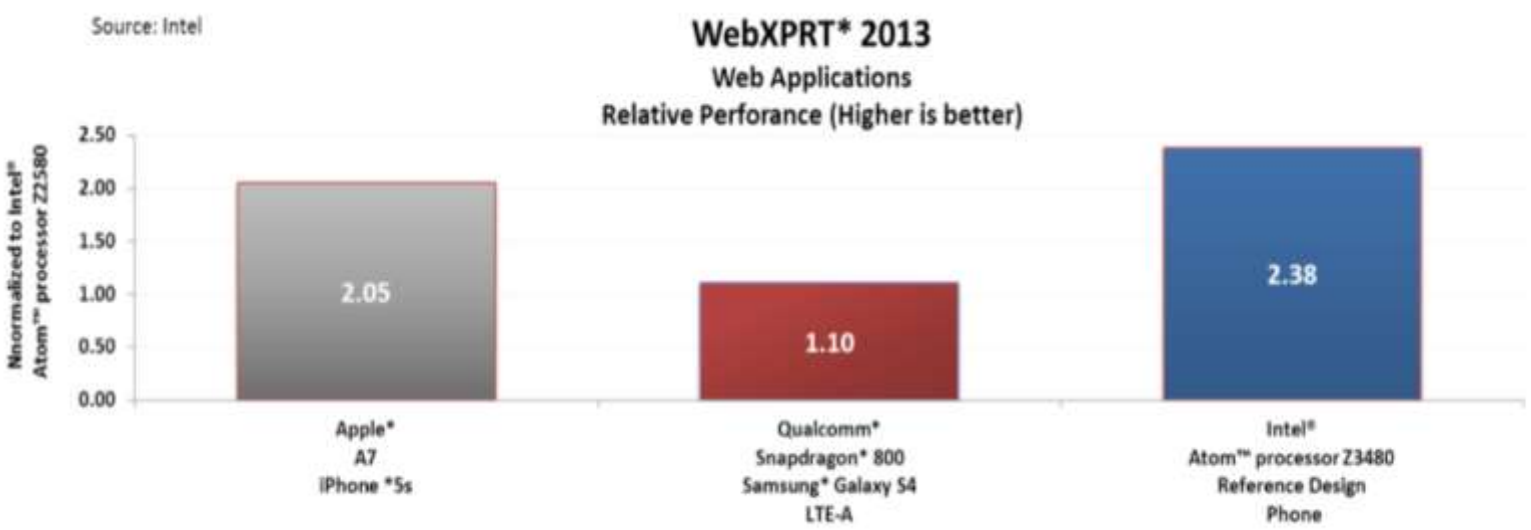
Intel® Atom™ Z3480 (Merrifield) in 64-Bit mode can deliver increased performance on certain application usages when 64-bit Android applications are available

Intel® Atom™ Z3480 (Merrifield) is Intel's 2nd generation Android 64 bit ready SoC

Software and workloads used in performance tests may have been optimized for performance only on Intel microprocessors. Performance tests, such as SYSmark and MobileMark, are measured using specific computer systems, components, software, operations and functions. Any change to any of those factors may cause the results to vary. You should consult other information and performance tests to assist you in fully evaluating your contemplated purchases, including the performance of that product when combined with other products. **For more information go to** http://www.intel.com/performance Note: See configurations and workload description in backup. SPECint results have been estimated based on internal Intel analysis and are provided for informational purposes only. Any difference in system hardware or software design or configuration may affect actual performance. ++ Based on SPEC*CPU2000 estimates. *Other names and brands may be claimed as the property of others.

5.2.5 The Merrifield platform (11)

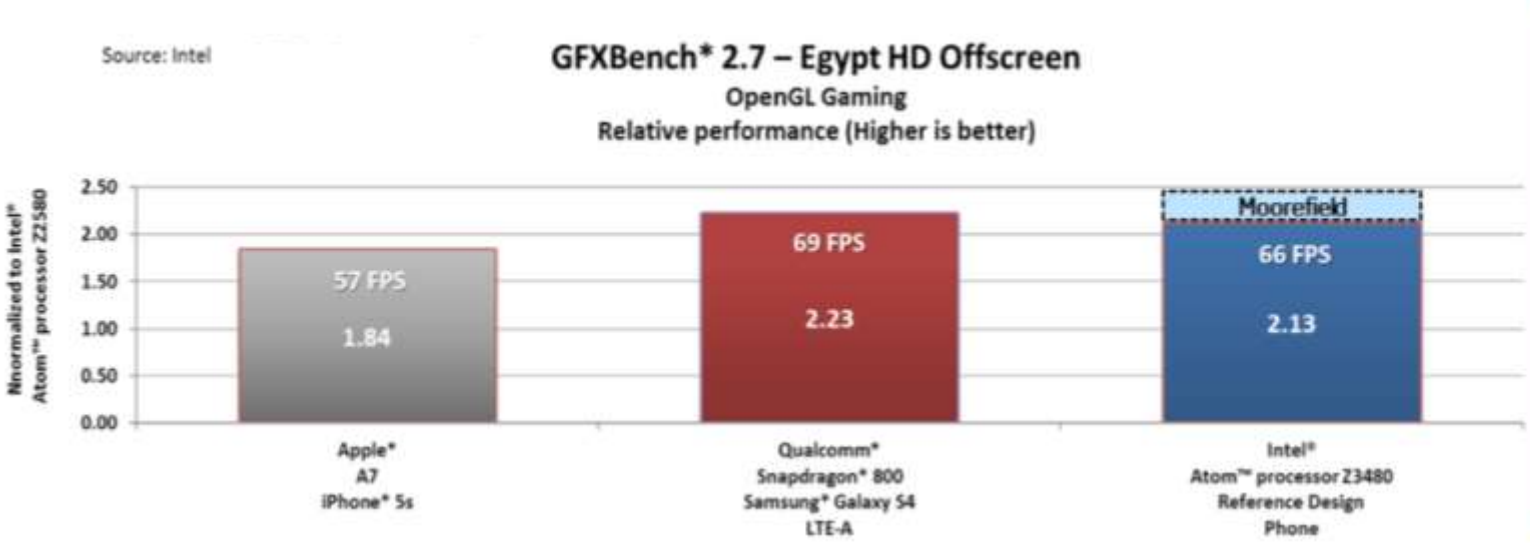
Web application performance of Z3480 (Merrifield) processors vs. competing smartphones [179]



The Intel® Atom™ processor Z3480 (Merrifield) delivers up to 2x web application performance relative to Qualcomm* Snapdragon* S800

5.2.5 The Merrifield platform (12)

3D gaming performance of Z3480 (Merrifield) processors vs. competing smartphones [179]



Intel's Atom™ processor Z3480 (Merrifield) is competitive on 3D gaming as measured by GFXBench* 2.7 Egypt HD Offscreen

5.2.5 The Merrifield platform (13)

Market expectations

- Merrifield is designed to compete with the energy-efficient ARM chips that are inside the vast majority of smartphones and tablets today [139].
- It can be taken for granted that the 22 nm Merrifield has very attractive performance and power consumption figures when contrasted with recent 28 nm ARM CPUs.

Nevertheless, in 2014 Intel achieved only less than 1 % share in revenue in smartphone application processors [177] and finally Intel abandoned the mobile and tablet market in 04/2016, as discussed in Section xx.

5.2.6 The Moorefield platform

5.2.6 The Moorefield platform

- It is based on the same 22 nm Silvermont CPU as the Merrifield platform.
- Announced with no technical details in 6/2013 at Computex.
- Launched in 02/2014.
- It has 4 cores and an enhanced GPU and thus higher compute and graphics performance compared to the Merrifield platform.

5.2.6 The Moorefield platform (2)

Platform comparison: The Moorefield platform vs. the Merrifield platform [179]

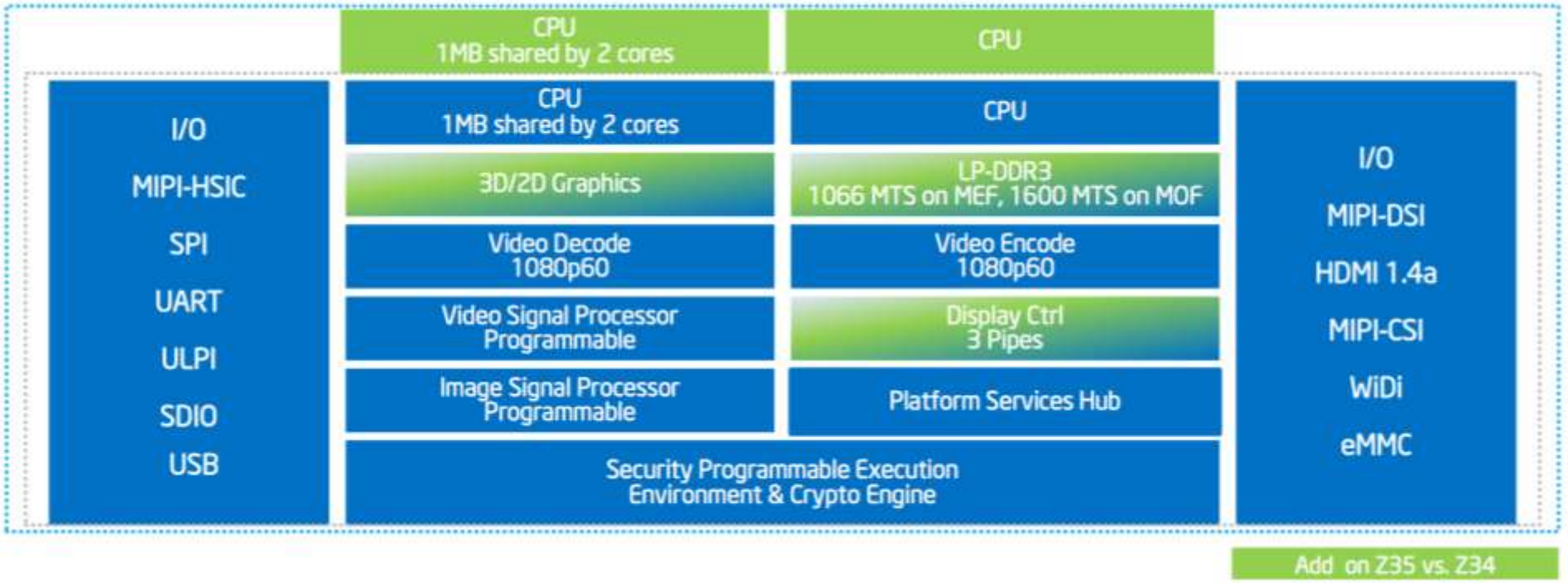
Intel® processor Z34XX (Merrifield) vs. Intel® processor Z35XX (Moorefield)

Intel® processor Z34XX (Merrifield)		Intel® processor Z35XX (Moorefield)
Intel® Atom™ DC Processor with up to 2.13 Ghz	CPU	Intel® Atom™ Quad Core Processor with up to 2.3 Ghz
2C , new micro architecture with out-of-order execution	Cores/Threads	4C , new micro architecture with out-of-order execution
22nm	Process	22nm
Intel XMM 7160 – LTE 150Mbps DL / (HSPA+ 42 Mbps),	Cellular	Intel XMM 7160 – LTE 150Mbps DL / (HSPA+ 42 Mbps) Intel XMM 6360 – HSPA+ 42 Mbps DSDS Intel XMM 7260 with CA
PowerVR G6400 Quad Cluster new architecture with media compute via OpenCL, RenderScript	GPU	PowerVR G6430 Quad Cluster new architecture with media compute via OpenCL, RenderScript
4GB Max LPDDR3 @ 533MHz	RAM	4GB Max LPDDR3 @ 800MHz
256GB Package Max	Internal Storage	256GB Package Max
Rear facing: 13MP Max hardware capable, 1080p60 Front-facing camera: 2.1MP Max	Camera	Rear facing: 13MP Max hardware capable, 1080p60 Front-facing camera: 2.1MP Max
Next Gen Intel Image Signal Processor	Imaging	Next Gen Intel Image Signal Processor
New: dedicated, programmable video signal processor	Video Processor	New: dedicated, programmable video signal processor
Android* 4.4.2-L[2]	Supported OS	Android* 4.4.2- L[2]

* Android is a trademark of Google Inc.; 1 At launch; 2 Depending on Google's release timing

5.2.6 The Moorefield platform (3)

Enhancements of Moorefield processors (Z35xx) vs. Merrifield processors (Z34xx) [179]



MEF: Merrifield
MOF: Moorefield

5.2.6 The Moorefield platform (4)

Key features of the Moorefield line of processors [178]

Intel Merrifield & Moorefield specs							
	Intel Atom Z3460	Intel Atom Z3480	Intel Atom Z3530	Intel Atom Z3560	Intel Atom Z3570	Intel Atom Z3580	Intel Atom Z35960
Launch date	Q1/2014	Q1/2014	Q2/2014	Q2/2014	Q3/2014	Q2/2014	Q1/2015
Codename	Merrifield		Moorefield				
CPU Cores/Threads	2/2		4/4				
CPU Max Turbo Clock	1.60 GHz	2.13 GHz	1.33 GHz	1.83 GHz	2.0 GHz	2.33 GHz	2.5 GHz
GPU	PowerVR G6400		PowerVR G6430				
Max GPU Clock	457 MHz	533MHz	533 MHz	533MHz	640 MHz	640 MHz	640 MHz
No. of mem. channels	2x 32-bit		2x 32-bit				
Memory	LPDDR3-1066		LPDDR3-1600				
Companion XMM chip at intro.	XMM 6360 3G (HSPA+) DS: 42 Mbps		XMM7160 4G (LTE) DS: 150 Mbps				

5.2.6 The Moorefield platform (5)

Main features of the Moorefield platforms targeting performance oriented smartphones

Platform	Moorestown	Medfield	Clover Trail+	Merrifield	Moorefield
Available	(09/2009 announced)	01/2012	02/2013	02/2014	06/2014
Focus	High end smartphones	Mainstream smartphones	Smartphones	Smartphones	Smartphones
AP processor	Lincroft	Penwell	Cloverview	Tangier	Anniedale
Models	Z6xx	Z2460/Z2480	Z2520-Z2580	Z3460/Z3480	Z3530-Z3590
Technology	45nm	32nm	32nm	22nm	22nm
Die size	65 mm^2				
No. of trans.	140 mtrs				
CPU micro-arch.	Bonnell	Saltwell	Saltwell	Silvermont	Silvermont
32/64-bit	32-bit	32-bit	32-bit	64-bit	64-bit
No. of cores	1	1	2	2	4
HT	HT	HT	HT	no HT	no HT
fc [GHz] (Turbo)	0.9-1.9 GHz	1.2-2.0 GHz	1.2-2.0 GHz	1.6-2.13 GHz	1.33- 2.5 GHz
L2	512 kB	512 kB	2x512 kB	1 MB/2 cores	1 MB/2 cores
Mem. channels	Single 32-bit mem. ch. MC on proc. die	Dual 32-bit mem. ch. MC on proc. die	Dual 32-bit mem. ch. MC on proc. die	2x32-bit mem. ch. MC on proc. die	2x32-bit mem. ch. MC on proc. die
Memory	LPDDR1-400/DDR2-800	LPDDR2-800 POP	LPDDR2-1066 POP	LPDDR3-1066	LPDDR3-1600
GPU	GMA 600 (Power VR SGX 535)	Power VR SGX 540	Power VR SGX 544 MP2	Power VR G6400	Power VR G6430
DX	DX 9.0c	DX 9	DX 9.L3	DX10	DX10
Rear camera res.	5 Mpixel	8 Mpixel	13 Mpixel	13 Mpixel	13 Mpixel
GPU clock	200/400 MHz	400 MHz	300-533 MHz	400/457 MHz	457 MHz
ISP	—	ISP	ISP	ISP	ISP
Security Engine	—	Security Engine	Security Engine	Security Engine	Security Engine
Integr. baseband m.	No, wireless modem	No, XMM 6260	No, XMM 6268/6360/7160	No, XMM 7160/7260	No, XMM 7360
FSB	cDMI (8bit) (400 MT/s per dir.)	—	—	—	—
Proc. TDP	1.3-3.0 W				
Socket	BGA 518	BGA 617	BGA 760	PoP	PoP
Platform Cont. Hub	MP20 (Langwell)	—	—	—	—
OS at launch	Moblin 2.1 MeeGo/Android 2.1	Android 2.3.7/ 4.1.0	Android 4.2	Android 4.4.2	Android 4.4.2
Smartphone eExamples	Aava Virta Android LG GW990 both withdrawn	Lava Xolo X900 Lenovo K800 Motorola RAZRi Orange San Diego ZTE Grand X IN	Lenovo K900 ZTE Geek/ Grand X2 IN	Dell Venue 7 Dell Venue 8	Asus Fonepad 7 Asus Fonepad 8 Nokia N1, Dell Venue 8 7000,

5.2.7 The Morganfield platform

5.2.7 The Morganfield platform

Key features	Morganfield
Technology	14 nm
CPU µarch.	Goldmont
Core count	4
Integrated modem	No
Companion chip	XMM 7360A Up to LTE cat. 10
Max. turbo clock	2.7 GHz
Status (Q2/2013)	In-development
Target OS	Android 6.
To be launched	Na.

Table: Main features of the planned but in 2016 cancelled Morganfield platform [145]

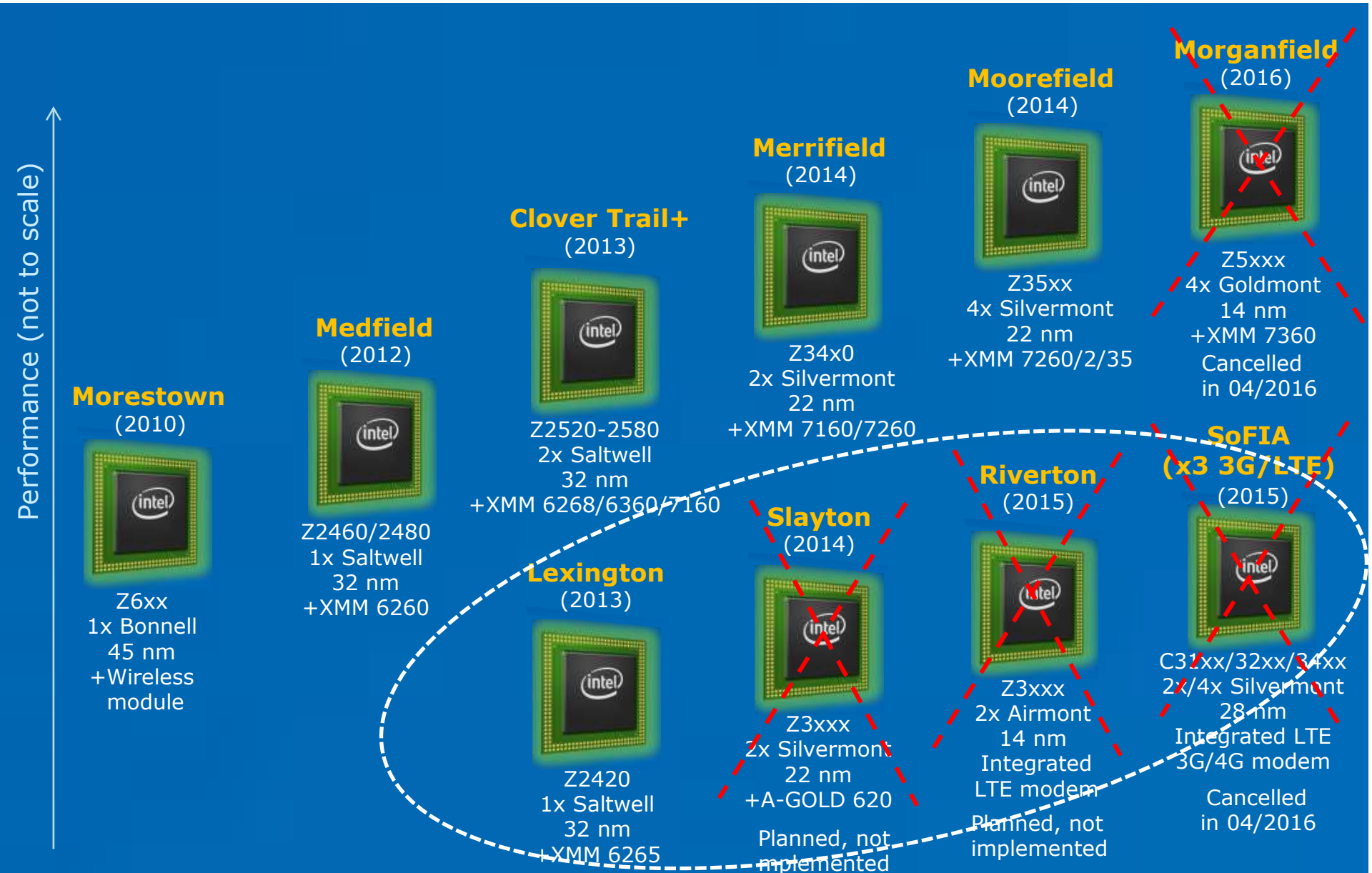
The Morganfield processor was cancelled in 04/2016 when the firm left the smartphone and tablet market, as discussed in Section xx.

5.3 Low-cost oriented smartphone platforms

- 5.3.1 Overview of Intel's low-cost oriented smartphone platforms
- 5.3.2 The Lexington platform
- 5.3.3 The SoFIA (aka x3) platform
- 5.3.4 The Slayton and Riverton platformsm

5.3.1 Overview of Intel’s low-cost oriented smartphone platforms

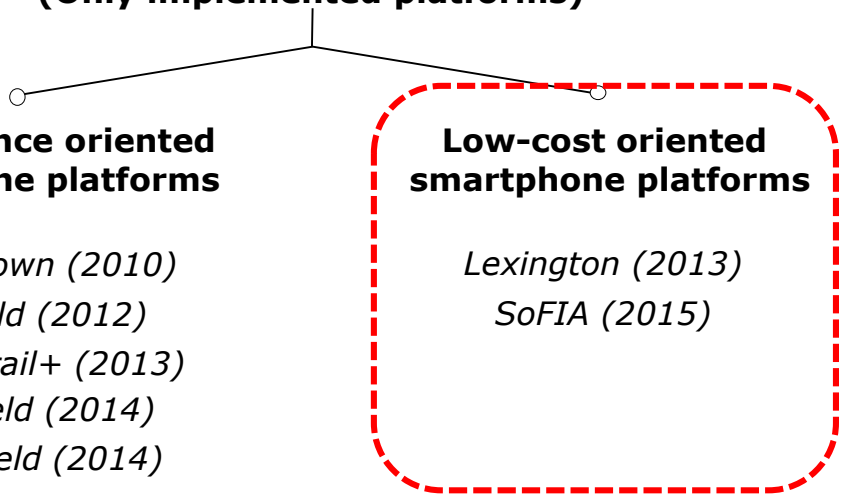
5.3.1 Overview of Intel's low-cost oriented smartphone platforms (based on [43]) -1



5.3.1 Overview of Intel's low-cost oriented smartphone platforms -2

As already mentioned, Intel's smartphone families can be subdivided into two groups according to the targeted price/performance points, as shown below.

Intel's smartphone platforms classified according to their price/performance orientation (Only implemented platforms)



In this Section we discuss Intel's low-cost oriented smartphone platforms.

5.3.1 Overview of Intel's low-cost oriented smartphone platforms (3)

Main features of the Atom-based platforms targeting low-cost oriented smartphones

Platform	Lexington	SoFIA (x3 3G/LTE)
Available	01/2013 (CES)	03/2015
Focus	Value smartphones	Value smartphone
AP processor	Penwell	x3
Models	Z2420	x3-C31xx/C32xxC34xx
Technology	32nm	28 nm (by TSMC)
Die size		
No. of trans.		
CPU micro-arch.	Saltwell	Silvermont
32/64-bit	32-bit	64-bit
No. of cores	1	2/4
HT	HT	no
fc [GHz] (Turbo up to)	1.2	1.4
L2	512 kB	1 MB/2 cores
Mem. channels	Dual mem. ch. MC on proc. die	Single 32-bit mem. ch. MC on proc. die
Memory up to	LPDDR2-800 POP	DDR2/3-1066 DDR3/3L-1333
GPU	Power VR SGX 540	Mali 400/450/T720
DX	DX 9	DX9?
Camera res.	8 Mpixel	13 Mpixel
GPU clock up to	400 MHz	600 MHz
FSB	—	--
Proc. SDP		2 W
ISP	ISP	ISP
Security Engine	Security Engine	
Baseband modem	No, XMM 6265 (3G) comp. chip	Yes, 3G or LTE
Socket	BGA 617	BGA361
Platform Controller Hub	—	--
OS at introduction	Android 4.0.4	Android 4.4
Smartphone examples	Acer Liquid C1 Lava Xolo X500 Safaricom Yolo	

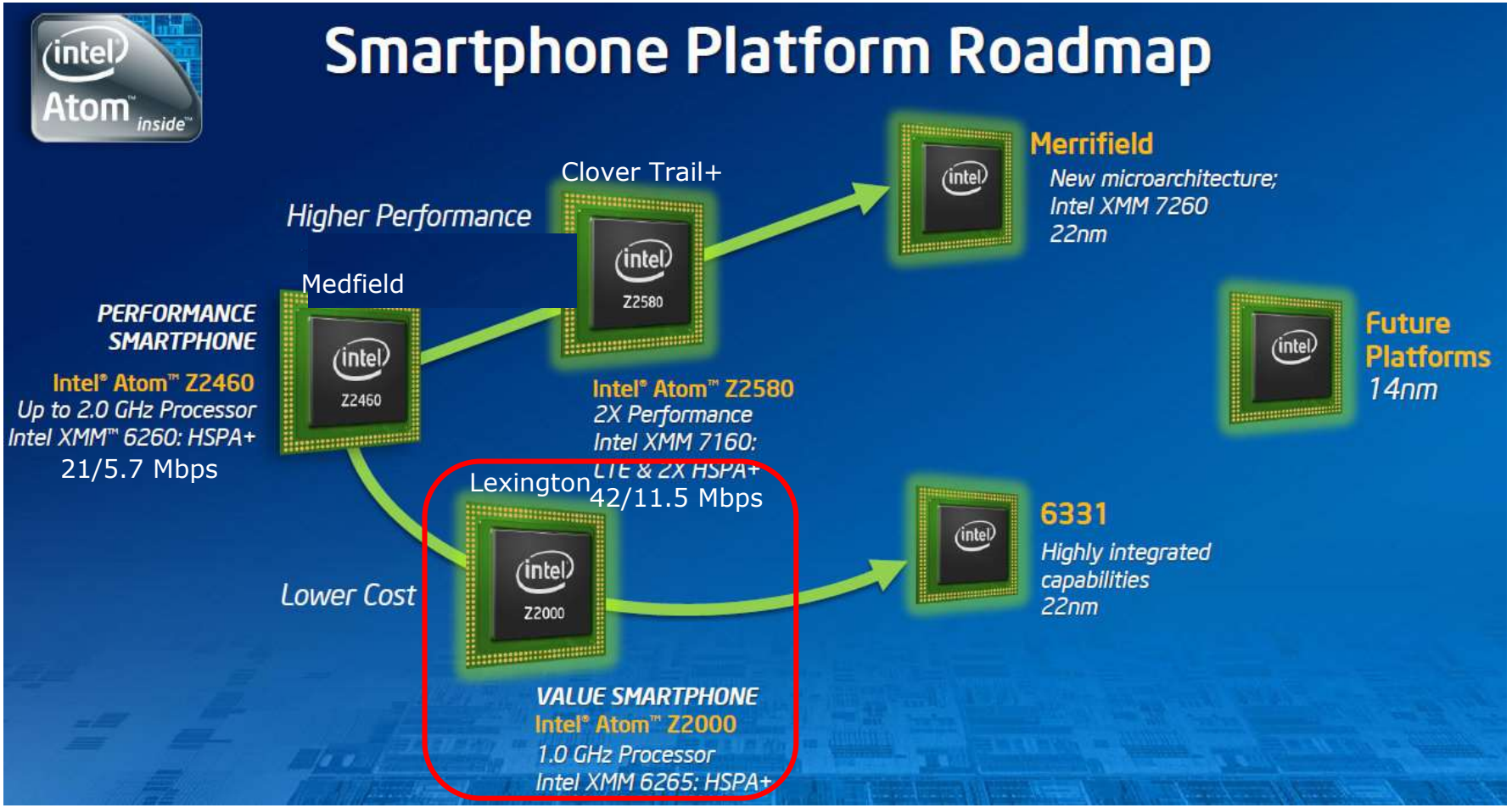
5.3.2 The Lexington platform

5.3.2 The Lexington platform

- Introduced in 01/2013 at CES (Consumer Electronics Show).
- There is only one model introduced, the Z2420.
- It is a lower clocked version of the Medfield line (1.2 GHz turbo clock frequency vs. 1.6 GHz Turbo clock frequency of the Medfield Z2460).
- The Lexington platform targets value smartphones for emerging markets.
- It is accompanied by the XMM6265 3G modem (a dual SIM version of the single SIM XMM6260).
- The first device was announced already at introduction (the Safaricom Yolo smartphone).

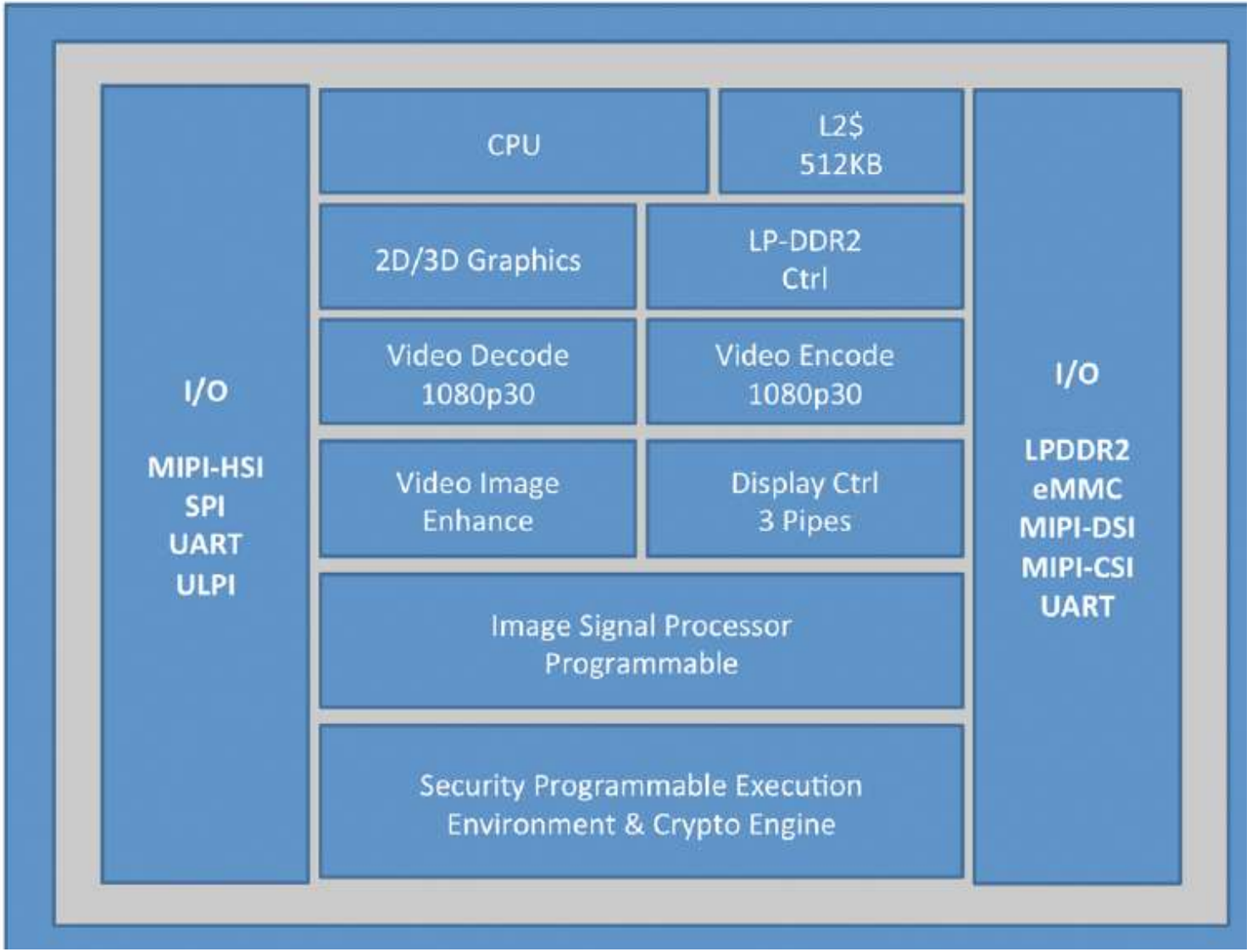
5.3.2 The Lexington platform (2)

Intel's smartphone roadmap from 2012 [176]



5.3.2 The Lexington platform (3)

Block diagram of the Lexington platform [134]



5.3.2 The Lexington platform (4)

Main features of Lexington low-cost oriented platform

Platform	Lexington	SoFIA (x3 3G/LTE)
Available	01/2013 (CES)	03/2015
Focus	Value smartphones	Value smartphone
AP processor	Penwell	x3
Models	Z2420	x3-C31xx/C32xxC34xx
Technology	32nm	28 nm (by TSMC)
Die size		
No. of trans.		
CPU micro-arch.	Saltwell	Silvermont
32/64-bit	32-bit	64-bit
No. of cores	1	2/4
HT	HT	no
fc [GHz] (Turbo up to)	1.2	1.4
L2	512 kB	1 MB/2 cores
Mem. channels	Dual mem. ch. MC on proc. die	Single 32-bit mem. ch. MC on proc. die
Memory up to	LPDDR2-800 POP	DDR2/3-1066 DDR3/3L-1333
GPU	Power VR SGX 540	Mali 400/450/T720
DX	DX 9	DX9?
Camera res.	8 Mpixel	13 Mpixel
GPU clock up to	400 MHz	600 MHz
FSB	—	--
Proc. SDP		2 W
ISP	ISP	ISP
Security Engine	Security Engine	
Baseband modem	No, XMM 6265 (3G) comp. chip	Yes, 3G or LTE
Socket	BGA 617	BGA361
Platform Controller Hub	—	--
OS at introduction	Android 4.0.4	Android 4.4
Smartphone examples	Acer Liquid C1 Lava Xolo X500 Safaricom Yolo	

5.3.3 The SoFIA (aka x3) platform

5.3.3 The SoFIA (aka x3) platform

Announcing the SoFIA platform [181]

- At their Annual Investor Day in 11/2013 Intel announced a platform including 64-bit processors with integrated baseband modems for entry and value smartphones and tablets and called it the SoFIA platform (*Smart of Feature Phone with Intel Architecture*).
- The first SoFIA models were reported to include 3G modems and were expected to appear by the end of 2014 whereas an LTE version should follow in the first half of 2015.

Remark

While the idea originated at Intel, SoFIA chips were conceived and designed by the former Infinion team (since 2011 acquired by Intel) in Singapore [182].

5.3.3 The SoFIA (aka x3) platform (2)

Announcing a strategic partnership with Rockchip to design and sell SoFIA processors [183]

- Intel disclosed a strategic agreement with the Chinese fabless semiconductor company Rockchip and provided first technical details about SoFIA processors in 05/2014.
- At introduction the SoFIA family of processors was made up of 3 models, including
  - a dual-core 3G version expected to be shipped in Q4/2014,
  - a quad-core 3G version that is expected to be shipped in 1H/2015,
  - and a dual-core LTE version, also due to in 1H/2015.
- Rockchip became authorized to design quad-core 3G versions of the SoFIA line.

5.3.3 The SoFIA (aka x3) platform (3)

Introduction of a new branding for the Atom family

- In 02/2015 Intel announced the x3/x5/x7 branding for their Atom processors in order to streamline the Atom family and help costumers to differentiate between entry-level, mid-range and high-performance models.
- This classification is similar to the Core i3/i5/i7 or Xeon E3/E5/E7 branding of the desktop and server processors, respectively, as indicated below.

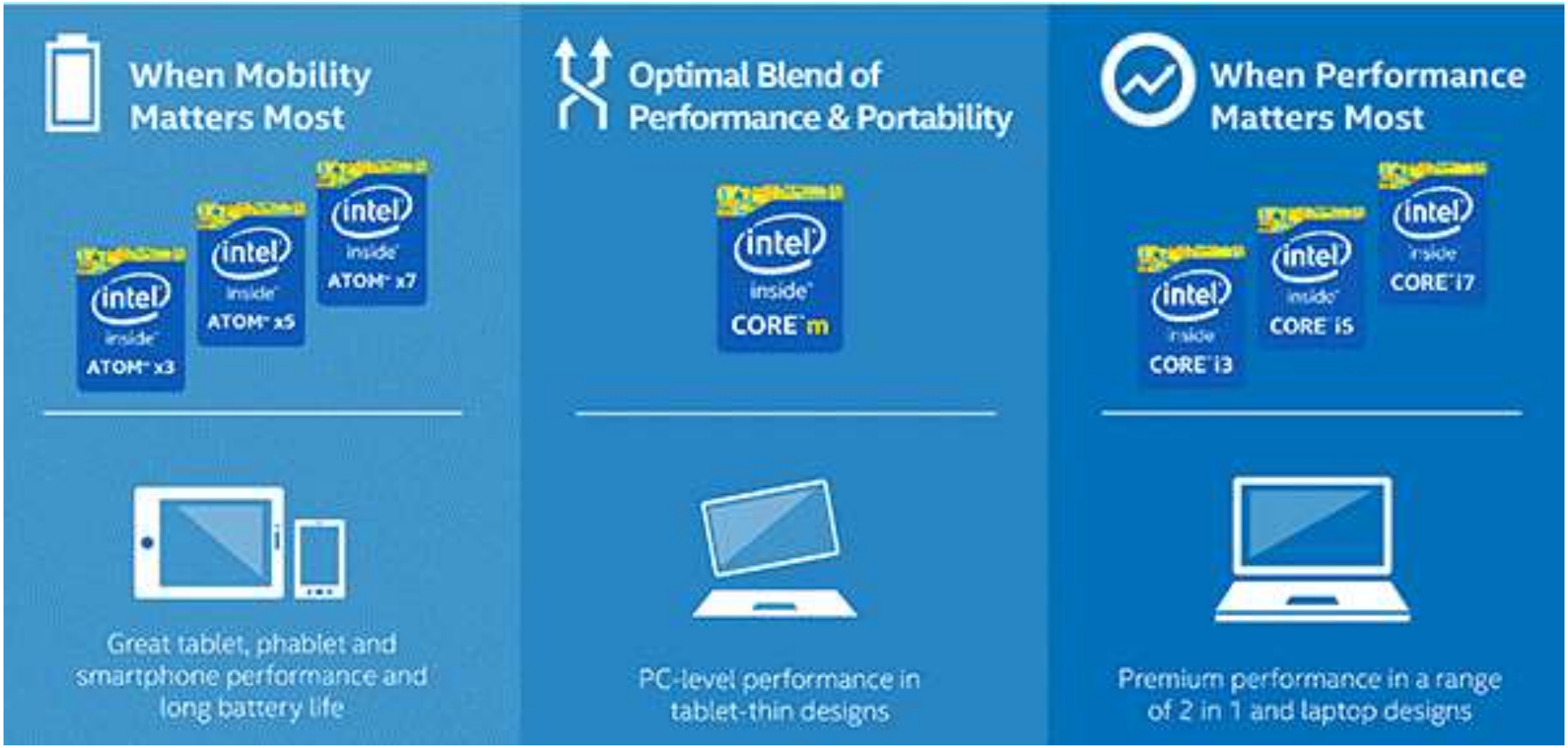


Figure: Intel's new classification of their Atom models [184]

5.3.3 The SoFIA (aka x3) platform (4)

Introducing the first x3 (aka SoFIA) models in 03/2015 [185]

Intel Atom x3-C3130

Intel® Atom™ processor with dual-core, 64-bit and low-power 3G modem

Intel Atom x3-C323XRK

Intel Atom processor with quad-core, 64-bit and low-power 3G modem

Partnership with Rockchip

Intel Atom x3-C344X

Intel Atom processor with quad-core, 64-bit and world – class LTE modem

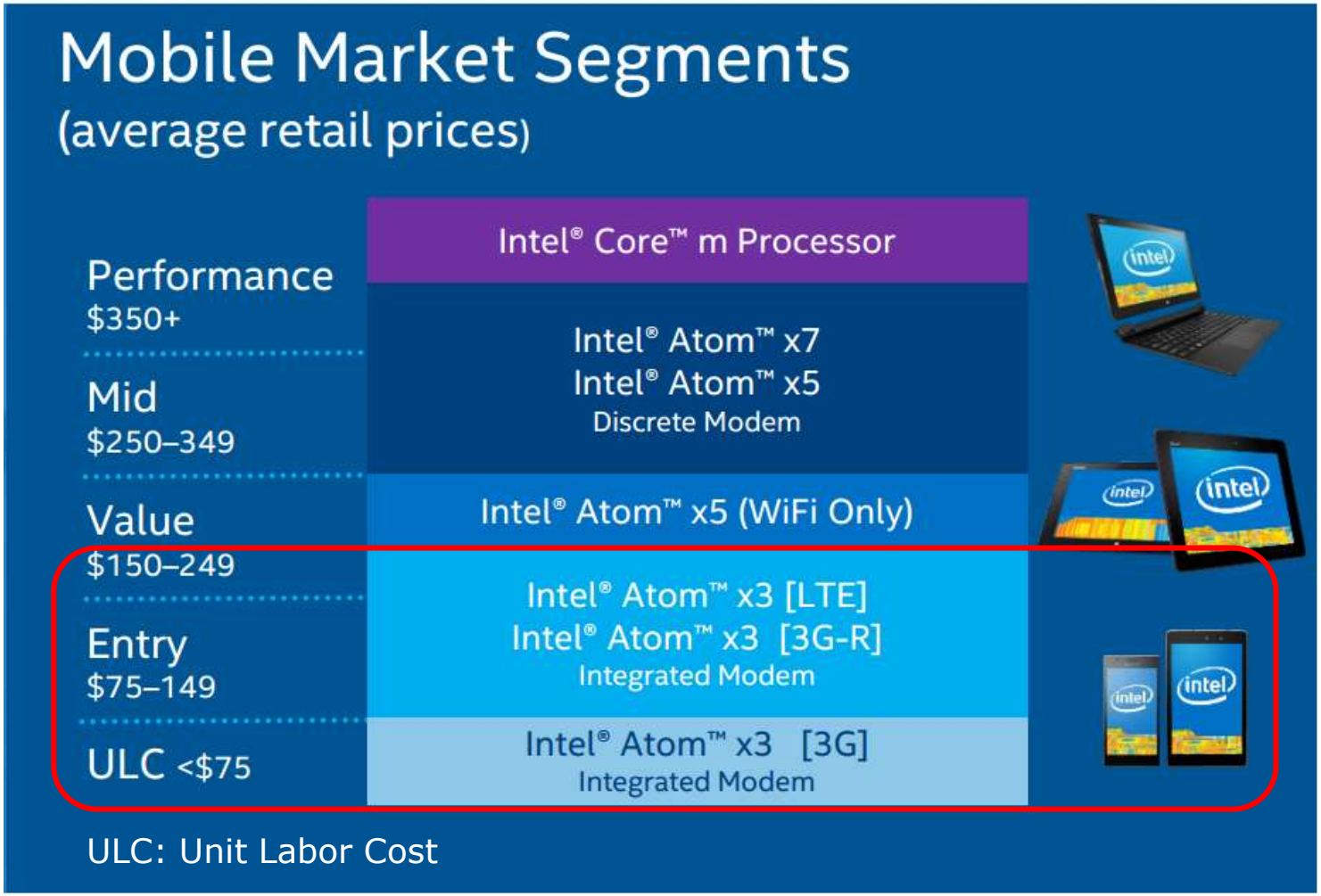
Note that the quad-core 3G model has been developed in partnership with Rockchip.

Remarks

- The x5 and x7 series were previously designated as Cherry Trail processors.
- They were Intel's first Atom chips manufactured on the 14nm process.

5.3.3 The SoFIA (aka x3) platform (5)

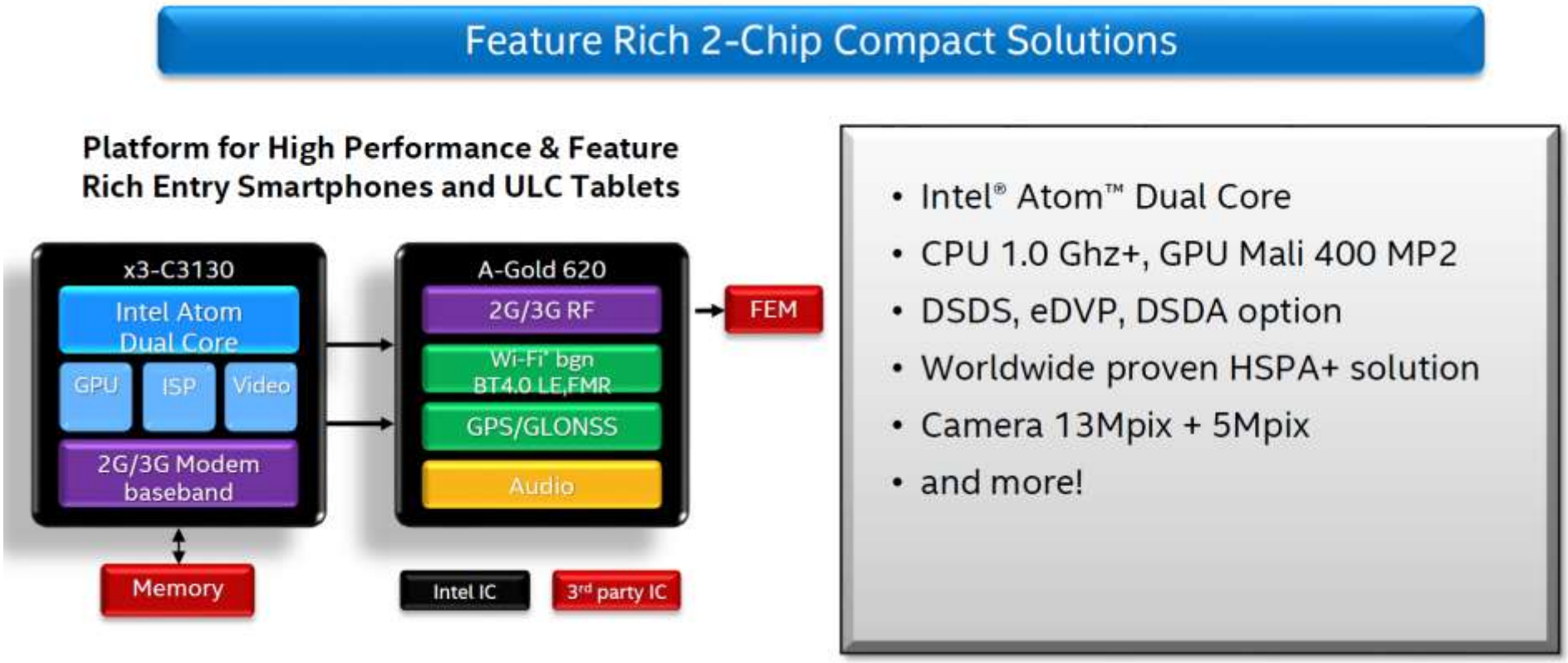
Positioning Intel's x3 (SoFIA) processors in the mobile market segments [169]



Note that the x3 models target very low priced or entry level smartphones.

5.3.3 The SoFIA (aka x3) platform (6)

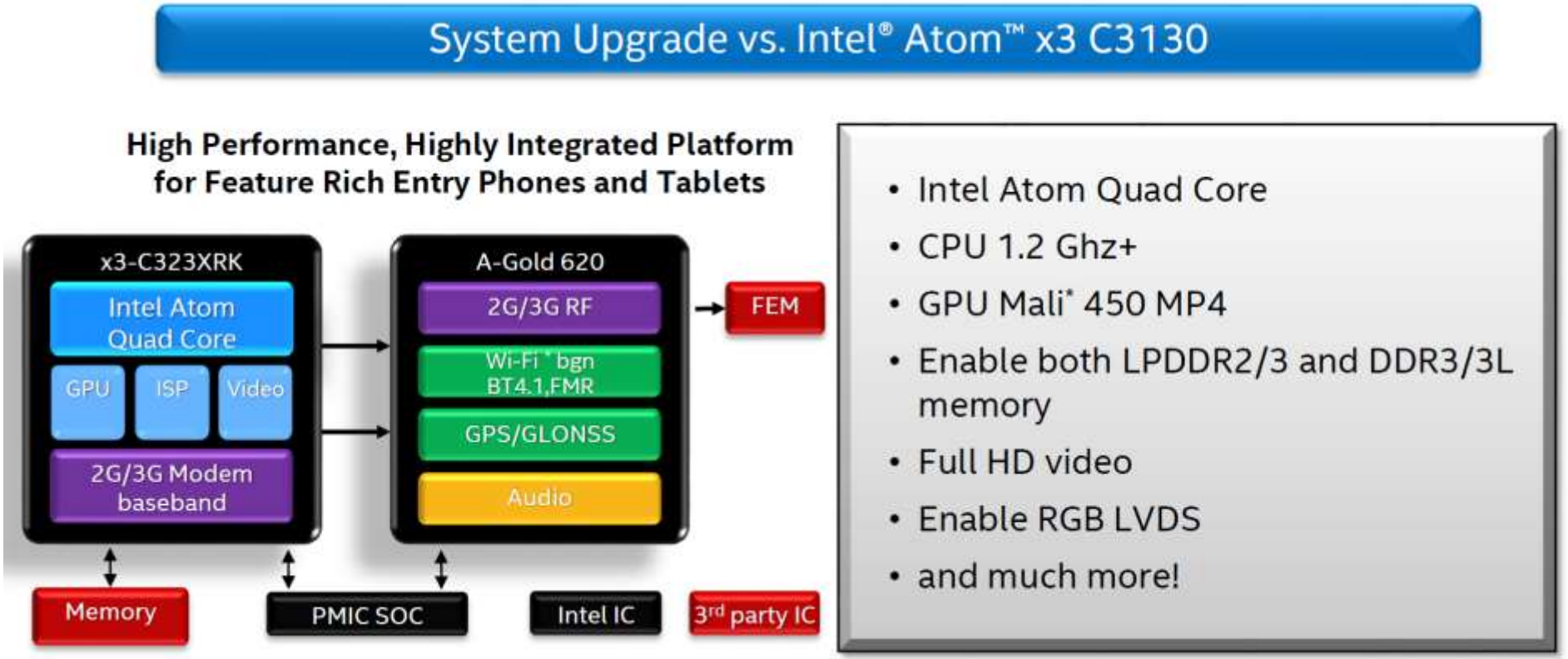
Main functional blocks and features of the x3-C3130 processor model [185]



- Note that this model has dual cores and includes a 2G/3G baseband modem.
- The companion chip (A-Gold 620) implements the RF parts.

5.3.3 The SoFIA (aka x3) platform (7)

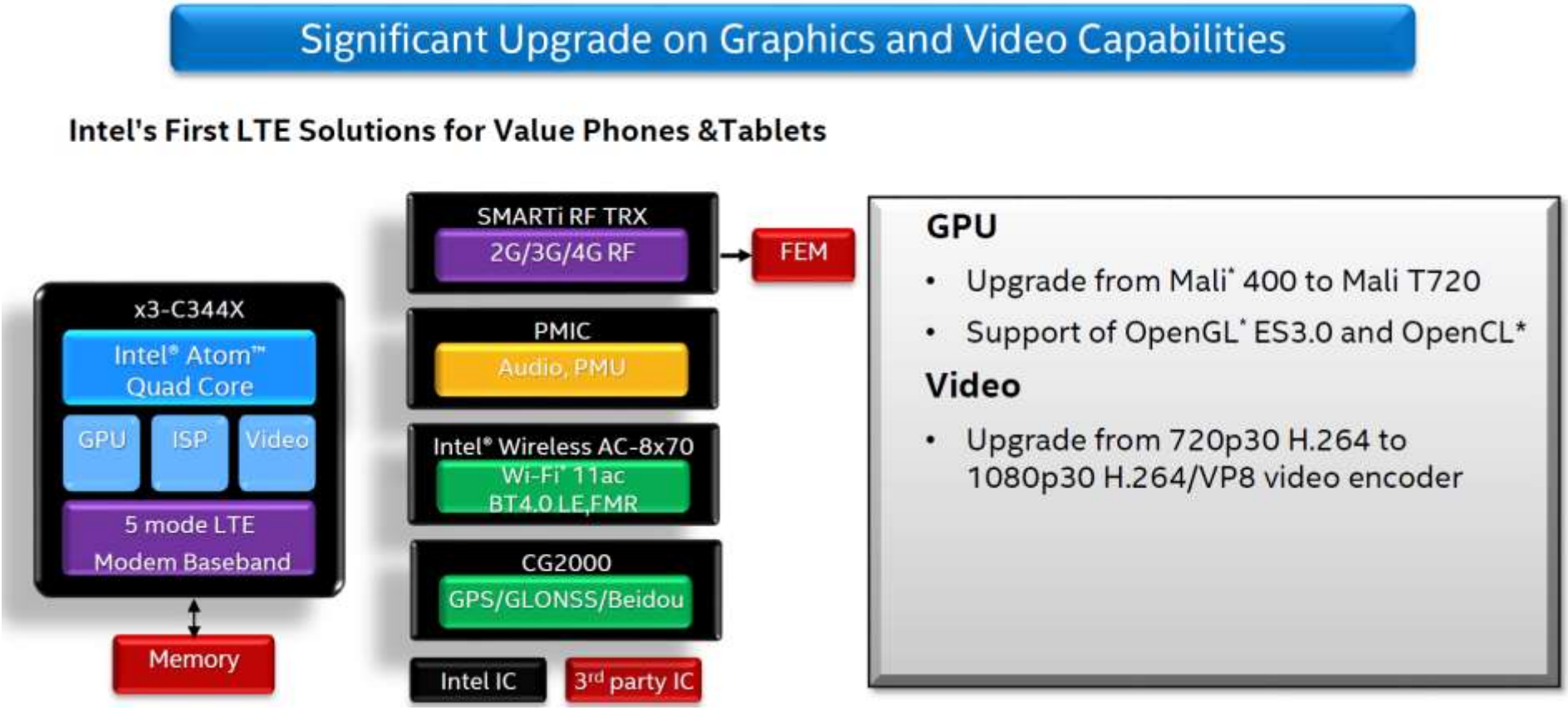
Main functional blocks and features of the x3-C3230 processor model [185]



- Note that this model has quad-cores and includes a 2G/3G baseband modem.
- The companion chip (A-Gold 620) implements the RF parts.
- This processor has been developed in partnership with Rockwell.
- We note also that Rockchip has been working with Intel also to develop a 7-inch reference platform based on the C3230RK processor and running under Android 5.1 with a very low selling price of $45 in quantities of 1000-5000 [186].

5.3.3 The SoFIA (aka x3) platform (8)

Main functional blocks and features of the x3-C344x processor model [185]



- Note that this model has quad-cores and includes a 4G baseband modem.
- In this case four companion chips are needed to implement the RF parts.

5.3.3 The SoFIA (aka x3) platform (9)

Main features of the first introduced x3 (SoFIA) processors [185]

Specifications	Intel® Atom™ x3-C3130 (3G)	Intel Atom x3-C323XRK (3G)	Intel Atom x3-C344X (LTE)
CPU	Dual core 64-bit Atom x3 Up to 1.0 GHz	Quad core 64-bit Atom x3 Up to1.2 GHz	Quad core 64-bit Atom x3 Up to 1.4 GHz [1]
Processor	28nm	28nm	28nm
Graphics (GPU)	Mali* 400 MP2 OpenGL* ES 2.0	Mali 450 MP4 OpenGL ES2.0	Mali T720 MP2 OpenGL ES3.0 & DirectX9.3, OpenCL*
Media (Encode/Decode)	Encode: H.264 @720p30 Decode: H.264, VP8 @ 1080p30	Encode:H.264, VP8@1080p30 Decode: H.264, VP8@ up to 1080p60 HEVC (H.265) @ up to 1080p60	Encode: H.264, VP8@1080p30 Decode: H.264, VP8@1080p30 VP9/H.265 (SW) Decoder
Memory	1x32 LPDDR2 800	1x32 LPDDR2/3 1066, DDR3/DDR3L 2x16 1333	1x32 LPDDR2/3 1066
Display Resolution	1280x800@60fps	Up to 1920x 1080 @60fps	1280x800@60 fps 1920x1080>30 fps
MODEM (Integrated)	GSM/GPRS/EDGE , HSPA+ 21/5.8, DSDS, eDvP	GSM/GPRS/EDGE , HSPA+ 21/5.8, DSDS, eDvP	GSM/GPRS/EDGE DC-HSPA+ 42/11, TD-SCDMA FDD/TDD LTE Cat4→Cat 6
Connectivity	Wi-Fi* 802.11bgn, Bluetooth® 4.0 LE, GPS & GLONASS, FM Radio	Wi-Fi* 802.11bgn, BT 4.0 LE, GPS & GLONASS, FM Radio	Wi-Fi* 802.11ac, BT4.1 LE, GPS, GLONASS & Beidou, FM Radio Near Field Communications (optional feature)
Input Output	UART/SPI, I2C, I2S, SDIO	UART/SPI, I2C, I2S, SDIO	UART/SPI, I2C, I2S, SDIO
USB	USB 2.0 HS	USB 2.0 HS	USB 2.0 HS
Storage	eMMC 4.41	eMMC 4.51	eMMC 4.51
ISP / Camera (rear/front)	Up to 13MP/ 5MP	Up to 13MP/ 5MP	Up to 13MP/ 5MP

[1]Intel® Atom™ x3-C344X processor max sustained clock frequency is 1.2 GHz for all four cores. Burst Mode enables up to a max clock frequency of 1.4 GHz for relatively short peak loads for max 2 CPU cores simultaneously within specific temperature ranges. Availability and frequency of Burst Mode varies depending on, but not limited to, type of workload, hardware, software, number of active cores, power consumption, processor temperature, and system configuration as determined by your device OEM. For details on specific implementations depending on device configuration, please refer to your device manufacturers specifications.

5.3.3 The SoFIA (aka x3) platform (10)

Main features of the first and subsequently introduced x3 (SoFIA) processors [187]

Atom x3 Microprocessors								
Main processor							IGP	
Model	CPU μarch.	Launched	Core count	SDP	Max. Turbo clock	Max mem. size	Name	Base clock
x3-C3130	Silvermont	4 March 2015	2		1.0 GHz	1.0 GB	Mali-400 MP2	480 MHz
x3-C3200RK	Silvermont	4 March 2015	4	2 W	1.1 GHz	2.0 GB	Mali-450 MP4	600 MHz
x3-C3230RK	Silvermont	4 March 2015	4	2 W	1.1 GHz	2.0 GB	Mali-450 MP4	600 MHz
x3-C3405	Silvermont	April 2015	4	2 W	1.4 GHz	2.0 GB	Mali T720 MP2	456 MHz
x3-C3445	Silvermont	April 2015	4	2 W	1.4 GHz	2.0 GB	Mali T720 MP2	456 MHz

SDP: Scenario Design Power (typical power consumption)
RK: Developed in partnership with Rockchip

5.3.3 The SoFIA (aka x3) platform (11)

Main features of the SoFIA (aka x3 3G/LTE) low-cost oriented platform

Platform	Lexington	SoFIA (x3 3G/LTE)
Available	01/2013 (CES)	03/2015
Focus	Value smartphones	Value smartphone
AP processor	Penwell	x3
Models	Z2420	x3-C31xx/C32xxC34xx
Technology	32nm	28 nm (by TSMC)
Die size		
No. of trans.		
CPU micro-arch.	Saltwell	Silvermont
32/64-bit	32-bit	64-bit
No. of cores	1	2/4
HT	HT	no
fc [GHz] (Turbo up to)	1.2	1.4
L2	512 kB	1 MB/2 cores
Mem. channels	Dual mem. ch. MC on proc. die	Single 32-bit mem. ch. MC on proc. die
Memory up to	LPDDR2-800 POP	DDR2/3-1066 DDR3/3L-1333
GPU	Power VR SGX 540	Mali 400/450/T720
DX	DX 9	DX9?
Camera res.	8 Mpixel	13 Mpixel
GPU clock up to	400 MHz	600 MHz
FSB	—	--
Proc. SDP		2 W
ISP	ISP	ISP
Security Engine	Security Engine	
Baseband modem	No, XMM 6265 (3G) comp. chip	Yes, 3G or LTE
Socket	BGA 617	BGA361
Platform Controller Hub	—	--
OS at introduction	Android 4.0.4	Android 4.4
Smartphone examples	Acer Liquid C1 Lava Xolo X500 Safaricom Yolo	

5.3.3 The SoFIA (aka x3) platform (12)

Remark -1

- A leaked internal roadmap from Q2/2013 revealed that Intel planned two low-cost oriented platforms with integrated 3G and 4G modems, respectively, called Slayton and Riverton [145].
- Main features of these platforms were:

Key features	Slayton	Riverton
Technology	22 nm	14 nm
CPU µarch.	Silvermont	Airmont
Core count	2	2
Integrated modem	3G (HSPA+)	4G (LTE)
Companion RF chip	A-GOLD 620	
Max. turbo clock	1.2 GHz	1.6 GHz
Status	In-development	In-planning
Target OS	Android	Android
To be launched	Q4/2014	Na.

Table: Main features of the planned Slayton and Riverton platforms [145]

5.3.3 The SoFIA (aka x3) platform (13)

Remark -2

- Both platforms vanished from later roadmaps probably in connection with the Rockchip agreement, nevertheless became replaced by the SoFIA platform.
- The Slayton processor that was already in development in Q2/2013 became the x3-C3130 model whereas the Riverton processor was basically re-designed by substituting the planned Airmont microarchitecture by the preceding Silvermont microarchitecture and implementing 4 cores instead of the targeted 2.
- Further on, also the planned 22 nm technology was changed to 28 nm and instead of in-house fabrication all x3 chips were produced externally by TSMC.

5.3.4 The Slayton and Riverton platforms

5.3.4 The Slayton and Riverton platforms -1

- A leaked internal roadmap from Q2/2013 revealed that Intel planned two low-cost oriented platforms, with integrated 3G and 4G modems, respectively, called the Slayton and Riverton platforms, with the following features [145]:

Key features	Slayton	Riverton
Technology	22 nm	14 nm
CPU µarch.	Silvermont	Airmont
Core count	2	2
Integrated modem	3G (HSPA+)	4G (LTE)
Companion RF chip	A-GOLD 620	
Max. turbo clock	1.2 GHz	1.6 GHz
Status	In-development	In-planning
Target OS	Android	Android
To be launched	Q4/2014	Na.

Table: Main features of the planned Slayton and Riverton platforms [145]

5.3.4 The Slayton and Riverton platforms (2)

The Slayton and Riverton platforms -2

Intel replaced the Slayton and Riverton processors by the x3 (SoFIA line) that provided more or less the same features as the previously planned processors, presumable in connection with their strategic agreement entered with the Chinese semiconductor manufacturer Rockchip aiming at developing and selling very low priced application processors with integrated modems.

6. Intel’s withdrawal from the mobile market

6. Intel's withdrawal from the mobile market (1)

6. Intel's withdrawal from the mobile market

Intel's worldwide market share in smartphone application processors in 1H2017 [175]

(revenue based) [175]

Vendor	Market share	Processor lines (examples)	ISA
Qualcomm (USA)	42 %	Snapdragon line 200-805 Snapdragoon 808-845	ARMv7 ARMv8
Apple (USA)	18 %	Apple A4-A6X Apple A7-A11	ARMv7 ARMv8
MediaTek (Taiwan)	18 %	Helio x10 Helio X20	ARMv7 ARMv8
Samsung (S. Korea)		Exynos 5 line Exynos 7/8/9	ARMv7 ARMv8

[Source: Strategy Analytics]

ARMv7: 32-bit
ARMv8: 64-bit

- As the table shows Intel is not among the first five leading vendors in selling smartphone processors.
- Industry sources indicate that e.g. in 2014 Intel achieved only less than 1 % share in smartphone application processor revenue [177].

6. Intel's withdrawal from the mobile market (2)

Intel's worldwide market share in tablet application processors [190], [191], [192]

Subsidies paid by Intel for OEMs

- In the first years of 2010 Intel paid significant subsidies (~ 50 $/tablet) to notebook and tablet manufacturers to inspire their switch from ARM based processors to x86 Atom processors.

Obtained market share in 2015 due to paying subsidies

- In 2015 Intel achieved the 3. place in the worldwide market share in tablet application processor revenue, as the Table below shows.

Tablet application processors worldwide market share 2015 (revenue) [193]	
Apple (USA)	28 %
Qualcomm (USA)	19 %
Intel (USA)	16 %
MediaTek (Taiwan)	
Samsung (S. Korea)	

Table: Worldwide market share of application processors used in tablets in 2015 (based on revenue) [193]

Subsidy: szubvenció

*

6. Intel’s withdrawal from the mobile market (3)

Intel's losses in the mobile market segment in 2013 - 2014

Owing to subsidies Intel's mobile and communication division has lost 7 billion $ in the years 2013-2014 , as indicated in the next Figure [188].

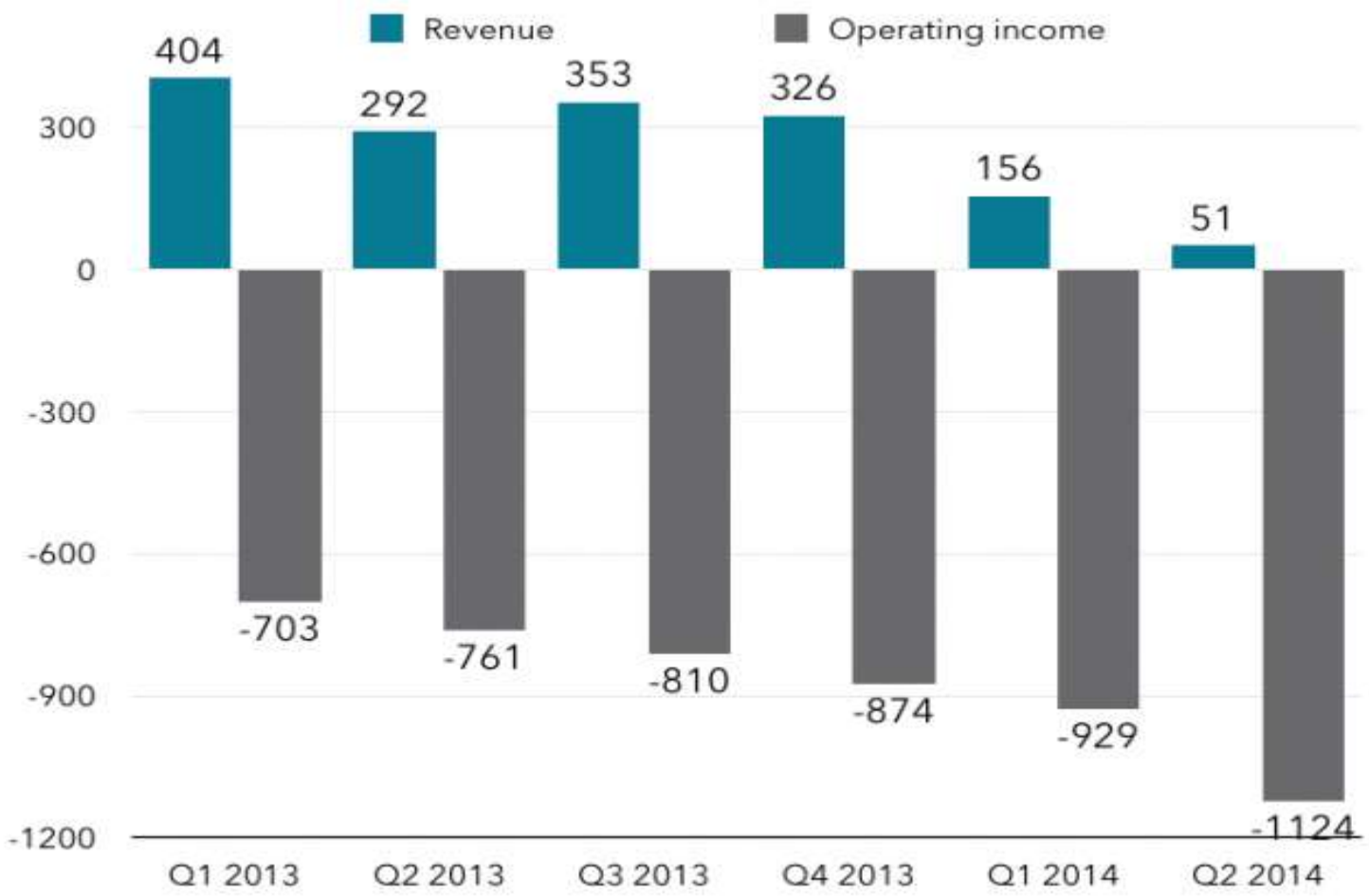


Figure: Revenues/operating income of Intel's Mobile and Communications segment [188]

6. Intel’s withdrawal from the mobile market (4)

Intel's withdrawal from the smartphone and mobil market

- As Intel failed to gain traction in the mobile sector and suffered high losses on the mobile segment the firm announced their withdrawal from the mobil market in 4/2016.
- Intel's statement says [169]:

"I can confirm that the changes included canceling the Broxton platform as well as SoFIA 3GX, SoFIA LTE and SoFIA LTE2 commercial platforms to enable us to move resources to products that deliver higher returns and advance our strategy.

These changes are effective immediately."

- At the same time Intel laid off about 12000 employees (~ 11 % of their workforce).

6. Intel’s withdrawal from the mobile market (5)

NVidia's leaving the smartphone and tablet market in June 2016 [189]

- NVIDIA’s Tegra 4 chips were also not successful, so the firm announced in 05/2014 that they will abandon the phone market.

  Apple’s iPad Air 2 with its A8X processor and its GPU with 256 EUs became a very powerful rival to NVIDIA's subsequent 64-bit K1 chip including a GPU with 192 EUs.

  As a consequence, NVIDIA also gave up their tablet interests.

- In 6/2016 (at Computex) NVIDIA's CEO declared the firm's leaving the smartphone and tablet market by saying:

  “We are no longer interested in that market”. He adds, “Anybody can build smartphones, and we’re happy to enjoy these devices, but we’ll let someone else build them”.

- Instead NVIDIA became interested in designing in-car computers and car infotainment systems.

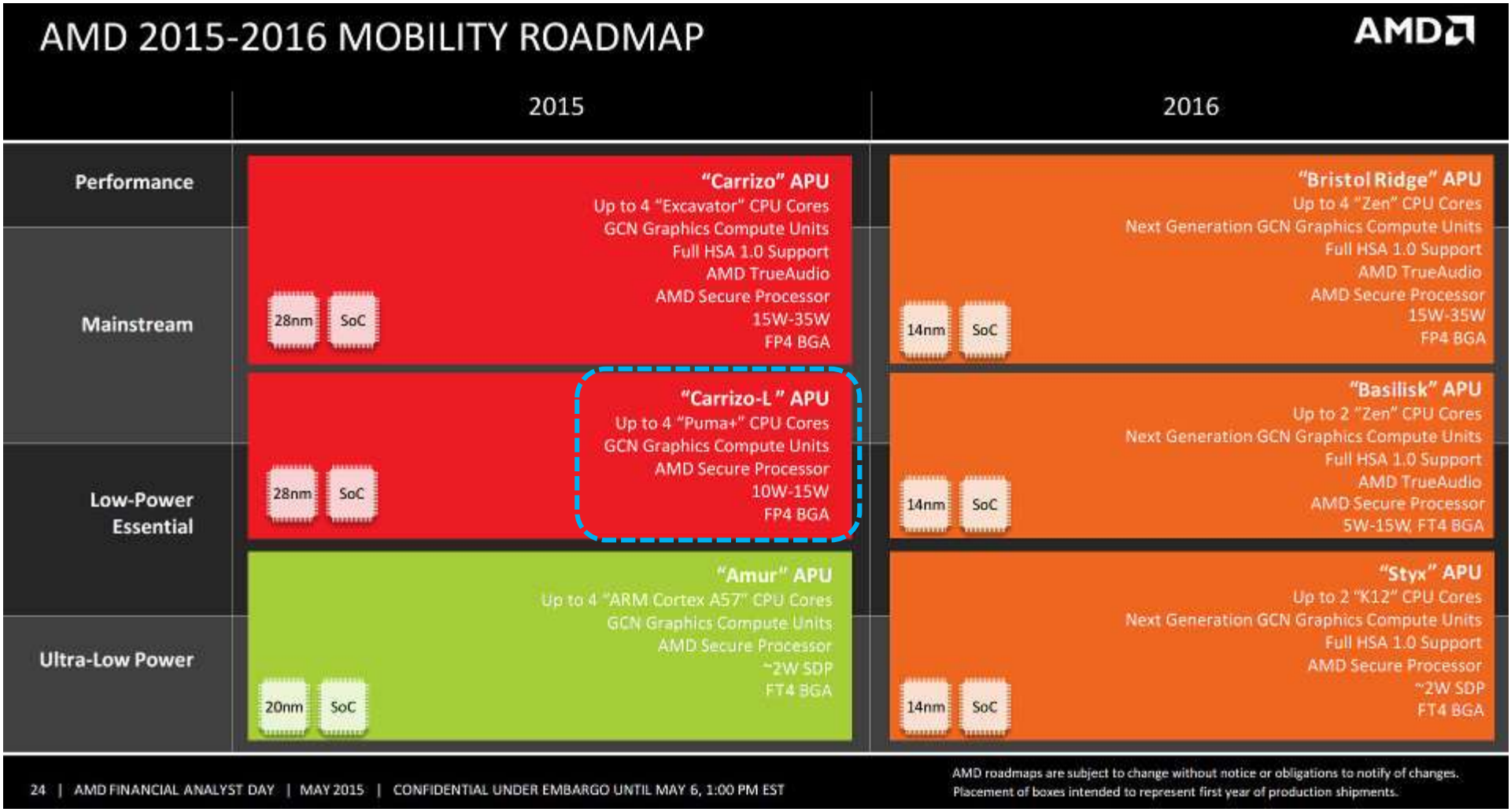
6. Intel’s withdrawal from the mobile market (6)

Cancellation of AMD's low-power Cat line in 2015

- Neither Intel nor AMD became successful on the mobile market, so beyond Intel also AMD stopped their activities on this market.
- The last core of AMD's Cat line was the Puma+ core (launched in 6/2015 in the Carrizo-L APU).
- In AMD's 2016 Mobility roadmap there is no sign of an APU powered by the Puma+ core or a derivative of a core belonging to the Cat line, as seen in the next slice.
- Instead AMD placed emphasis on the development of Zen core based products.

6. Intel's withdrawal from the mobile market (7)

AMD's 2015-2016 mobility roadmap revealed at Financial Analyst Day May 6 2015 [146]



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