

Sima Dezsó

List of publications and references

A Books (in English)

A2 Sima D., Fountain T. and Kacsuk P., “*Advanced Computer Architectures, A Design Space Approach*,” Addison-Wesley Kiadó, Harlow, etc., 1997, 1998, 2000, 766 pages, Tata McGraw-Hill, New Delhi 2003, Kindersly (India) 2006

A2-c153 Zhang X. D., Yeager K. C., “Method and system for renaming registers in a microprocessor,” *US Patent 7406587*, 2008

A2-c152 Yoshida, T., “Processor for executing instruction control in accordance with dynamic pipeline scheduling and a method thereof,” *US Patent 7337304*, 2008.

A2-c151 Wilson S., “Processor instruction with repeated execution code,” *US Patent 7346763*, 2008.

A2-c150 Slogsnat D. C., „*Tightly-Coupled and Fault-Tolerant Communication in Parallel Systems*,” PhD Thesis, Universität Mannheim, 2008, pp. 1-218

A2-c149 Ramdas T., Egan G., Abramson D., Baldrige K., „Towards a special-purpose computer for Hartree-Fock computations,” *Theor Chem Account*, Springer-Verlag 2008, pp. 133-153

A2-c148 Lee J-H., Cho K-R., „Design of a high performance self-timed ARM9 processor,” *IEICE Electronics Express*, Vol. 5 2008, No. 3 pp. 87-93

A2-c147 Wilson S., “Microprocessor with high speed memory integrated in load/store unit to efficiently perform scatter and gather operation,” *US Patent 7216218*, 2007.

A2-c146 Su Y-H., Liu J., Chen J., „Hardware Loop Buffer Design for Low-Power VLIW DSP Processors,” *Chinese Journal of Electron Devices*, Issue 5, 2007, pp. 1866-1869, 1873

A2-c145 Ramdas T., Egan G., Abramson D., Baldrige K., „Converting Massive TLP to DLP: a Special-Purpose Processor for Molecular Orbital Computations,” *Proc. of the 4th International Conference on Computing Frontiers*, Ischia, Italy, 2007, pp. 267-276

A2-c144 Pomante L., Di Felice P., Paolino, “A System-Level HW/SW Co-Design Methodology for Ad-Hoc Implementation of DMBS Operators,” *WSEAS Transactions on Computers Research*, Vol. 2, No. 2, 2007, pp. 298-304.

- A2-c143 Bandyopadhyay S., “Dissemination of Information in Optical Networks: From Technology to Algorithm,” *Springer*, 2007, 250 pages.
- A2-c142 Pomante L., Di Felice P., “Ad-hoc HW/SW architectures for DBMSs: a co-design approach,” *Proc. of the 6th Conference on 6th WSEAS International Conference on Artificial Intelligence*, Knowledge Engineering and Data Bases Vol. 6, 2007, pp. 153-158.
- A2-c141 Lee J-H., Lee S-S., Cho K-R., „Asynchronous ARM Processor Employing an Adaptive Pipeline Architecture,” *Proc. ARC 2007 In: LNCS 4419*, Springer-Verlag, Berlin, Heidelberg, 2007, pp. 39-48
- A2-c140 Lee S-S., Lee J-H., Lim Y., Cho K-R., “Adaptive Pipeline Architecture for an Asynchronous Embedded Processor,” *Journal of the Institute of Electronics Engineers of Korea*, Vol. 44, Issue 1, 2007, pp. 51-58
- A2-c139 Jung E.G., Lee J.G., Jhang K.S., Lee J.A., Har D., „Asynchronous Layered Interface of Multimedia SoCs for Multiple Outstanding Transactions,” *The Journal of VLSI Signal Processing*, Springer, Vol. 46, No. 2-3, 2007, pp. 133-151.
- A2-c138 Je-Hoon L., Seung-Sook L., Kyoung-Rok C., “Asynchronous ARM Processor Employing and Adaptive Pipeline Architecture,” *Lecture Notes in Computer Science*, Springer, Vol. 4419/2007, pp. 39-48.
- A2-c137 Tutsch D., “Performance Analysis of Network Architectures,” *Springer-Verlag*, 2006, 244 pages.
- A2-c136 Timothy J, “*Compiler-Directed Energy Savings in Superscalar Processors*,” Doctoral Thesis, University of Edinburgh, 2006, pp. 1-155.
- A2-c135 Panis C., Leitner, R., “Programmable unit with a stack buffer storage device configurable into discrete shadow storage elements accessible by a plurality of command execution units,” *US Patent 7124288*, 2006.
- A2-c134 Lozano M., Morillo P., Orduna J. M., Cavero V., „On the Design of a Scalable Architecture for Crowd Simulation,” *XVII Jornadas De Paralelismo – Albacete*, 2006, pp. 1-6
- A2-c133 Laskowski E, Tudruj M., “Scheduling Programs with Conditional Branches for Look-Ahead Dynamically Reconfigurable Systems,” *Proc. 14th Euromicro International Conference on Parallel, Distributed and Network-Based Processing (PDP’06)*, 2006, pp. 211-218.
- A2-c132 Jones T. M., „*Compiler-Directed Energy Savings in Superscalar Processors*,” PhD Thesis, University of Edinburgh, 2006, pp. 1-155
- A2-c131 Ivanov L., “A modern course on parallel and distributed processing,” *Proc. Consortium for Computing Sciences in Colleges*, 2006, pp. 29-38.

- A2-c130 De Florio V., and Blondia C., "The algorithm of pipelined gossiping," *Journal of Systems Architecture*, Vol. 52, Issue 4, April 2006, pp. 235-256.
- A2-c129 Zhou P., Önder S., Carr S., "Fast Branch Misprediction Recovery in Out-of-order Superscalar Processors," *Proc. 19th ACM International Conference on Supercomputing, (ICS'05)*, 2005, Cambridge, USA, pp. 1-10.
- A2-c128 Vokorokos L., Ádám N., Baláz A., "Paralelization of the Sequential Threads in DF Computers," *Proc. 3rd Slovakian-Hungarian Joint Symposium on Applied Machine Intelligence (SAMI'05)*, 2005, pp. 1-9.
- A2-c127 Vega-Rodríguez M. A., Jorge Gil-Ramos R., Gómez-Pulido J. A., Sánchez-Pérez J. M., "A versatile simulator for cache memories on dsm systems," *Proc. 19th European Conference on Modelling and Simulation (ECMS'05)*, pp. 1-8.
- A2-c126 Vega-Rodríguez M. A., Gutiérrez-Gil R., Ávila-Román J. M., Sánchez-Pérez J. M., Gomez-Pulido J. A., "Genetic Algorithms Using Parallelism and FPGAs: The TSP as Case Study," *Proc. of the International Conference on Parallel Processing Workshop (ICPPW'05)*, 2005, pages 1-7.
- A2-c125 Yi J. J., Lilja D. J., Hawkins D. M., "Improving Computer Architecture Simulation Methodology by Adding Statistical Rigor," *IEEE Transactions on Computers*, Vol. 54, No. 11, November 2005, pp. 1360-1373.
- A2-c124 Ayala Rodrigo J. L., "Power estimation and power optimization policies for processor-based systems," PhD Thesis, Universidad Politécnica de Madrid, 2005, pp. 1-159.
- A2-c123 Níyonkuru A., "Zum Einsatz von rekonfigurierbarer Hardware in Prozessorarchitekturen," Dissertation, Helmut-Schmidt-Universität/Universität der Bundeswehr Hamburg, 2005, pp. 1-139.
- A2-c122 Min G., Oul-Khaoua M., "Prediction of communication delay in torus networks under multiple time-scale correlated traffic," *Performance Evaluation*, Vol. 60, Issue 1-4, May 2005, pp. 255-273.
- A2-c121 Kim S., Vijaykrihnan N., Kandemir M. and Irwin M. J., "Exploiting temporal loads for low latency and high bandwidth memory," *IEE Proc. Computer and Digital Techniques*, Vol. 152, No. 4., July 2005, pp. 457-466.
- A2-c120 Kadayif I., Sivasubramaniam A., Kandemir M., Kandiraju G., Chen G., "Optimizing Instruction TLB Energy Using Software and Hardware Techniques," *ACM Transaction on Design Automation of Electronic Systems*, Vol. 10. No. 2, April 2005, pp. 229-257.

- A2-c119 Chan S., “*Architectures for a Space-Based Information Network with Shared On-Orbit Processing*,” PhD Thesis, Massachusetts Institute of Technology, 2005, ppl. 1-343.
- A2-c118 Tudruj M., Masko L., “Communication on the Fly in Dinamic SMP Clusters – Towards Efficient Fine Grain Numerical Computations,” *Proc. Parallel Processing and Applied Mathematics, 5th International Conference, (PPAM 2003)*, in LNCS 3019, Springer Verlag, 2004, pp. 59-68.
- A2-c117 Sekanina L., “Evolvable Components: From Theory to Hardware Implementations,” *Springer* 2004, 194 pages.
- A2-c116 Popa T.S., “*Compiling Data Dependent Control Flow on SIMD GPUs*,” PhD Thesis, the University of Waterloo, 2004, 98 pages.
- A2-c115 Panis C., Hirschrott U., Laure G., Lazian W., Nurmi J., “DSPxPlore: design space exploration methodology for an embedded DSP core,” *Proc. of the 2004 ACM Symposium and Applied Computing*, Cyprus, 2004, pp. 876-883.
- A2-c114 Panis C., Hirschrott U., Ferfeleder S., Krall A., Laure G., Lazian W., Nurmi J., “A scalable embedded DSP core for SoC applications,” *Proc. International Symposium*, 2004, pages 85-88.
- A2-c113 Panis C., Grunbacheer H., Nurmi J., “A scalable instruction buffer and align unit for xDSPcore,” *Solid-state Circuits*, Vol. 39, Issue 7, 2004, pp. 1094-1100.
- A2-c112 Munoz A. J. C., “*Optimización Automática de Software Paralelo de Álgebra Lineal*,” Tesis Doctoral, Universidad de Murcia, Departamento de Ingeniería y Tecnología de Computadores, 2004, pp. 1-200.
- A2-c111 Moore R. C., “Method and apparatus for utilizing renamed registers based upon a functional or defective operational status of the register,” United States Patent No.6 748 519, *IBM*, June 8, 2004. pp. 1-14.
- A2-c110 Misev A., Gusev M., “Visual simulator for ILP dynamic OOO processor,” *Proc. 31st International Symposium on Computer Architecture*, Munich, Germany, 2004, pp. 1-6.
- A2-c109 Michaud P., “Exploiting the Cache Capacity of a Single-Chip Multi-Core Processor with Execution Migration,” *Proc. 10th International Symposium on High Performance Computer Architecture*, 2004, pp. 1-10.
- A2-c108 Lazarov V. and Marinova M., “Dependencies Evaluation in Superscalar Processors,” *Proc. CompSysTech’2004*, 2004, pp. 1.3-1 - 1.3-4.

- A2-c107 Kroeger R., "Admission Control for Independently-authored Realtime Applications," PhD Thesis, University of Waterloo, 2004, pp. 1-236.
- A2-c106 Hlope H, Changelain D, Van Wyk BJ, "Dotta: A Dynamic VLIW-like Architecture for High Speed Parallel Computing," *Proc. 7th AFRICON Conference (AFRICON 2004)*, Gaborone, Botswana, 2004, pp. 526-557.
- A2-c105 Cohen A. A., "Adressing architecture for Brain-like Massively Parallel Computers," *Proc. EUROMICRO Systems on Digital System Design (DSD'04)*, 2004, pp. 594-597.
- A2-c104 Chang-Yong H., in-Pyo H. Yon-Srk L., "Implementation of a Scoreboard Array and a Port Arbiter for in-order SMT Processors," *Journal of the Institute of Engineers of Korea*, Semiconductor and devices, Vol. 4.1, Issue 6., 2004, pp. 59-70.
- A2-c103 Castilla I., Moreno L., Sigut J., González C., González E.J., "SIMDE: Un Simulador para el Apoyo Docente en la Enseñanza de las Arquitecturas ILP con Planificación Dinámica y Estática," *Jornadas de Enseñanza Universitaria de la Informática*, Vol. 10, 2004, pp. 505-508.
- A2-c102 Ayala J. L. and López-Vallejo M., "Improving Register File Banking with a Power Aware Unroller," *Proc. Workshop on Power-Aware Real-Time Computing (in conjunction with ACM International Conference on Embedded Software)*, September 2004, pp. 1-6.
- A2-c101 Yi J. J., Lilja D. J. and Hawkins D. M., "A Statistically Rigorous Approach for Improving Simulation Methodology," *Proc. 9th International Symposium on High Performance Computer Architecture (HPCA-9)*, 2003, pp. 1-15.
- A2-c100 Yi Joshua J., "Improving Processor Performance and Simulation Methodology," PhD Thesis, The University of Minnesota, 2003, pp. 1-143.
- A2-c99 Tudruj M. and Masko L., "Communication on the Fly and Program Execution Control in a System of Dinamically Configurable SMP Clusters," *Proc. 11th Euromicro Conference on Parallel, Distributed and Network-Based Processing*, 2003, pp. 67-74.
- A2-c98 Shinichi Y., "Method and system dynamically presenting the branch target address in conditional branch instruction," *US Patent 6662295*, 2003.
- A2-c97 Panis C., Leitner R. and Nurmi J., "Scaleable Shadow Stack for a Configurable DSP Concept," *Proc. 3rd IEEE International Workshop on System-on-Chip for Real-Time Applications (IWSOC'03)*, 2003, pp. 222-227.

- A2-c96 Panis C., Leitner R., Grunbacher H., Nurmi J., “ xLIW – a scaleable long instruction word (DSP applications),” *Proc. 2003 International Symposium on Circuits and Systems, (ISCAS’03)*, Vol. 5, 2003, pp. 69-72.
- A2-c95 Panis C., Laure G., Lazian W., Krall A., Grunbacher H., “DSPXPlore – Design Space Exploration for a Configurable DSP Core,” *Proc. Global Signal Processing Expo (GSPx)*, Dallas, Texas, USA 2003, pp. 1-6.
- A2-c94 Panis C., Bramberger M., Grünbacher H., Nurmi J., “A Scaleable Instruction Buffer for a Configurable DSP Core,” *Proc. 29th European Solid-State Circuits Conference (ESSCIRC 2003)*, Estoril, Portugal, 2003, pp. 1-4.
- A2-c93 Moore, C. R., “Microprocessor instruction buffer redundancy scheme,” *US Patent 6625746*, 2003.
- A2-c92 Lee J-H., Cho K-R., „A New Asynchronous Pipeline Architecture for CISC type Embedded Micro-Controller,” *Journal of the Institute of Electronics Engineers of Korea*, Vol. 40, Issue 4, 2003, pp. 85-94
- A2-c91 Lazarov V., “Effectiveness Evaluation of Parallel Execution of Some Mathematical Methods,” *Lecture Notes in Computer Science, Springer* Vol. 2542/2003, pp. 514-518.
- A2-c90 Kim S., “*Energy-efficient high performance cache architectures*,” PhD Thesis, The Pennsylvania State University, 2003, pp. 1-137.
- A2-c89 Ivanov L., “Hardware Courses and the Undergraduate Computer Science Curriculum at Small Colleges,” *The Journal of Computing in Small Colleges*, vol. 18, No. 3, 2003, pp. 177-184.
- A2-c88 Heo C-Y., Choi K-B., Hong I-P. and Lee Y-S., “An Implementation of Scoreboarding Mechanism for ARM-Based SMT Processor,” *Proc. 5th International Conference on ASIC*, 2003, pp. 443-446.
- A2-c87 Hallberg J., Palm T. and Brorsson M., “Cache-Conscious Allocation of Pointer-Based Data Structures Revisited with HW/SW Prefetching,” *Proc. Second Annual Workshop on Duplicating, Deconstructing, and Debunking (WDDD’03)*, 2003, pp. 2-35.
- A2-c86 El-Kharashi M.W., Pfrimmer J., Li K.F. and Gebali F., “A Design Space Analysis of Java Processors,” *Proc. IEEE Pacific Rim 2003 Conference*, 2003, pp. 159-163.
- A2-c85 Cowell C., Moritz Cs.A. and Burleson W., “Improved Modeling and Data Migration for Dynamic Non-Uniform Cache Accesses,” *Proc. Second Annual Workshop on Duplicating, Deconstructing, and Debunking (WDDD 2003)*, 2003, pp. 1-10.

- A2-c84 Chang-Yong H., Kyu-Baik C. in-Pyo H., Yong-Surk L., "An implementation of scoreboard mechanism for ARM-based SMT processor," *Proc. 5th International Conference on ASIC*, Vol. 1., Issue 21-24., 2003, pp. 443-446.
- A2-c83 Chang-Yong H., "Design of a Register File and a Scoreboard Array for In-order SMT Processors," Phd Thesis, The Graduate School Yonsei University, 2003. 131 pages.
- A2-c82 Cadenas O. and Megson G., "Pullpipelining: A Technique for Systolic Pipelined Circuits," *Proc. 3rd IEEE International Workshop on System-on-Chip for Real-Time Applications (IWSOC'03)*, 2003, pp. 205-210.
- A2-c81 Ayala J.L., López-Vallejo M. and Veidenbaum A., "Energy-Efficient Register Renaming in High Performance Processors," *Proc. IEEE Workshop on Application Specific Processors (in conjunction with IEEE International Symposium on Microarchitecture)*, San Diego, USA, 2003, pp. 1-7.
- A2-c80 Arnal T.M., "Técnicas Hardware para Optimizar el Uso de los Registros en Procesadores Superescalares," Tesis Doctoral, Universidad de Zaragoza, Departamento de Informática e Ingeniería de Sistemas, 2003.
- A2-c79 Tudruj M. and Masko L., "Program Execution Control for Communication on the Fly in Dynamic Shared Memory Processor Clusters," *Proc. International Conference on Parallel Computing in Electrical Engineering (PARELEC'02)*, 2002, pp. 15-20.
- A2-c78 Tudruj M., Masko L., "Task Scheduling for Dynamically Configurable Multiple MSP Clusters Based on Extended DSC Approach," *Proc. Parallel Processing and Applied Mathematics, 4th International Conference, (PPAM 2001)*, in LNCS 2328, Springer Verlag, 2002, pp. 115-124.
- A2-c77 Tudruj M., Masko L., "A Parallel System Architecture Based on Dynamically Configurable Shared Memory Clusters," *Springer*, Vol. 2328/2002, page 51-61.
- A2-c76 Tudruj M., Masko L., "An Architecture and Task Scheduling Algorithm for Systems Based on Dynamically Reconfigurable Shared Memory Clusters," *Proc. International Workshop on Cluster Computing (IWCC 2001)*, in LNCS 2326, Springer Verlag, 2002, pp. 197-206.
- A2-c75 Tudruj M., "Embedded Cluster Computing through Dynamic Reconfigurability of Inter-processor Connections," *Proc. International Workshop on Cluster Computing, (IWCC 2001)*, in LNCS 2326, Springer Verlag, 2002, pp. 77-91.

- A2-c74 Tapus N., Slusanschi E., Popescu T., „Distributed Rendering Engine,” *Proc. IWCC 2001 In: LNCS 2326*, Springer-Verlag, Berlin, Heidelberg, 2002, pp. 207-215
- A2-c73 Roldan M. C., Naiouf M. and De Giusti A, “Parallelizing Tracking Algorithms,” *Journal of Computer Science & Technology*, Vol. 1, No. 6, 2002, pp. 1-13.
- A2-c72 Qian Y., “*Loop transformations for clustered vliw architectures*,” Dissertation for the degree of doctor of philosophy, Michigan Technological University, 2002, pages 1-117.
- A2-c71 Pomante, L., “*System-Level Co-Design of Heterogeneous Multi-processor Embedded Systems*,” PhD Thesis, DEI Politecnico di Milano, 2002.
- A2-c70 Pilz N.A and Adamson K., “Code Optimization Techniques of Data-Intensive Tasks onto Statically Scheduled Architectures: Optimal Performance on the TigerSharc,” *Proc. 6th International Conference (PARA 2002)*, 2002, pp. 172-184.
- A2-c69 Nepomniaschaya A.S., “Associative Parallel Algorithms for Computing Functions Defined on Paths in Trees,” *Proc. International Conference on Parallel Computing in Electrical Engineering (PARELEC’02)*, 2002, pp. 399-404.
- A2-c68 Németh Zs., “Definition of a Parallel Execution Model with Abstract State Machines,” *Acta Cybernetica*, Vol. 15, No. 3, 2002, pp. 417-455.
- A2-c67 Naiouf M. and De Giusti A., “Escalabilidad y Balance de carga en Sistemas Paralelos,” *Proc. IV. Workshop de Investigadores en Ciencias de la Computación (WICC 2002)*, Buenos Aires, Argentina, 2002, pp. 387-390.
- A2-c66 Kadayif I., Sivasubramaniam A., Kandemir M., Kandiraju G. and Chen G., “Generating Physical Addresses Directly for Saving Instruction TLB Energy,” *Proc. 35th Annual International Symposium on Microarchitecture (MICRO-35)*, 2002, pp. 1-12.
- A2-c65 Ismail N. A., “Evaluation of dynamic branch predictors for modern ILP processors,” *Microprocessors and Microsystems*, Vol. 26, No. 5, 2002, pp. 215-231.
- A2-c64 De Giusti A., Naiouf M., Sanz C., Tinetti F., De Giusti L. and Bertone R., “Procesamiento Paralelo y Distribuido en tratamiento masivo de datos,” *Proc. IV. Workshop de Investigadores en Ciencias de la Computación (WICC 2002)*, Buenos Aires, Argentina, 2002, pp. 364-367.

- A2-c63 De Giusti L., Naiouf M. and De Giusti A., “Modelos de predicción de performance en sistemas paralelos,” *Proc. IV. Workshop de Investigadores en Ciencias de la Computación (WICC 2002)*, Buenos Aires, Argentina, 2002, pp. 360-363.
- A2-c62 De Florio V., Deconinck G. and Belmans R., “A Massively Parallel Architecture for Hopfield-Type Neural Network Computers,” *Proc. Massively Parallel Computing Systems (MPCS'02)*, 2002, pp. 14-22.
- A2-c61 Fiedler R., “*Mikroarchitektur eines digitalen Signalprozessors mit Datenflusserweiterung*,” Dissertation, Elektrotechnik und Informationstechnik der Technischen Universität Chemnitz, 2002, pp. 1-182.
- A2-c60 Engblom J., “*Processor Pipelines and Static Worst-Case Execution Time Analysis*,” PhD Thesis, Uppsala University, April 19, 2002.
- A2-c59 Cowell C., Moritz Cs. A. and Burleson W., “Improved Modeling and Data Migration for Dynamic Non-Uniform Cache Accesses,” *Proc. Workshop on Duplicating, Deconstructing, and Debunking (WDDD'02)*, 2002, pp. 26-35.
- A2-c58 Bik A. J. C., Birkar M., Grey P. M., “Automatic Intra-Register Vectorization for the Intel Architecture,” *International Journal of Parallel Programming*, Vol. 30. No. 2, April 2002, pp. 65-98.
- A2-c57 Bencomo S. D., „Control learning: present and future,” *Proc. 15th Triennial IFAC World Congress*, Barcelona, Spain, 2002, pp. 1-23
- A2-c56 Beltrame G., Brandolese C., Fornaciari W., Salice F., Sciuto D. and Trianni V., “Modelling Assembly Instruction Timing in Superscalar Architectures,” *Proc. 15th International Symposium on System Synthesis (ISSS'02)*, 2002, pp. 132-137.
- A2-c55 Battle J., Martí J., Ridao P. and Amat J., “A new FPGA/DSP-Based Parallel Architecture for Real-Time Image Processing,” *Real-Time Imaging*, vol. 8, no.5, 2002, pp. 345-356.
- A2-c54 Ayala-Rincón M., Neto R.M., Jacobi R.P., Llanos C.H. and Hartenstein R., “Applying ELAN Strategies in Simulating Processors over Simple Architectures,” *Proc. 2nd Int. Workshop on Reduction Strategies in Rewriting and Programming (WRS'02)*, Copenhagen, Denmark, 2002, pp. 127-141.
- A2-c53 Ayala-Rincon M., Neto R.M., Jacobi R.P., Llanos C.H. and Hartenstein R.W., “Applying ELAN Strategies in Simulating Processors over Simple Architectures,” *Electronic Notes in Theoretical Computer Science*, Vol. 70, No. 6, 2002, pp. 1-16.

- A2-c52 Ayala-Rincon M., Hartenstein R.W., Neto R.M., Jacobi R.P. and Llanos C.H., "Architectural Specification, Exploration and Simulation Through Rewriting-Logic," *Columbian Journal of Computation*, Vol. 3, No. 2, 2002, pp. 20-34.
- A2-c51 Wilkinson B., "Processors," in UNESCO's Encyclopedia of Life Support System, Theme 6.45, *Computer Science and Engineering, UNESCO*, 2001, pp. 6.45.2.4/1-12.
- A2-c50 – "Taschenbuch der Informatik", Hanser Fachbuchverlag, 2001.
- A2-c49 Sosnowski J., Jurkiewicz R. and Nowicki J., "Experimental Evaluation of CPU Performance Features," *Proc. Euromicro Symposium on Digital Systems Design (DSD'01)*, 2001, pp. 194-201.
- A2-c48 Schinichi Y., "Method and System for High Performance Implementation of Microprocessors," *USA Patent*, No. 20010044892, 2001, pp. 2-8.
- A2-c47 Rodríguez M.A.V., Pulido J.A.G. and Pérez J.M.S., "Enseñanza de Arquitecturas de Memorias Caché mediante Simuladores," *Actas de las VII Jornadas de Enseñanza universitaria de la Informática*, 2001, pp. 1-7.
- A2-c46 Moschetti F., „A Statistical Approach to Motion Estimation,” PhD Thesis, Lausanne, École Polytechnique Fédérale De Lausanne, 2001, pp. 1-127
- A2-c45 Moore R., Klauer B. and Waldschmidt K., "The SDAARC Architecture," *Proc. 9th Euromicro Workshop on Parallel and Distributed Processing (PDP 2001)*, Mantova, Italy, 2001, pp. 1-7.
- A2-c44 Mišev A. and Gušev M., "Exploring the Register Renaming Design Space Using the Supersim Simulator," *Proc. Second International Conference for Informatics and Information Technology (CIIT 2001)*, Molika, Macedonia, 2001, pp. 57-70.
- A2-c43 May D., Muller H.L. and Smart N.P., "Random Register Renaming to Foil DPA," in Koc C.K., Naccache D., and Paar C., editors, *Proc. Cryptographic Hardware and Embedded Systems (CHES 2001)*, in LNCS 2162 Springer Verlag, May 2001, pp. 28-38.
- A2-c42 May D., Muller H.L. and Smart N.P., "Non-deterministic Processors," in Varadharajan V. and Mu Y., editors, *Information Security and Privacy*, in LNCS 2119, Springer Verlag, July 2001, pp. 115-129.
- A2-c41 Kim J. K., Kim Y. G., Kim T. G., „DHMIF: Devs-Based Hardware Model Interchange Format," *Proc. ESS'2001*, Marseille, 2001, pp. 622-629

- A2-c40 Flynn M. and Hung P., "Computer Architecture," in J. Webster (editor), *Wiley Encyclopedia of Electrical and Electronics Engineering*, New York, etc., 2001.
- A2-c39 El-Kharashi M. W., Elguibaly F., Li K. F., "A Robust stack folding approach for Java processors: an operand extraction-based algorithm," *Journal of System Architecture*, Vol. 47, issue 8, 2001, pages. 697-726.
- A2-c38 El-Kharashi M. W., Elguibaly F. and Li K. F., "Adapting Tomasulo's Algorithm for Bytecode Folding Based Java Processors," *ACM SIGARCH Computer Architecture News*, vol. 29, no. 5, 2001, pp. 1-8.
- A2-c37 Carpinelli J. D., "*Computer Systems Organization and Architecture*," Addison Wesley Longman, 2001.
- A2-c36 Brook R. G., Oppenheimer P. E., Weatherford C. A., "Solving the hydrodynamic formulation of quantum mechanics: A parallel MLS method," *International Journal of Quantum Chemistry*, Vol. 85, issue 4-5, 2001, pages 263-271.
- A2-c35 Broczkó P., "*Műszaki informatika*," SZIF-UNIVERSITAS Kft., Győr, 2001.
- A2-c34 Alamuru S. R. and Vadali R., "*Impact of Thread Management on MultiThreaded Architectures*," Project Report CSE 530, Department of Computer Science and Engineering, The Pennsylvania State University, 2001, pp. 1-13.
- A2-c33 Verians X., "*Extraction du parallélisme entre flots d'instructions à l'aide de techniques superscalaires pour des architectures multiprocesseurs ou multiflot*," Docteur Thesis en Sciences Appliquées, Université Catholique de Louvain, 2000, pp. 1-214.
- A2-c32 Vega M. A., Martin R., Zarallo F. A., Sánchez J. M., Gómez J. A., "SMPCache: Simulador de Sistemas de Memoria Caché en Multiprocesadores Simétricos," *Actas de las XI Jornadas de Paralelismo*, 2000, pp.3-8.
- A2-c31 Sosnowski J., "Improving Fault Coverage in System Tests," *Proc. 6th IEEE International On-Line Testing Workshop (IOLTW)*, 2000, pp. 207-213.
- A2-c30 Salazar J., "Procesadores digitales de señal (DSP) – Arquitecturas y criterios de seleccion," *Mundo Electronico 314*, 2000, pp. 1-7.
- A2-c29 Pessolano F., "*Heterogeneous Clustered Processors Organization and Design*," PhD Thesis, South Bank University, London, 2000.

- A2-c28 Németh Zs., “A Novel Execution Model For Logflow on a Hybrid Multithreaded Architecture,” *Proc. of Distributed and Parallel Systems*, 2000, pp. 117-126.
- A2-c27 Németh Zs., “Abstract Machine Design on a Multithreaded Architecture,” *Future Generation Computer Systems*, Vol. 16, No. 6, 2000, pp. 705-716.
- A2-c26 Naiouf M., De Giusti A., Tarrío D. and De Giusti L., “Métricas y escalabilidad de algoritmos paralelos,” *Proc. of Workshop de Investigadores en Ciencias de la Computación (WICC 2000)*, La Plata, Argentina, pp. 1-3.
- A2-c25 Hu P., “*Translation, Static Analysis and Software Pipelining for Guarded Code*,” PhD Thesis, University Paris, 2000.
- A2-c24 Herbordt M. C., Cravy J., Sam R., Kidwai O. and Lin C., “A System for Evaluating Performance and Cost of SIMD Array Designs,” *Journal of Parallel and Distributed Computing*, Vol. 60, No. 2, 2000, pp. 217 -246.
- A2-c23 Heo S., Kim J. and Ma A., “Next Generation On-chip Communication Networks,” Project Report, No. 6.893, *MIT Laboratory for Computer Science*, 2000, pp. 1-3.
- A2-c22 De Giusti A., Naiouf M., De Giusti L. and Tarrío D., “Análisis y Evaluación de Algoritmos Paralelos sobre diferentes modelos de Aruitecturas multiprocesador,” *Proc. Workshop de Investigadores de Ciencias de la Computación (WICC 2000)*, La Plata, 2000, pp. 1-3.
- A2-c21 Chung L. M., Pean D. L. and Chen C., “Improve Memory Access Latency for F-COMA,” *Proc. International Computer Symposium 2000*, Workshop on Computer Architecture, National Chung Cheng University, Chiayi, Taiwan, 2000, pp. 1-8.
- A2-c20 Benyó B., Fék M., Kiss I., Kóczy A., Kondorosi K., Mészáros T., Román Gy., Szeberényi I., Sziray J., “*Operációs rendszerek mérnöki megközelítésben*,” Panem Könyvkiadó Kft., Budapest, 2000.
- A2-c19 Verplaetse P., Van Campenhout J. and Neefs H., “ESCAPE: Environment for the Simulation of Computer Architectures for the Purpose of Education,” *Technical Committee on Computer Architecture Newsletter*, February, 1999, pp. 57-59.
- A2-c18 Tanenbaum A. S., “*Structured Computer Organization*,” Prentice Hall International, New Jersey, 1999.
- A2-c17 Puiatti J-M., “*Instruction-Level Parallelism for Low-Power Embedded Processors*,” Docteur Thesis No. 2110, École Polytechnique Fédérale de Lausanne, 1999, pp.1-156.

- A2-c16 Mujtaba S. A., "Trends in digital signal processors," *Proc. VLSI Technology, Systems and Applications, International Symposium*, 1999, pp. 108-111.
- A2-c15 Lloyd L., Heron K., Koelmans A.M. and Yakovlev A.V., "Asynchronous Microprocessors: From High Level Model to FPGA Implementation," *Journal of Systems Architecture*, Vol. 45, No. 12-13, 1999, pp. 975-1000.
- A2-c14 Herbordt M.C., Cravy J., Sam R., Kidwai O. and Lin C., "A System for Evaluating Performance and Cost of SIMD Array Designs," *Proc. 7th Symposium on the Frontiers of Massively Parallel Computation*, 1999, pp. 16-24.
- A2-r13 Dvorak V., "Book Review: Advanced Computer Architectures - A Design Space Approach," D. Sima, T. Fountain, P. Kacsuk (Eds.), Addison-Wesley Longman Ltd., 1997, *Microprocessors and Microsystems*, Vol. 2, No. 9, 1999, pp. 571-572.
- A2-c12 Clifton M.H., "Logical Conditional Instructions," *Proc 37th Annual ACM Southeast Regional Conference*, ACM Press, 1999, pp. 1-5.
- A2-r11 Vazbenin A., "Book Review: Advanced Computer Architecture: A Design Space Approach," *IEEE Concurrency*, July-September 1998, pp. 87-88.
- A2-r10 Sotudeh R., "*Times Higher Educational Supplement*," February 1998.
- A2-c9 Shriver B. and Smith B., "The Anatomy of a High-Performance Microprocessor, A Systems Perspective," *IEEE Computer Society Press*, Los Alamitos, CA, 1998, 545 pages
- A2-c8 Pimentel A. D., "*A Computer Architecture Workbench*," PhD Thesis, Universiteit van Amsterdam, 1998.
- A2-c7 Paprzycki M., "High Performance Computing: Challenges for Future Systems," *Concurrency*, Vol. 6, Issue 3, 1998, pp. 85-89.
- A2-c6 Maurer P. M., "Enhancing the Hardware Design Experience for Computer Engineers," *Proc. Frontiers in Education (FIE '98)*, 1998, pp. 1-4.
- A2-c5 El-Kharashi W., Elguibaly F., Li K. F., "Multithreaded processors: the upcoming generation for multimediachips," *Proc. Advances in Digital Filtering and Signal, IEEE Symposium*, 1998, pp. 111-115.
- A2-c4 Crawley D., "An Analysis of MIMD Processor Interconnection Networks for Nanoelectronic Systems," *Report 98/3, Dept. of Physics & Astronomy, University College London*, pp. 1-1.

- A2-r3 Bramer B., "Book Review: Advanced Computer Architecture, A Design Space Approach," *C Vu*, January 1998.
- A2-c2 Crawley D., "An Analysis of MIMD Processor Node Designs for Nanoelectronic Systems," 97/3, Dept. of Physics & Astronomy, University College London, pp. 1-47.
- A2-r1 – "MTA KFKI Mérés- és Számítástechnikai Kutató Intézet hírei," *Akadémia*, 1997 ősz, 57. pages

A1 Sima D. és Haring G.: (eds:) "*The Challenge of Networking: Connecting, Equipment, Humans, Institutions*," Oldenbourg Kiadó, München, 1993, 265 pages

B Book chapters (in English)

- B2 Sima D., "Register Renaming Techniques," in *The Computer Engineering Handbook*, 2nd Edition CRC Press LLC, Boca Raton, etc., 2008, pp. 2.10-2.38. (átdolgozott könyvrészlet)
- B1 Sima D., "Register Renaming Techniques," in *The Computer Engineering Handbook*, CRC Press LLC, Boca Raton, etc., 2002, pp. 6.6-6.30.
- B1-c1 Tran L., Nelson N., Ngai F., Dropsho S. and Huang M, "Dynamically Reducing Pressure on the Physical Register File through Simple Register Sharing," *Proc. IEEE International Symposium on Performance Analysis of Systems and Software (ISPASS'04)*, 2004, pp.1-10.

C Books (in Hungarian)

- C2 Sima D., „*Quo Vadis – Mikroarchitektúra?*”, Mozaikok a magyar informatikából, MIL-ORG Kft, Budapest, 2005, pp. 120-130 (Book chapter)
- C1 Sima D., Fountain T., Kacsuk P., "Korszerű számítógép architektúrák – Tervezési tér megközelítésben," SZAK Kiadó, 1998, 809 pages
- C1-c6 Iványi A., "Párhuzamos Algoritmusok," ELTE Eötvös Kiadó, Budapest, 2003.
- C1-c5 Vargha L., "Ipari Sínrendszerek," ELEKTRONet, 2000/2, 64-67. pages
- C1-c4 Budai A., "Mikroszámítógép-rendszerek," LSI Oktatóközpont, 2000.
- C1-r3 Vajda F., "Könyvszemle," Byte, 1999 június, 21. pages
- C1-c2 Keresztes P., "A VHDL nyelv alkalmazásának lehetőségei a digitális rendszerek és architektúrák oktatásában," *Proc. Informatika a Felsőoktatásban '99*, pp. 21-24.
- C1-c1 Broczkó P., "Műszaki informatika," SZIF-UNIVERSITAS Kft., Győr, 1998.

D Journal papers (in English / German)

- D15 Sima D., "Decisive Aspects in the Evolution of Microprocessors," *Proc. IEEE*, Vol. 92, No. 12, 2004, pp. 1895-1926. (Impact factor: 3.34)
- D15-c8 Youssef A., "Power Management for Deep Submicron Microprocessors," PhD Thesis, University of Waterloo, 2008, pp. 1-150
- D15-c7 Bech S., Carro A. C., "Transparent acceleration of data dependent instructions for general purpose processors," *Proc. VLSI – SoC*, 2007, pp. 66-71
- D15-c6 Bergstra J. A., Middelburg C. A., "Maurer Computers for Pipelined Instruction Processing," Report der Technical University Eindhoven, 2006, 35 pages.
- D15-c5 Stallings W., "Computer Organization and Architecture: Designing for Performance, Seventh Edition, Prentice Hall, 2005, pages 792.
- D15-c4 Lertora F., Borgatti M., "Handling Different Computational Granularity by a Reconfigurable IC featuring Embedded FPGAs and a Network-On-Chip," *Proc. 13th Annual IEEE Symposium on Field-Programmable Custom Computing Machines (FCCM'05)*, 2005, pp. 1-10.
- D15-c3 Kisacanin B., "Examples of Low-Level Computer Vision on Media Processors," *Proc. of the 2005 IEEE Computer Society Conference on Computer Vision and Pattern Recognition (CVPR'05)*, Vol. 3, 135 pages.
- D15-c2 Kisacanin B., Pavlovic V., "Real-Time Algorithms: From Signal Processing to Computer Vision," *Real-Time Vision for Human Computer Interaction*, Springer 2005, pp. 15-40.
- D15-c1 Kisacanin B., "Examples of Low-Level Computer Vision on Media Processors," *Proc. of IEEE Computer Society Conference on Computer Vision and Pattern Recognition (CVPR'05)*, 2005, pp. 1-6.
- D14 Sima D., "The Design Space of Register Renaming Techniques," *IEEE Micro*, Vol. 20, No. 5, 2000, pp. 70-83. (Impact factor: 0.81)
- D14-c42 Sangireddy R., Shah J., "Operand-Load-Based Split Pipeline Architecture for High Clock Rate and Commensurable IPC," *Parallel and Distributed Systems*, Vol. 19. Issue 4., 2008, pp. 529-544.
- D14-c41 Choi M., Maeng S., "An Energy Efficient Instruction Window for Scalable Processor Architecture," *IEICE Transactions on Electronics*, 2008, pp. 1427-1436

- D14-c40 Vandierendonck H., Manet P., Delavallee T., Loïselle I., Legat J.D., "Bypassing the out-of-order execution pipeline to increase energy-efficiency," *Proc. of the 4th International Conference on Computing Frontiers*, 2007. pp. 97-104.
- D14-c39 Yang H., Cui G., Liu H., Yang X., "Compacting register file via 2-level renaming and bit-partitioning," *Microprocessors & Microsystems*, Vol. 31, Issue 3, 2007, pp. 178-187.
- D14-c38 Gaojian C., Jiayue Q., "Design of a High-Speed Low-Power 9-Port Register File," *Chinese Journal of Semiconductors*, Vol. 28, No. 4, 2007, pp. 614-618.
- D14-c37 Yang H., Cui G., Liu H-W., Yang X-Z., "Multi-Usable Rename Register with 2-Level Renaming and Allocating," *Chinese Journal of Computers*, 2006, pp. 1729-1739
- D14-c36 Timothy J., "*Compiler-Directed Energy Savings in Superscalar Processors*," Doctoral Thesis, University of Edinburgh, 2006. pp. 1-155.
- D14-c35 Sangireddy R., "Reducing Rename Logic Complexity for High-Speed and Low-Power Front-End Architectures," *IEEE Transactions on Computers*, Vol. 55, No. 6, June 2006, pp. 672-685.
- D14-c34 Hsu S. K., "*Advanced microarchitecture and Circuit Design Techniques for On-Chip*," Dissertation, Oregon State University, 2006, pp. 1-131.
- D14-c33 Hua Y., Gang C., Hong-Wie L., Xiao-Zong Y., "Multi-Usable Rename Register with 2-Level Renaming and Allocating," *Chinese Journal of Computer*, Vol. 29, No. 10, 2006, pp. 1729-1739.
- D14-c32 Yang H., Cui G., Yang X., "Eliminating Inter-Thread Interference in Register File for SMT Processors," *Proc. Sixth International Conference on Parallel and Distributed Computing Applications and Technologies (PDCAT '05)*, 2005, pp. 40-45.
- D14-c31 Yang H., Cui G., Yang X.Z., "2L-MuRR: A Compact Register Renaming Scheme for SMT Processors," *Lecture Notes in Computer Science*, Springer, Vol. 3758/2005, pp. 407-418.
- D14-c30 Monreal T., Vinals V., Gonzalez A., Valero M., "Hardware support for early register release," *International Journal of High Performance Computing and Networking*, Vol. 3, No. 2-3, 2005, pp. 83-94.
- D14-c29 Kondo M., Nakamura H., "A Small, Fast and Low-Power Register File by Bit-Partitioning," *Proc. 11th Int'l Symposium on High-Performance Computer Architecture, (HPCA '05)*, 2005, pp. 40-49.
- D14-c28 Suresh P., "*PERL – A Register-Less Processor*," Doctoral Thesis, Indian Institute of Technology, Kanpur, 2004. pp. 1-196.

- D14-c27 Petersen W., Arbenz P., "Introduction to Parallel Computing: A Practical Guide with Examples in C," *Oxford University Press*, 2004, 288 pages.
- D14-c26 Müller J., "Schleifenparallelisierung für Prozessoren mit parallelen Funktionseinheiten," PhD Thesis, Technischen Universität Dresden, 2004, 151 pages.
- D14-c25 Monreal T., Vinals V., González J., González A. and Valero M., "Late Allocation and Early Release of Physical Registers," *IEEE Transaction on Computers*, Vol. 53, No. 10, October 2004, pp. 1244-1259.
- D14-c24 Michaud P., "Exploiting the Cache Capacity of a Single-Chip Multi-Core Processor with Execution Migration," *Proc. 10th International Symposium on High-Performance Computer Architecture (HPCA'04)*, Madrid, Spain, 2004, pp. 186-195.
- D14-c23 Darsch A., "L'exécution dans le désordre des jeux d'instructions prédiquées," PhD Thesis, Université de Rennes, 2004, 140 pages.
- D14-c22 Cristal A., Llosa J., Valero M., Ortega D., "Future ILP processors," *International Journal of High Performance Computing and Networking*, Vol. 2, No. 1, 2004, pp. 1-10.
- D14-c21 Barli N. D., "Designing NEKO: A Speculative Multithreading chip Multiprocessor," PhD Thesis, The University of Tokyo, 2004.
- D14-c20 Ayala J. L. and López-Vallejo M., "Improving Register File Banking with a Power-Aware Unroller," *Proc. Workshop on Power-Aware Real-Time Computing (in conjunction with ACM International Conference on Embedded Software)*, September 2004, pp. 1-6.
- D14-c19 Heo C-Y., Choi K-B., Hong I-P. and Lee Y-S., "An Implementation of Scoreboarding Mechanism for ARM-Based SMT Processor," *Proc. 5th International Conference on ASIC*, 2003, pp. 443-446.
- D14-c18 Greene D. A., "A Design, Implementation and Use of the MIRV Experimental Compiler for Computer Architecture Research," PhD Thesis, University of Michigan, 2003.
- D14-c17 Darsch A. and Sez nec A., "Out-of-order Predicated Execution with Translation Register Buffer," *Rapport de Recherche, Inria*, No. 5011, Novembre 2003, pp. 1-25.
- D14-c16 Cristal A., Ortega D., Llosa J. and Valero M., "Kilo-instruction Processors," *Proc. High Performance Computing, 5th International Symposium (ISHPC'03)*, in LNCS 2858, 2003, Tokyo-Odaiba, Japan, pp. 10-25.

- D14-c15 Barli N. D., Tashiro D., Iwama C., Sakai S., and Tanaka H., "A Register Communication Mechanism for Speculative Multithreading Chip Multiprocessors," *Proc. Symposium on Advanced Computing Systems and Infrastructures (SACSYS)*, 2003, pp. 1-8.
- D14-c14 Arnal T. M., "Técnicas Hardware para Optimizar el Uso de los Registros en Procesadores Superescalares," Tesis Doctoral, Universidad de Zaragoza, Departamento de Informática e Ingeniería de Sistemas, 2003.
- D14-c13 Zingiran N., Maresca M., "On the efficiency of image and video processing programs on instruction level parallel processors," *Proc. IEEE*, Vol. 90, Issue 7, 2002, pp. 1230-1243.
- D14-c12 Weldon R. D., Chang S. S., Wang H., Hoflehner G., Wang P. H., Lavery D. And Shen J. P., "Quantitative Evaluation of the Register Stack Engine and Optimizations for Future Itanium Processors," *Proc. 6th Annual Workshop on Interaction between Compilers and Computer Architectures (INTERACT'02)*, 2002, pp. 57-67.
- D14-c11 Sprunt B., "The Basics of Performance-Monitoring Hardware," *IEEE Micro*, vol. 22, no. 4, 2002, pp. 64-71.
- D14-c10 Savransky G., Ronen R. and Gonzalez A., "Lazy Retirement: A Power Aware Register Management Mechanism," *Proc. Workshop on Complexity-Effective Design*, Anchorage, USA, 2002, pp. 1-9.
- D14-c9 Oriol R. G., Sosa O. E., and Salinas M. A. R., "Técnicas de Renombramiento de Registros en Procesadores de Altas Prestaciones," *Proc. 4th International Conference on Control, Virtual Instrumentation and Digital Systems (CICINDI)*, 2002, pp. 1-10.
- D14-c8 Monreal T., Vinals V., González A. and Valero M., "Hardware Schemes for Early Register Release," *Proc. International Conference on Parallel Processing (ICPP'02)*, 2002, pp. 1-9.
- D14-c7 Llana E. M., "Address Prediction and Recovery Mechanism," PhD Thesis, Universitat Politècnica de Catalunya, Spain, 2002, pages 1-197.
- D14-c6 Grävinghoff A., "On the Realization of Fine-Grained Multithreading in Software," PhD Thesis, University Hagen, 2002, 332 pages
- D14-c5 Zingirian N. and Maresca M., "Selective Register Renaming: A Compiler-Driven Approach to Dynamic Register Renaming," *Proc. High Performance Computing & Network (HPCN) Europe, 2001*, pp. 344-352.
- D14-c4 Postiff M., Greene D., Raasch S. and Mudge T., "Integrating Superscalar Processor Components to Implement Register Caching," *Proc. International Conference on Supercomputing (ICS01)*, ACM Press 2001, pp. 348-357.

- D14-c3 Postiff M. A., “*Compiler and Microarchitecture Mechanisms for Exploiting Registers to Improve Memory Performance*,” PhD Thesis, The University of Michigan, 2001.
- D14-c2 Monreal T., Vinals V., González A. and Valero M., “*Early Register Release*,” DIIS Report, RR-01-01, Universidad de Zaragoza, 2001.
- D14-c1 Sainrat P. and Lecussan B., “L’architecture du noeud de la grappe: état de l’art et prospective,” *Proc. School of Winter (IHPerf 2000)*, Aussois, France, 2000, pp. 1.1-1.16.
- D13 Sima D., “The Design Space of Shelving,” *Journal of Systems Architecture*, Vol. 45, No.11, 1999, pp. 863-885. (Impact factor: 0.30)
- D12 Sima D., “Superscalar Instruction Issue,” *IEEE Micro*, Vol. 17, No. 4, 1997, pp. 28-39. (Impact factor: 0.99)
- D12-c21 Colmenar J.M., Moron N., Garnica O., Lanchares J., Hidalgo J.I., “Modelling Asynchronous Systems using Probability Distribution Functions,” *Proc. of the 16th Euromicro Conference on Parallel, Distributed and Network-Based Processing (PDP 2008)*, 2008, pp. 3-11.
- D12-c20 J. Timothy, “*Compiler-Directed Energy Savings in Superscalar Processors*,” PhD Thesis, the University of Edinburgh, 2006, 155 pages.
- D12-c19 Jones T.M., “*Compiler-Directed Energy Savings in Superscalar Processors*,” PhD Thesis, the University of Edinburgh, 2006, 155 pages.
- D12-c18 Colmenar J. M., Garnica O., Lanchares J., Hidalgo J. I., Minana G., Lopez S., “Sym-async: An Architectural Simulator for Asynchronous Processor Modeling Using Distribution Functions,” *Proc. Euro-Par 2006*, LNCS 4128, 2006, pp. 495-505.
- D12-c17 Colmenar J. M., Garnica O., Lanchares J., Hidalgo J. I., Minana G., Lopez S., “Comparing the Performance of a 64-bit Fully-Asynchronous Superscalar Processor versus its Synchronous Counterpart,” *Proc. of the 9th EUROMICRO Conference on Digital System Design (DSD’06)*, 2006, pages 1-8.
- D12-c16 Stallings W., “*Computer Organization and Architecture: Designing for Performance*,” *Prentice Hall*, 2005, 792 pages.
- D12-c15 Shatnawi A., Shatnawi M. F., “Improving Branch Predictors by Combining with Prediated Execution,” *Journal of Electrical Engineering*, Vol. 56, No. 11-12, 2005, pp. 298-305.
- D12-c14 Mitropolszkij J., “Szuperkompjuteri i mikroprocesszori,” *Elektronika*, 2005., pp. 1-7.

- D12-c13 Abella J, Canal R. and González A., "Power- and Complexity-Aware Issue Queue Designs," *IEEE Micro*, Vol. 23, No. 5, 2003, pp. 50-57.
- D12-c12 Huang I. J. and Xie P. H., "Application of Instruction Analysis/Scheduling Techniques to Resource Allocation of Superscalar Processors," *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, Vol. 10, No. 1, 2002, pp. 44-54.
- D12-c11 Chiu J. C., Wang M. J. and Chung C. P., "Design of Instruction Address Queue for High Degree X86 Superscalar Architectures," *Journal of Information Science and Engineering*, Vol. 18, No. 3, 2002, pp. 393-409.
- D12-c10 Lee H., Beckett P. and Appelbe B., "High Performance Extendable Instruction Set Computing," *Proc. 6th Australasian Conference on Computer Systems Architecture (ACSAC)*, 2001, pp. 88-94.
- D12-c9 Gloria A. and Olivieri M., "An Application Specific Multi-Port RAM Cell Circuit for Register Renaming Units in High Speed Microprocessors," *Proc. The 2001 IEEE International Symposium on Circuits and Systems (ISCAS 2001)*, Sydney, 2001, pp. 934-937.
- D12-c8 Chiu J. C. and Chung C. P., "High-Bandwidth x86 Instruction Fetching Based on Instruction Pointer Table," *IEE Proc. Computers and Digital Techniques*, Vol. 148, No. 3, 2001, pp. 113-118.
- D12-c7 Wang L., "On the Boosting of Instruction for Speculative Execution in ILP Processors," PhD Dissertation, Feng Chia University Taiwan, 2000, 50 pages.
- D12-c6 Jih-Ching C., I-Huan H., and Chung-Ping C., "Design of Instruction Stream Buffer with Trace Support for X86 Processors", *Proc. 2000 IEEE International Conference on Computer Design (ICCD' 2000)*, Austin, USA, 2000, pp. 294-299.
- D12-c5 Chiu J.C., Huang I.H., Chung C.P., "Design of instruction stream buffer with trace support for X86processors," *Computer Design*, 2000, pp. 294-299.
- D12-c4 Cameron K. W., "Empirical and Statistical Application Modelling Using On-Chip Performance Monitors," PhD Thesis, Louisiana State University, 2000.
- D12-c3 Tanenbaum A. S., "Structured Computer Organization," Prentice Hall International, New Jersey, 1999.
- D12-c2 Shriver B. and Smith B., "The Anatomy of a High Performance Microprocessor," IEEE Computer Society, Press, Los Alamitos, CA 1998.

- D12-c1 Mitropolskij J., "Supercomputers and Microprocessors," *Electronics* No. 3-4, 1998, pp. 1-5. (orosz nyelven)
- D11 Fenyő I. and Sima D., "Ein didaktischer Versuch zum Unterricht der Mathematik an technischen Universitäten und Hochschulen," *Jahrbuch Überliche Mathematik*, 1985, pp. 139-142.
- D10 Simonyi J., Szauder I., Sima D., Utassy S., Karsa M., Fellner L. and Velkei A., "Noninvasive multiparameter computer analysis of 1000 subjects," *Acta Cardiologica*, Vol.38, No. 4, 1983, pp. 312-334.
- D10-c1 Okayama H., Kumada T., Ozaki M., Sugihara N., Yamagishi T., Utsunomiya H., Yorozu T., Shibata M., Matsuda Y. and Kusakawa R., "Noninvasive Evaluation of Left Ventricular Relaxation by Apexcardiogram in Man," *Journal of Cardiography*, Vol. 14, 1984, pp. 140-142.
- D9 Sima D. and Meinhardt J., "Zu einigen aktuellen Entwicklungstendenzen der Rechentechnik und deren Auswirkungen auf das Gesundheitswesen," *Wissenschaftliche Beiträge der Ingenieurhochschule Dresden*, Vol. 3, 1983, pp. 41-47.
- D8 Sima D. and Meinhardt J., "Zu einigen aktuellen Entwicklungstendenzen der Rechentechnik und deren Auswirkungen auf das Gesundheitswesen," *Rechentechnik/Datenverarbeitung*, Vol. 19, No. 11, 1982, pp. 33-34.
- D7 Sima D., "Einige Entwicklungstendenzen von Mikroprozessor-Architekturen," *Nachrichtentechnik – Elektronik*, Vol. 31, No. 2, 1981, pp. 70-72.
- D6 Sima D., "Formale Beschreibung der logischen Architektur von Rechnern (1)-(2)," *Wissenschaftliche Beiträge der Ingenieurhochschule Dresden*, Vol. 5, 1977, pp. 2-11., Vol. 6, pp. 2-13.
- D6-c1 Lieblich W., "Architektur universeller Mikrorechner," *Proc. Mikroprozessoren und Mikrorechnertechnik in der studentischen Ausbildung und industriellen Anwendungen*, in *Scientific Papers of Wroclaw Technical University*, No. 22, 1982, pp. 5-12.
- D5 Sima D., "Redundanzreduktion – eine Möglichkeit zur Erhöhung der Effektivität zeitgeteilter Informationssysteme," *Zeitschrift der elektrischen Informations- und Energietechnik*, Vol. 2, No. 6, 1972, pp. 346-352.
- D4 Greger R. and Sima D., "Ein Beitrag zur Betrachtung Zeitgeteilter Übertragungssysteme (1)," *Fernmeldetechnik*, Vol. 9, No. 7, 1969, pp. 201-203.
- D3 Greger R. and Sima D., "Ein Beitrag zur Betrachtung Zeitgeteilter Übertragungssysteme (2)," *Fernmeldetechnik*, Vol. 9, No. 8, 1969, pp. 241-246.
- D2 Greger R. and Sima D., "Ein Beitrag zur Betrachtung Zeitgeteilter Übertragungssysteme (3)," *Fernmeldetechnik*, Vol. 9, No. 9, 1969, pp. 271-273.

- D1 Greger R. and Sima D., "Ein Beitrag zur Betrachtung Zeitgeteilter Übertragungssysteme (2)," *Fernmeldetechnik*, Vol. 9, No. 11, 1969, pp. 327-330.

E Conference proceedings (International conferences)

- E9 D. Sima, B. Schmuck, S. Szöllösi, Á. Miklós: „Intelligent Short Text Assessment in eMax,” *IEEE Africon 2007*, Windhoek Namibia, ISBN: 0-7803-8606-x.
- E8 Szöllösi S., Sima D, Schmuck B., „The Design Space of the Services of Knowledge Assessment Systems,” *Proc. 7th International Conference on Information Technology Based Higher Education & Training (ITHET)*, Sydney, 2006, pp. 392-399.
- E7 Schmuck B., Sima D., Szöllösi S., „The Design Space of the Implementation of Knowledge Assessment Systems,” *Proc. 7th International Conference on Information Technology Based Higher Education & Training (ITHET)*, Sydney, 2006, pp. 408-414.
- E6 Csink L., György A., Rainesák Zs., Schmuck B., Sima D., Sziklai Zs. and Szöllösi S., “Intelligent Assessment Systems for e-Learning,” *Proc. 4th European Conference on E-Activities, 2003*, Bucharest, 2003, pp. 224-229.
- E5 Miklós Á. and Sima D., “VSIM – A Superscalar CPU Simulator,” *Proc. 3rd International Conference on Information Technology Based Higher Education and Training (ITHET 2002)*, Budapest, 2002, pp. 561-572.
- E4 Sima D., “Some Aspects of the Functional Evolution of ILP-Processors,” *Proc. International Conference on Information Infrastructure (ICII '96)*, Beijing, 1996, pp. 130-133.
- E3 Sima D., “TEACHSOFT, ein CAL-Programmpaket für den Mathematik-Unterricht,” *Proc. 1990 Frontiers in Education Conference*, Leuchtturm-Verlag, pp. 331-333.
- E3-c1 Sréterné Zs.L. and György A., “TEACHSOFT Educational Programme Package,” *Proc. Conference on Intelligent Systems (CIS'91)*, Veszprém, 1991, pp. 151-155.
- E2 Sima D., “Education of Informatics at Kandó Kálmán College of Electrical Engineering,” *Proc. Information Management*, Budapest, 1990, pp. 24-27.
- E1 Sima D., Kotsis D., Tick J. and Kutor L., “Remor and Rekel Based Knowledge Representation and Manipulation,” *Proc. First Seminar on Artificial Intelligence*, Jan. 1989, Visegrád, Hungary, pp. 41-56.

F Journal papers (in Hungarian)

- F3 Sima D.: Korszakváltás a processzorok fejlődésében, *Alkalmazott Matematikai Lapok*, Vol. 25, 2007, pp. 265-275.

F2 Sima D., Bársony A., Fehér Gy., Géczy L., Kóré L., Tapa B., "Kalkulátor alapú automatikus kromatogram-kiértékelő rendszer," *Mérés és Automatika*, 25. évf., 3. sz., 1977, pp. 94-102.

F1 Sima D., Gregor R., "Időmultiplex átviteli rendszerek," *Híradástechnika*, 21. évf., 9. sz., 1970, pp. 267-270.

G Conference proceedings (Hungarian conferences)

G20 Sima D., Miklós Á., Schmuck B., Szöllösi S., „Rövid szöveges válaszok szemi-automatikus kiértékelése,” *Informatika a Felsőoktatásban előadásai*, Debrecen, 2008. pp. 1-10.

G19 Sima D., "Egymagos szuperskalárok: egy korszak alkonya," *IX. Országos Neumann Kongresszus előadásai*, Győr, 2006. pp. 1-10.

G18 György A., Kos V., Schmuck B., Sima D., Szöllösi S., Vajda I., "Intelligens vizsgakiértékelő rendszer – Előkészítő vizsgáldások –," *IX. Országos Neumann Kongresszus előadásai*, Győr, 2006. pp. 1-7.

G17 Sima D., "Paradigmaváltások a processzorfejlesztésben," *Informatika a Felsőoktatásban előadásai*, Debrecen, 2005, pp. 1-7

G16 Miklós Á., Sima D., "A VSIM szuperskalár processzorszimulátor használata a számítógépes architektúrák oktatásában," *Informatika a Felsőoktatásban 2002 előadásai*, Debrecen, 2002, pp. 285-295.

G15 Sima D., "Mikroprocesszorok fejlődésének meghatározó szempontjai," Oktatási szekció, *VII. Országos Neumann Kongresszus előadásai*, Eger, 2000, pp. 1-11.

G14 Sima D., "Szuperskalár processzorok mikroarchitektúrája," *KKVMF Tudományos Közlemények*, 1998, pp. 67-72.

G13 György A., Csink L., Sima D., "A műszaki informatika brit szakakkreditációja," *Informatika a Felsőoktatásban Konferencia előadásai*, Debrecen, 1996, pp. 131-141.

G12 Sima D., "Mikro-operációs rendszerek néhány kiemelt kérdése," *KKVMF Tudományos Közlemények*, 1984, pp. 182-190.

G12 Fenyő I., Páris Gy., Sima D., "Személyi számítógépek a matematika műszaki főiskolai oktatásban," *Műszaki Főiskolák Matematika, Fizika és Számítástechnika Oktatói 7. Országos Tanácskozása*, Győr, 1984, pp. 20-25.

G11 Tick J., Sima D., Tiszai T., Fellner L., Sima M., Varga I., "M056 rezidens makroassembler INTEL 8080 alapú mikrógépén," *KKVMF Tudományos Közlemények*, 1978, pp. 118-120.

- G10 Fenyő I., Sima D., Siminszky M., "Egy diagnosztikus célt szolgáló tanulóprogram," *Számítástechnikai és kibernetikai módszerek alkalmazása az orvostudományban és a biológiában, 7. Kollokvium előadásai*, Szeged, 1978, pp. 94-106.
- G9 Tóth J., Géczy L., Sima D., Bodnár J., Izsó L., Veress S., Szököndei L.-né, "Integrált információs rendszerek nagy városok szennyvíz-kibocsátó forrásainak ellenőrzésére," *KKVMF Tudományos Közlemények*, 1978, pp. 235-237.
- G8 Sima D., "Számítógépek gépi szintű architektúrájának formális leírása 6-tupellel," *KKVMF Tudományos Közlemények*, 1978, pp. 226-230.
- G7 Fenyő I., Sima D., Bársony A., Fehér Gy., Kóré L., Tapa B., Bachus P., "Számítástechnikai módszereken alapuló on-line kromatogram-kiértékelő módszer," *KKVMF Tudományos Közlemények*, 1978, pp. 207-208.
- G6 Fenyő I., Sima D., Siminszky M., Dobay Z., Ádám K., "Eljárások és programok a cluster analízis számítógépes végrehajtására," *KKVMF Tudományos Közlemények*, 1978, pp. 204-206.
- G5 Farkas I., Géczy L., Kakuk S., Lakatos I., Sághegyi M., Sima D., Sima M., "Az EMG HUNOR 301 asztali kalkulátor néhány fejlesztési kérdése," *KKVMF Tudományos Közlemények*, 1978, pp. 201-204.
- G4 Fenyő I., Sima D., Siminszky M., "Számítógépes eljárás bizonyos praecarcinomás állapotok differenciál-diagnosztizálására," *IV. Orvostechnikai Konferencia előadásai*, Budapest, 1977, pp. 15-16.
- G3 Fenyő I., Sima D., Siminszky M., "Egy „cluster”-eljárás," *Számítástechnikai és kibernetikai módszerek alkalmazása az orvostudományban és a biológiában, 7. Kollokvium előadásai*, Szeged, 1976, pp. 29-39.
- G2 Fenyő I., Bánóczy J., Sima D., Siminszky M., "A clusteranalízis diagnosztikai alkalmazása leukoplakiás betegek carcinoma veszélyeztetettségének megállapítására," *Számítástechnikai és kibernetikai módszerek alkalmazása az orvostudományban és a biológiában, 6. Kollokvium előadásai*, Szeged, 1975, pp. 353-364.
- G1 Sima D., "Kisszámítógép struktúrák," *Számítógéptechnika'74 Konferencia előadásai*, Esztergom, 1974, pp. 78-91.

H Further publications (in Hungarian)

- H8 Sima D., "Gondolatok a kétlépcsős műszaki felsőoktatásról, Bolognai nyilatkozat és a magyar felsőoktatás," *MAB, 2001*, pp. 1-13.
- H7 Agg G., Selényi E., Sima D., "A brit akkreditáció gyakorlata," *Magyar Felsőoktatás*, 6. szám, 1993, pp. 22-23.

- H6 Sima D., Szabó I., “A nyelvrontás ellen – az egységes számítástechnikai nyelvért,” *Élet és Tudomány* 40. évf., 16. sz., 1985, pp. 491-492.
- H5 Sima D., Szabó I., “Számítástechnika – magyarul?,” *Magyar Nemzet*, 48 évf., 244. sz., 1985.
- H4 Sima D., “A személyi számítógépek fejlődése,” *Információ – Elektronika*, 17. évf., 4. sz., 1982, pp. 187-193.
- H3 Sima D., Szabó G., Tick J., Tiszai T., “A VT 20 BASIC programozási rendszere,” *Videoton Software Tájékoztató*, 1-2. sz. 1981, pp. 16-19.
- H2 Györi J., Sima D., “A terminológia szabványosítása,” *Számítástechnika*, 11 évf., 9. sz., 1980, 15. pages
- H1 Ivanyos L., Sima D., “Fortran nyelvű matematikai programkönyvtár 1010B számítógépre,” *Videoton Software Tájékoztató*, 1. sz., 1975, pp. 29-35.

I Lecture notes (in English)

- I2 Sima D., Kacsuk P., “*Parallel Architectures*,” (Tempus lecture notes), 1997, 455 pages, the part written by me: 248 pages.
- I1 Sima D., Polacsek L., Koschek V., “*Computer Architectures I*,” European Informatics Student’s Series, lecture notes of Kandó Műszaki Főiskola, Budapest, South Bank University, London, Hochschule Bremen és Technological and Education Institute, Patras, Budapest, 1993, the part written by me: 188 pages.

J Strategic studies (in Hungarian)

- J3 Társszerzőként, “*Felsőoktatási Informatikai Stratégia*,” MKM, 1997.
- J2 Kovács M., Gantner J., Hajdú B., Kiss I., Moharos I., Sima D., Sziklai K., Zámori Z., Zöld S., “*Át- és továbbképző bázisok rendszerének kialakítása*,” LSI ATSZ Tanulmányterv, 1982.
- J1 Sima D., “*Személyi számítógépek fejlődésének áttekintése, az iskolai és személyi számítógép alapú számítástechnikai rendszerek hazai gyártásának és alkalmazásának lehetőségei*,” part of the OMF B Study 16-8006-T.sz., 1981, 23-35. pages.