Institute of Cyber-physical Systems						
Name of the subject:	Code of the subject:	Credits:	Weekly hours:			
				lec	sem	lab
Digital Systems	NKXDR1EBNF	4	full-time	2	0	2
Responsible person for the subject: Dr. Mehdi Taassori			Classification:			
Subject lecturer(s):						
Prerequisites:						
Way of the assessment:	Mid-term mark					

Course description	
Goal:	The goal of a course is to provide students with a thorough understanding of digital logic design. The course aims to teach the foundational principles and techniques for designing, analyzing, and implementing digital systems.
Course description:	This course covers topics such as Boolean algebra, combinational and sequential logic circuits, and the principles behind designing and analyzing digital systems. Students will learn about logic gates, flip-flops, registers, counters, and memory elements.

Lecture schedule	
Education week	Topic
1.	Introduction, Digital Representation of Information, Number System
2.	Conversion, Fixed Point Numbers, Conversion of Fixed Point Numbers
3.	Binary Arithmetic: Addition of Unsigned Numbers, Subtraction, Signed and Magnitude Numbers, 2's Complement Addition, 2's Complement Subtraction
4.	Binary Arithmetic: Arithmetic Overflow, Binary Multiplication, Binary Coded Decimal, ASCII Character Code, Unicode o ASCII Parity Bit, Gray Codes
5.	Boolean Algebra: Logical Operations, Logic Gates, Boolean Expressions and Truth Tables, Combinational Logic Circuits, Analysis of a Combinational Logic Network, Complementing Boolean Expressions, Complementing Logic Gates
6.	Boolean Algebra: Optimization of Combinational Circuits, Sum of Products, Product of Sums, Minterms o Maxterms, Canonical SOP, Canonical POS, Canonical forms conversion
7.	Karnaugh Map: Two, Three, Four and Five Variable Karnaugh Maps, Literal, Implicant, Prime Implicant, Essential Prime Implicant, Minimization Procedure, Determination of Minimum Expressions Using Essential Prime Implicants, Incompletely Specified Functions
8.	Decoder and Encoder: Binary Decoder, Implementing Combinational Circuit Using Decoder, Design 4 to 16 Decoder using 3 to 8, 7-Segment Decoder, Encoder, Priority Encoder
9.	Multiplexer and Demultiplexer: Multiplexers, Quad Multiplexer, Implementation by MUX, Demultiplexer
10.	Combinational Logic Circuits: Half Adder, Full Adder, Ripple Carry Adder, Subtractor, Multiplier
11.	Latch, Flip Flop: D Flip Flop, Comparison of level sensitive & edge triggered D storage elements, Master-Slave FF configuration using SR latches, Master Slave JK Flip-Flop, JK Flip Flop, T Flip Flop, Flip-Flops with Additional Inputs, Asynchronous Clear-Preset, Synchronous Clear
12.	Analysis of Sequential Circuit: Synchronous vs. Asynchronous, Synchronous Circuits, Sequential Circuits, State Table, State Diagram, Timing Chart, State Table with Multiple Inputs & Outputs, State Diagram with Multiple Inputs & Outputs
13.	Theoretical Exam – Lab Exam
14.	Retake Theoretical Exam – Retake Lab Exam

Mid-term requirements	
Conditions for obtaining a mid-term grade/signature	Written exam, , Lab exam, Quizzes, Homeworks, Project

Assessment schedule	
Education week	Topic
13	Theoretical Exam – Lab Exam
14	Retake Theoretical Exam – Retake Lab Exam

Method used to calculate the *mid-term grade* (to be filled out only for subjects with mid-term grades)

- Homework 10%
- Quiz 0 - 10%
- Lab 15%
- Project 0 - 5%
- Exam 60% - 75%

Type of the replacement	
Type of the replacement of written test/mid-term grade/signature	Retake exam: once in the first 10 working days of the examination period.

Type of the exam (to be filled out only for subjects with exams)

Written exam

Calculation of the exam mark (to be filled only for subjects with exams)

- Homework 10%
- Quiz 0 - 10%
- Lab 15%
- Project 0 - 5%
- Exam 60% - 75%
- The submission of homework and project by the designated deadline is mandatory for all students.
- Attendance for lab sessions, lab exam, quizzes, and the exam is mandatory.
- Conducting the quiz and delivering the project depends on the class schedule.
- A minimum of 51% must be achieved in each exam to pass.

Final grade calculation methods:

0-59 points - Fail
60-69 points - Pass
70-79 points – Satisfactory
80-89 points - Good
90-100 points - Excellent

References	
Obligatory:	Stephen Brown, and Zvonko Vranesic. Fundamentals of Digital Logic with Verilog Design. Third Edition. New York: McGraw-Hill, 2014.
Recommended:	Charles H. Roth Jr., and Larry L. Kinney, Fundamentals of Logic Design. Seventh Edition, Cengage Learning, 2020.
Other references:	