Institute of Cyberphysical Systems			Semester 2. of the curriculum 2025-26-2			
Name of the subject:	Code of the subject:	Credits:	Hours per semester:			
				lec	sem	lab
Computer architectures	NKXSA1EMLF	4	part-time	15	0	0
Responsible person for the subject: Prof. Dr. SIMA Dezső			Classification: professor emeritus			
Subject lecturer(s): Zoltan Fried						
Prerequisites:						
Way of the assessment:	exam					

Course description

Goal:	The aim of the course is to provide students with a deeper understanding of the internal structure and operating mechanisms of computers and processors, and to introduce them to the main concepts, cause-effect relationships and emerging trends. The course will introduce students to instruction-level architectures, the microarchitecture of traditional Neumann computers. The approach of the course is based on the design space concept and focuses on concrete implementation examples and trends.
Course description:	Topics: Computing models, architectures, ISA. Memory space and register space. Data types, operations, operand types, instruction formats, addressing modes. Usermanageable state attributes. RISC, CISC architectures and main features of the most common instruction level architectures. Operation execution unit, operation execution, the principle of parallel addition and multiplication. Basics of bus system, types of buses, parallel/serial buses, main features of most important parallel and serial buses (FSB, USB, PCIe, HT, QPI). DMA, and interrupt system. The concept of DRAM, types of DRAM technologies (SDRAM, DDR memory generations). Evolution of transistor technology. Levels of parallelism that can be exploited. Flynn and modern classification of processors. Data, control and resource dependencies and their main management techniques and how to maintain sequential consistency. Conveyor belt and superscalar processors. ISA extensions (MMX, SSE, ...). Cache organization alternatives, cache coherence, trends, examples. Processor performance issues. Main areas of dissipation management. Thread level and process level parallel architectures.

Lecture schedule

Education week	Topic
1.	Computing models, the concept of architecture, data space, register space
2.	Instruction processing thread, state space, state operations, building blocks of microprocessors
3.	Arithmetic-logic unit structure, working principle. Operation executor
4.	Floating point number representation, IEEE754 standard
5.	Bus system, I/O system, DMA
6.	Interrupt system, Memory, addressing modes,
7.	Transistor technology evolution
8.	Introduction to parallel processing, dependencies and sequential consistency
9.	Pipeline architectures, CISC-RISC architectures
10.	1st, 2nd and 3rd generation superscalars. ISA extensions. Netburst architecture

11.	Performance, dissipation and frequency constraints, thread and process level parallel architectures
12.	Alternatives for cache organisation
13.	Lecture Test
14.	Substitution of lecture Test

Mid-term requirements

Conditions for obtaining a mid-term grade/signature	Pass mark of at least 51% in the Test lecture

Assessment schedule

Education week	Topic
13.	Lecture Test based on the lecture material
14.	Replacement of the lecture Test based on the lecture material.

Method used to calculate the *mid-term grade* (to be filled out only for subjects with mid-term grades)

Test result needs to exceed 51%.

Type of the replacement

Type of the replacement of written test/mid-term grade/signature	In week 14, Test can be replaced. A minimum of 51% must be achieved in Test to pass.

Type of the exam (to be filled out only for subjects with exams)

Written exam
Admission to the examination is only possible if the subjects specified as prerequisites have been passed. Students write an examination paper during the examination period in order to obtain a mark. The marking of questions is linear. Bonus marks will be awarded for a logical, clear and convincing answer to each question, and malus marks for a mosaic, confused and uncertain answer. Marks for drawings will only be awarded if their context (description of operation, example, etc.) demonstrates understanding. Successful is the examination paper,

- at least 15% of all questions have been answered, and
- at least the minimum score per paper is achieved.

Calculation of the exam mark (to be filled only for subjects with exams)

The minimum score (out of 100%): 60% with the first exam, which increases by 6% after the first failed exam.

Final grade calculation methods:

Exam mark	First time score in %	After first failed exam, in %
pass (5)	90-100	90-100
good (4)	80-99	80-99
average (3)	70-79	70-79
fair (2)	60-69	66-69
unsatisfactory (1)	<60	<66

References

Obligatory:	– Materials published on Moodle
Recommended:	– D. Sima, T. Fountain és P. Kacsuk: Advanced Computer Architectures, Addisson Wesley Longman 1997 – J. L. Hennessy és D. A. Patterson: Computer Architecture: A Quantitative Approach, Morgan Kaufmann Inc., San Mateo, 2002
Other references:	The slides used in the lecture will be available on the course website at

	https://elearning.uni-obuda.hu/ after the lecture.